INDUSTRIAL and COMPUTER PERIPHERAL ICs

DATABOOK

2nd EDITION

FEBRUARY 1992

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED.

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS OF LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics.

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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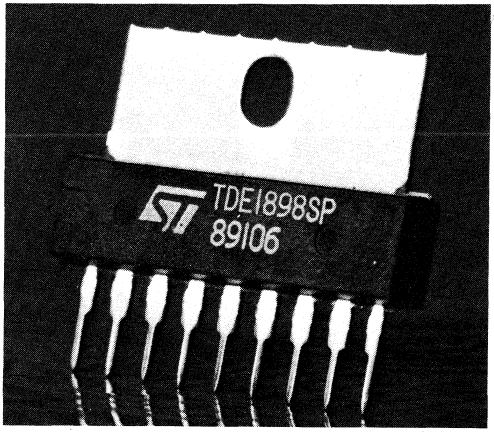
INDUSTRIAL AND COMPUTER PERIPHERAL ICs: TECHNOLOGY IS THE KEY TO SUCCESS

Since the first high power ICs emerged at the end of the 1960's SGS-THOMSON has set the pace in power IC process technology, plastic power packages and innovative circuit design.

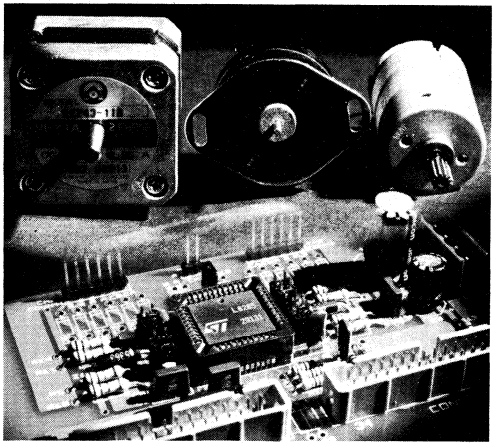
Originally this technology knowhow was applied to consumer circuits such as high power amplifiers and TV vertical deflection stages, so when motor driving ICs arrived at the end of the seventies SGS-THOMSON already possessed a unique understanding of the problems involved and, more importantly, how they could be solved.

SGS-THOMSON is not just the leader in smart power technology, it is also the number one supplier of smart power ICs and power ICs in the world (Dataquest ranking), with a clear lead over the second ranked supplier.

Many of the milestones in smart power technology have been developed by SGS-THOMSON and many are still unmatched. Today's leading edge is a family of smart power technologies integrating bipolar, CMOS and DMOS on the same chip. Using this technology the company has produced a new generation of ultra-efficient power Ics that are changing the whole approach to power system design.



SGS-THOMSON's Multipower-BCD smart power technology makes it possible to make power ICs that dissipate little power, reducing costs by eliminating heatsinks, cooling fans and so on. Already used in a wide variety of motion control circuits, this technology is now applied to produce switch ICs for industrial control applications, like the TDE1898 shown here.



Multipower-BCD technology allows the integration of very complex smart power systems having many power stages. Thanks to the low dissipation of DMOS power stages a PLCC package is suitable even for circuits like this - a single chip that controls and drives three motors.

This book contains many examples of the way this technology can be applied, ranging from simple drivers like the L6202 DMOS H bridge to complex circuits like the L6285 which integrate three complete driver channels plus interface logic.

In all of these "BCD" circuits dissipation is very low. The L6202, for example, is housed in a DIP package yet delivers 70W to the load. And the L6285, though it integrates all of the power subsystems needed in a printer mechanism, dissipates so little it is assembled in a PLCC package.

Other world-beating products described in this book include a new family of BCD intelligent power switches for industrial control applications, and a family of single-chip switching regulators that deliver up to 10A.

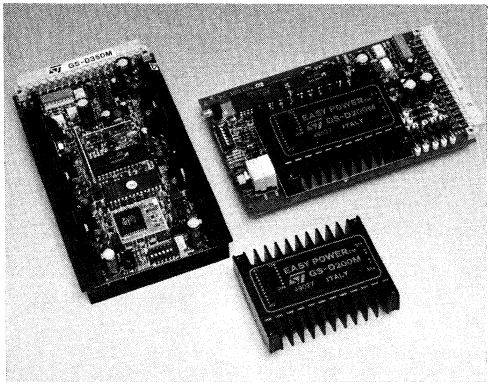
Today more than ever technology is the key to a successful product, and with unique power technologies like the 2nd generation BCD-II process, SGS-THOMSON is able to produce power ICs that are a generation ahead of anything else on the market.

SUBSYSTEMS MODULES AND BOARDS: THE SHORTEST WAY TO MARKET YOUR IDEAS

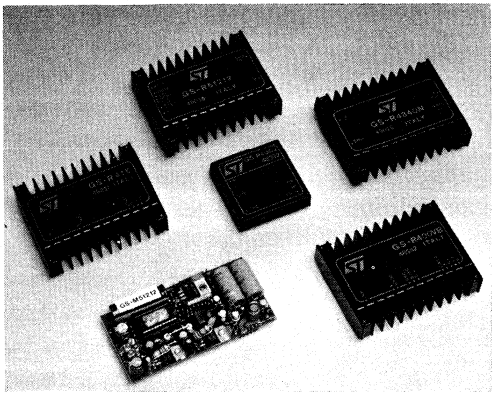
SGS-THOMSON Microelectronics is widely acknowledged as both a technology and a market leader in the field of smartpower, thanks to its portfolio of smartpower technologies and its expertise in power packaging. The SUBSYSTEMS products exploit the company's capabilities in these areas, as well as its considerable in-house applications expertise in power supply design and motor control.
The result is a range of high performance modules and boards that are not only "SMART POWER", but EASY POWER™ too: complete functions for immediate use.

Major advantages to the customer include faster product design, reduced design, assembly and test costs and increased reliability. In addition, many of the standard subsystems can be adapted to meet special customer requirements.

This book contains detailed datasheets for DC-DC converters, switching regulators, stepper motor driver modules and boards in addition to a very useful PRODUCT SELECTION GUIDE for all products.



Taking advantage of its own advanced Multipower-BCD smartpower technology, SGS-Thomson has developed rugged, flexible modules that implement a complete stepper motor driver function.
The GS-D200M, GS-D250M an GS-D350M modules assure smooth and resonance-free operation and gives the user complete control over the electromechanical characteristics of the motion system.
The modules include many features that guarantee safe and versatile operating conditions, making them the simplest and most cost-effective solution for any stepper motor driving requirement.



Compact, lightweight, standard sized step-down regulators offering a solution to a wide range of applications, including battery powered equipments, peripheral equipments, industrial controllers, small uninterruptable power supplies.
The GS-R400 Family, supplied in finned, aluminium case, have "Soft Start", "Remote Sense", Logic level "Inhibit", crowbar and short circuit protection built-in. The GS-R400/2 Family are supplied in a reduced size module giving a power density of 24 watts/in^3.

Among the products featured are GS-C200 and GS-C200S intelligent stepper motor controllers which contain built-in command interpreters and EEPROM memories, thus allowing complex motion sequences to be programmed and stored; the GS-D range of stepper motor drivers, the GS-R family of switching regulators and many compact DC-DC converter modules, including models aimed at ISDN, LAN and other industrial and general purpose applications.

In addition to the range of products described in this book, SGS-THOMSON designs and manufactures a wide range of custom DC-DC converters as well as switching voltage regulators, to O.E.M. specifications and requirements.

Like every product family in SGS-THOMSON, this range of modules is continuously growing.

In case you don't find what you need, just call us and we may have an answer to your requests.

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GS-C200	Intelligent Stepper Motor Controllers Module	865
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GS-R1005	50W Step-Down Switching Regulator Module	1111
GS-R51212	20W Triple Output Step-Down Switching Regulator Module	1117
GS-R51212S	31W Triple Output Step-Down Switching Regulator Module	1021
GS-R51515S	31W Triple Output Step-Down Switching Regulator Module	1021
GS-T25-0500	25-30 Watt DC-DC Converters Module	1029
GS-T27-0600	25-30 Watt DC-DC Converters Module	1029
GS-T30-1200	25-30 Watt DC-DC Converters Module	1029
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L149	4A Linear Driver	45
L165	3A Power Operational Amplifier	49
L200	Adjustable Voltage And Current Regulator	57
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L290	Tachometer Converter	77
L291	5 Bit D/A Converter And Position Amplifier	83
L292	Switch-Mode Driver For Dc Motors	89
L293B/E	Push-Pull Four Channel Driver	99
L293C	Push-Pull Four Channel/Dual H-Bridge Driver	107
L293D	Push-Pull Four Channel Driver With Diodes	111
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L2720/2/4	Low Drop Dual Power Operational Amplifiers	179
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L4964	High Current Switching Regulator	239
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L5170A/D	Octal Line Driver	351
L6114/5	Quad 100V DMOS Switch	357
L6122/23	100V DMOS Switches	365
L6201/2/3	DMOS Full Bridge Drivers	371
L6204	DMOS Dual Full Bridge Drivers	387
L6210	Dual Schottky Diode Bridge	395
L6213	Solenoid Driver + SMPS	399
L6219	Stepper Motor Driver	407
L6220/N	Quad Darlington Switch	415
L6221A/N	Quad Darlington Switch	425
L6221C/N	Quad Darlington Switches	437
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MC3479C	Motor Driver	635
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SG1524	Regulating PWM	653
SG1525A	Regulating PWM	661
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SG42524	Regulating PWM	653
SG2525A	Regulating PWM	661
SG43524	Regulating PWM	653
SG3525A	Regulating PWM	661
SG3527A	Regulating PWM	661
TDA0161	Proximity Detector	671
TDE0160	Proximity Detector	675
TDE1707	Intelligent Power Switch	681
TDE/TDF1737	Intelligent Power Switch	685
TDE1747/TDF1747	Intelligent Power Switch	689
TDE1767/87/A	Intelligent Power Switch	697
TDE1798	Intelligent Power Switch	705
TDE3237	Intelligent Power Switch	717
TDF1778	Dual 2A Source Driver	721
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TEA3717	Stepper Motor Driver	737
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ULN2001A	Seven Darlington Array	797
ULN2002A	Seven Darlington Array	797
ULN2003A	Seven Darlington Array	797
ULN2004A	Seven Darlington Array	797
ULN2064B	80V Quad Darlington Switch	801
ULN2065B	50V Quad Darlington Switch	809
ULN2066B	80V Quad Darlington Switch	801
ULN2067B	50V Quad Darlington Switch	809
ULN2068B	80V Quad Darlington Switch	801
ULN2069B	50V Quad Darlington Switch	809
ULN2070B	80V Quad Darlington Switch	801
ULN2071B	50V Quad Darlington Switch	809
ULN2074B	80V Quad Darlington Switch	801
ULN2075B	50V Quad Darlington Switch	809
ULN2076B	80V Quad Darlington Switch	801
ULN2077B	50V Quad Darlington Switch	809
ULN2801A	Eight Darlington Array	817
ULN2802A	Eight Darlington Array	817
ULN2803A	Eight Darlington Array	817
ULN2804A	Eight Darlington Array	817
ULN2805A	Eight Darlington Array	817
ULQ2001A	Seven Darlington Arrays	823
ULQ2002A	Seven Darlington Arrays	823
ULQ2003A	Seven Darlington Arrays	823
ULQ2004A	Seven Darlington Arrays	823
ULQ2801A	Eight Darlington Arrays	827
ULQ2802A	Eight Darlington Arrays	827
ULQ2803A	Eight Darlington Arrays	827
ULQ2804A	Eight Darlington Arrays	827
ULQ2805A	Eight Darlington Arrays	827

SELECTION GUIDE

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

SGS-THOMSON DATABOOKS

DB		ORDER CODE
a	4 BIT MCU FAMILY ET9400	DBET9400ST/1
b	8 BIT MCU FAMILIES EF6801/04/05	DB68XXST/1
c	16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
d	AUDIO POWER and PROCESSING ICs	DBAUDIOPROST/1
e	AUTOMOTIVE PRODUCTS	DBAMOTIVEST/1
f	ANALOG CELLS AND ARRAYS	DBANACA/1090
g	CB12000 SERIES STANDARD CELLS	DBCB12ST/1
h	CB12000 SERIES STANDARD CELLS MODULE GENERATORS	DBCB12GEN/1
i	CMOS B SERIES	DBCMOSBST/1
j	CMOS LINEAR	BKCMOSLIN/0490
k	DATACOM PRODUCTS	DBDATACOMST/1
l	HIGH SPEED CMOS	DBHSCMOSST/1
m	IMAGE PROCESSING	DBIMAGEPROST/1
n	INDUSTRY STANDARD ANALOG ICs	DBSTANDANAST/1
o	ISDN ICs	DBISDNICST/1
p	ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12KST/1
q	SUBSYSTEMS PRODUCT PROFILE	BKSUBST/1
r	ISB18000 SERIES CONTINUOS ARRAYS	DBISB18/1
s	LINE CARD ICs	DBLINCARDST/1
t	LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
u	MACROFUNCTION LIBRARY DATABOOK	DBMACRO/1
v	MODEM	DBMODEMST/1
w	NON-VOLATILE MEMORIES	DBNVMST/1
y	POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
z	POWER MODULES	DBPOMODULEST/1
aa	POWER MOS DEVICES	DBPOWERMOSST/1
ab	PROTECTION DEVICES	DBPROTECST/1
ac	RF & MICROWAVE POWER TRANSISTORS	DBRFST/1
ad	SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
ae	SCRs & TRIACS	DBSCRTRIST/2
af	STATIC RAMs	DBSRAM/2
ag	ST8 MCU FAMILY	SGST8ST/1
ah	TELEPHONE SET ICs	DBTELSETST/1
ai	THE GRAPHICS DATABOOK	72TRN20400
aj	THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
ak	THE TRANSPUTER DATABOOK	72TRN20300
al	THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21900
am	THE T9000 TRANSPUTER	DBTRANSPST/1
an	VIDEO PRODUCTS POWER & GRAPHICS	DBPOMGRAST/1
ao	VIDEO PRODUCTS SIGNAL PROCESSING	DBTVCRSPST/1
ap	Z8 MCU FAMILY	BKZ8SELEC/0289
aq	Z80 MICROPROCESSORS FAMILY	DBZ80ST/1
ar	ZENER, SCHOTTKY & RECTIFIER DIODES	DBDIODEST/1
▲	NOT INCLUDED IN CURRENT DATABOOKS, CONTACT YOUR NEAREST SGS-THOMSON SALES OFFICE	

SINGLE CHIP MULTIPOWER

Type Number	Description	Package	Page/DB
L6280	Three Channels Multipower System	PLCC44	517
L6285	Three Channels Multipower System	PLCC44	541
L6286	Three Channels Multipower System	PLCC44	555

SOLENOID DRIVERS

Type Number	Description	Package	Page/DB
ESM1600B	Quad Comparator Interface Circuit	DIP14/SO16	29
ESM1602B	Quad Comparator Interface Circuit	DIP14/SO16	37
L294	Switch-Mode Solenoid Driver	MULTIWATT11	115
L295	Dual Switch Mode Solenoid Driver	MULTIWATT15	121
L601/2/3/4	Darlington Array	DIP18	171
L702	2A Quad Darlington Switch	MULTIWATT11/8+8	175
L6114/15	Quad 100V DMOS Switch	MULTIWATT15/14+3+3	357
L6122/23	100V DMOS Switch	MULTIWATT15/14+3+3	365
L6213	Solenoid Driver + SMPS	16+2+2	399
L6220/N	Quad Darlington Switch	MULTIWATT15/16+2+2	415
L6221A/N	Quad Darlington Switch	MULTIWATT15/16+2+2	425
L6221N/CN	Quad Darlington Switches	MULTIWATT15	437
L6504	Solenoid Controller	DIP14	569
TDE1707	Intelligent Power Switch	SO8	681
TDE/TDF1737	Intelligent Power Switch	MINIDIP/SO14	685
TDE1747	Intelligent Power Switch	SO14	689
TDE1767/87A	Intelligent Power Switch	MINIDIP	697
TDE1798	Intelligent Power Switch	MINIDIP	705
TDE3237	Intelligent Power Switch	MINIDIP/SO14	717
TDF1778	Dual 2A Source Driver	MULTIWATT11	721
TDF1779A	Dual 2A Source Driver	MULTIWATT11	729
ULN2001A to 2004A	Seven Darlington Arrays	DIP16/SO16	797
ULN2064B to 2076B	Quad Darlington Switches	12+2+2	801
ULN2065B to 2077B	Quad Darlington Switches	12+2+2	809
ULN2801A to 2805A	Eight Darlington Arrays	DIP18	817
ULQ2001A to 2004A	Seven Darlington Arrays	DIP16/SO16	823
ULQ2801A to 2805A	Seven Darlington Arrays	DIP18	827

DC MOTOR DRIVERS

Type Number	Description	Package	Page/DB
L149	4A Linear Driver	PENTAWATT	45
L165	3A Power Operational Amplifier	PENTAWATT	49
L272/M	Dual Power Operational Amplifier	MINIDIP/8+8	67
L272D	Dual Power Operational Amplifier	SO16	73
L290	Tachometer Converter	DIP16	77
L291	5 Bit D/A Converter and Position Amplifier	DIP16	83
L292	Switch-Mode Driver for DC Motors	MULTIWATT15	89
L293B/E	Push-Pull Four Channel Drivers	DIP16/16+2+2	99
L293C	Push-Pull Four Channel	16+2+2	107
L293D	Push-Pull Four Channel Driver with Diodes	12+2+2	111
L298N	Dual Full Bridge Driver	MULTIWATT15	161
L2720/2/4	Low Drop Dual Power Operational Amplifier	MINIDIP/8+8/SIP9	179
L2726	Low Drop Dual Power Operational Amplifier	SO20	187
L2750	Dual Low Drop High-Power Amplifier	MULTIWATT11	191
L6201/2/3	DMOS Full Bridge Drivers	SO20/12+3+3 MULTIWATT11	371
L6204	DMOS Dual Full Bridge Drivers	16+2+2	387
L6242	Voice Coil Motor Driver	SO20	503
L6243/D	Voice Coil Motor Driver	PLCC44/SO28	507
L6515	Dual DC Motor Positioning System	PLCC44	583

UNIPOLAR STEPPER MOTOR DRIVERS

Type Number	Description	Package	Page/DB
L297/A	Stepper Motor Controllers	DIP20	151
L702	2A Quad Darlington Switch	MULTIWATT11/8+8	175
L6122/23	100V DMOS Switches	MULTIWATT15/14+3+3	365
L6506/D	Current Controller For Stepping Motors	DIP18/SO20	577
ULN2064B to 2076B	Quad Darlington Switch	12+2+2	801
ULN2065B to 2077B	Quad Darlington Switch	12+2+2	809

BIPOLAR STEPPER MOTOR DRIVERS

Type Number	Description	Packages	Page/D/B
L297/A	Stepper Motor Controller	DIP20	151
L298N	Dual Full Bridge Driver	MULTIWATT15	161
L6201/2/3	0.3 Ω DMOS Full Bridge Driver	MULTIWATT11/ SO20/14+3+3	371
L6204	Voice Coll Motor Driver	16+2+2	387
L6210	Dual Schottky Diode Bridge	12+2+2	395
L6219	Stepper Motor Driver	20+2+2	407
L6506/D	Current Controller For Stepping Motors	DIP18/SO20	577
MC379C	Motor Driver	12+2+2	635
PBL3717A	Stepper Motor Driver	12+2+2	643
TEA3717	Stepper Motor Driver	12+2+2	737
TEA3718/S	Motor Driver	MULTIWATT15/12+2+2	745
TEF3718S	Stepper Motor Driver	MULTIWATT15/12+2+2	757

BRUSHLESS MOTOR CONTROLLERS

Type Number	Description	Packages	Page/DB
L6232A	Spindle Motor Driver	PLCC44	481
L6232B	Spindle Motor Driver	PLCC28	489
L6234	Three Phase Motor Driver	POWERDIP 16+2+2/ SO 16+2+2/ FLEXIWATT21	497

SWITCHING REGULATORS

Type Number	Description	Packages	Page/DB
L296/P	High Current Switching Regulator	MULTIWATT15	127
L4960	2.5A Power Switching Regulator	HEPTAWATT	199
L4962	1.5A Power Switching Regulator	12+2+2	213
L4963/D	1.5A Switching Regulator	SO16/12+2+2	225
L4964	High Current Switching Regulator	MULTIWATT15	239
L4970A	High Current Switching Regulator	MULTIWATT15	251
L4972A	2.0A Switching Regulator	SO20/16+2+2	271
L4974	3.5A Switching Regulator	POWERDIP 16+2+2	291
L4975A	5A Switching Regulator	MULTIWATT15	311
L4977A	7A Switching Regulator	MULTIWATT15	331
SG1524	Regulating Pulse Width Modulator	DIP16/SO16	653
SG1525A	Regulating Pulse Width Modulator	DIP16/SO16	661
UC2842/45	Current Mode PWM Controller	MINIDIP/SO14	781
UC3842/45	Current Mode PWM Controller	MINIDIP/SO14	781

SPECIAL FUNCTIONS

Type Number	Description	Packages	Page/DB
ESM1600B	Quad Comparator Interface Circuit	DIP14/SO14	29
ESM1602B	Quad Comparator Interface Circuit	DIP14/SO14	37
L149	4A Linear Driver	POWERDIP	45
L200	Adjustable Voltage And Current Regulator	POWERDIP/TO3 (4L)	57
L5170A/D	Octal Line Driver	DIP28/PLCC28	351
L6210	Dual Schottky Diode Bridge	12+2+2	395
L6213	Solenoid Driver + SMPS	16+2+2	399
L6242	Voice Coil Motor Driver	SO20	503
L6603A/4A	Memory Card Interface	DIP28/PLCC28	613
L6605	Smart Card Interface	12+3+3	603
L6720/21	Minitel Interface	12+2+2	611
MC1488	RS232C Quad Line Driver	CERDIP14/DIP14	619
MC1489/A	RS2S2C Quad Line Receiver	CERDIP14/DIP14	627
TDA0161	Proximity Detector	MINIDIP/SO8	671
TDE0160	Proximity Detector	MINIDIP/SO14	675
TL7700A	Supply Voltage Supervisors	MINIDIP/SO8	763
UAA4713	Motion Detector Interface	DIP14/SO14	769

SUBSYSTEMS MODULES

DC-CD CONVERTERS FOR GENERAL PURPOSE APPLICATIONS

Single Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt/mA	Dimensions L · W · H (mm)	Package	Page/DB
GS-1I5-5*	1	4.50 ÷ 5.50	5 / 250	35.6 · 21.6 · 14	B	q
GS-1I12-5*	1	10.8 ÷ 13.2	5 / 150	33 · 33 · 16.5	C	▲
GS-2I5-5*	2	4.50 ÷ 5.50	5 / 400	35.6 · 21.6 · 14	B	▲
GS-2I5-12*	2	4.50 ÷ 5.50	12 / 200	35.6 · 21.6 · 14	B	q
GS-2I12-12LR*	2	10.8 ÷ 13.2	12 / 150	50.8 · 25.4 · 12	D2	▲
GS-2I48-28*	2	38 ÷ 60	28 / 60	33 · 33 · 16.5	C	q
GS-3I5-3.3*	3	4.75 ÷ 5.25	3.3 / 750	33 · 33 · 16.5	C	q
GS-4I12-12*	4	10 ÷ 14	12 / 350	35.6 · 21.4 · 14	B	▲
GS-6I5-12*	6	4.65 ÷ 5.35	12 / 510	50.8 · 50.8 · 14.7	G1	▲
GS-21I5-12*	21	4.75 ÷ 5.25	12 / 1800	85.5 · 67 · 21.3	H2	▲
GS-25I24-5*	25	18 ÷ 36	5 / 5000	116 · 65 · 21.1	F1	▲
GS-30I24-12**	30	18 ÷ 36	12 / 2500	116 · 65 · 21.1	F1	▲
GS-30I24-15**	30	18 ÷ 36	15 / 2000	116 · 65 · 21.1	F1	▲

* Common feature: short-circuit protection.

** Common features: short-circuit protection, output overvolage protection, remote sense compensation, sixsided continuous shield, redundant operation.

SUBSYSTEMS MODULES (Cont'd)

DC-CD CONVERTERS FOR GENERAL PURPOSE APPLICATIONS (Cont'd)

Dual Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt / mA	Dimensions L . W . H (mm)	Package	Page/DB
GS-2I5-D5*	2	4.75 ÷ 5.25	± 5 / ± 200	50.8 . 25.4 . 12	D	q
GS-2I5-D12*	2	4.75 ÷ 5.25	± 12 / ± 100	50.8 . 25.4 . 12	D1	q
GS-31I10-D1524*	31	8.98 ÷ 13.00	15 / 2000 24/40	116 . 65 . 21.1	F2	q
Triple Output Type	**Output Power (W)**	**Input Voltage Range (V_{DC})**	**Output Volt / mA**	**Dimensions L . W . H (mm)**	**Package**	**Page/DB**
GS-1I5-5D15*	2	4.70 ÷ 5.30	+ 5 / + 20 ± 15 / ± 15	33 . 33 . 16.5	C2	q
GS-2I5-5D15*	2	4.70 ÷ 5.30	+ 5 / + 50 ± 15 / ± 70	33 . 33 . 16.5	C2	q
GS-5I24-5D15*	5	17.5 ÷ 30.00	+ 5 / + 250 ± 15 / ± 125	50.8 . 38.1 . 19	E	q

* Common feature: short-circuit protection.

** Common features: short-circuit protection, output overvolage protection, remote sense compensation, sixsided continuous shield, redundant operation.

DC-DC CONVERTERS FOR ECL APPLICATIONS (-5.2V Output)

Single Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt/mA	Dimensions L . W . H (mm)	Package	Page/DB
GS-3I5-5.2*	3	4.75 ÷ 5.25	– 5.2 / 600	33 . 33 . 16.5	C	q
GS-15I5-5.2*	15	4.65 ÷ 5.35	– 5.2 / 3000	50.8 . 50.8 . 14.7	G1	▲

* Common feature: short-circuit protection.

DC-DC CONVERTERS FOR LAN APPLICATIONS (–9V Output)

Single Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt/mA	Dimensions L . W . H (mm)	Package	Page/DB
GS-2I12-9*	2	11.28 ÷ 15.75	– 9 / 250	33 . 33 . 12.7	A	q
GS-2I12-9A*	2	9.50 ÷ 15.75	– 9 / 250	35.6 . 21.6 . 14	B	q
GS-2I5-9*	2	4.50 ÷ 5.50	– 9 / 250	35.6 . 21.6 . 14	B	q
GS-2IX-9*	2	4.50 ÷ 15.75	– 9 / 250	35.6 . 21.6 . 14	B	q

*Common feature: short circuit protection.

DC-DC CONVERTERS FOR –48V_{DC} INPUT VOLTAGES BUS

Single Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt/mA	Dimensions L • W • H (mm)	Package	Page/DB
GS-2I48-28*	2	38 ÷ 60	28 / 0.060	33 • 33 • 16.5	C	q
GS-4I48-5*	4	38 ÷ 60	5 / 0.8	33 • 33 • 16.5	C	q
GS-4I48-12*	4	38 ÷ 60	12 / 0.3	33 • 33 • 16.5	C	q
GS-5I48-5*	5	38 ÷ 60	5 / 1	50.8 • 50.8 • 14.7	G1	q
GS-5I48-12*	5	38 ÷ 60	12 / 0.42	33 • 33 • 16.5	C	▲
GS-5I48-15*	5	38 ÷ 60	15 / 0.33	33 • 33 • 16.5	C	q
GS-15I48-5*	15	38 ÷ 68	5 / 3	50.8 • 50.8 • 14.7	G1	▲
GS-20I48-5S*	20	36 ÷ 72	5 / 4	101.6 • 50.8 • 16	R2	▲
GS-T25-0500**	25	36 ÷ 72	5 / 5	116 • 65 • 21.1	F1	1029
GS-T27-0600**	27	36 ÷ 72	6 / 4.5	116 • 65 • 21.1	F1	1029
GS-T30-1200**	30	36 ÷ 72	12 / 2.5	116 • 65 • 21.1	F1	1029
GS-T30-1500**	30	36 ÷ 72	15 / 2	116 • 65 • 21.1	F1	1029
GS-T150-05/1***	150	38 ÷ 60	5 / 30	125 • 66.5 • 19	T	1037
GS-T150-05/2***	150	38 ÷ 60	5 / 30	125 • 66.5 • 34	T1	1037
GS-T300-05/1***	300	38 ÷ 60	5 / 60	135 • 85 • 21	V	▲
GS-T300-05/2***	300	38 ÷ 60	5 / 60	135 • 85 • 34	V1	▲
Dual Output Type	**Output Power (W)**	**Input Voltage Range (V_{DC})**	**Output Volt/mA**	**Dimensions L • W • H (mm)**	**Package**	**Page/DB**
GS-2I48-D5*	2	38 ÷ 60	+ 5 / + 0.2 – 5 / – 0.1	33 • 33 • 16.5	C2	▲
GS-2I48-D12*	2	38 ÷ 60	± 12 / ± 0.1A	50.8 • 38.1 • 19	E1	q

* Common features: short circuit protection.

** Common feature: short circuit protection, output overvoltage protection, remote sense compensation, sixsided continuous shield, redundant operation.

***Common features: short-circuit protection, output overvoltage protection, remote sense compensation, synchronization output, parallel operation with equal current sharing.

DC-DC CONVERTERS FOR ISDN APPLICATIONS

NT EQUIPMENT

Dual Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt/mA	Dimensions L • W • H (mm)	Package	Page/DB
GS-1I48-D540*	1	24 ÷ 70	5 / 80 40/12.5	60 • 35 • 20	S	q
GS-1I70-D540**	15	30 ÷ 115	5 / 90 40/10.5	50.8 • 50.8 • 16.5	G2	▲

*Common features: short-circuit protection.

**According to CCITT I.430 recommendation.

SWITCHING VOLTAGE REGULATORS

Type Number	Description	Dimensions L • W • H (mm)	Package	Page/DB
GS-M51212	Five Output Voltages: 5V/2A, ± 12V/0.125A, ± 12V/0.125A	101.6 • 50.8 • 16.5	Open Frame	q
GS-R1005**	5V/10A Fixed Output; V_i = 12 to 36 V	101.6 • 50.8 • 16	R	1111
GS-R1012**	12V/10A Fixed Output; V_i = 18 to 36 V	101.6 • 50.8 • 16	R	▲
GS-R400V*	5.1 to 40V/4A Adjustable Output Voltage; V_i up to 46 V	85.5 • 67 • 21.3	H	1001
GS-R400VB*	5.1V to 40V/Up to 4A Adjustable Output Voltage and Current; Syncro Module; V_i up to 46V	85.5 • 67 • 21.3	H	1001
GS-R405*	5.1V/4A Fixed Output; V_i = 9 to 46V	85.5 • 67 • 21.3	H	1001
GS-R405S*	5.1V/4A Fixed Output; V_i = 9 to 46 V;	85.5 • 67 • 21.3	H	1001
GS-R412*	12V/4A Fixed Output; V_i = 16 to 46V;	85.5 • 67 • 21.3	H	1001
GS-R415*	15V/4A Fixed Output; V_i = 19 to 46V	85.5 • 67 • 21.3	H	1001
GS-R424*	24V/4A Fixed Output; V_i = 28 to 46V	85.5 • 67 • 21.3	H	1001
GS-R400V/2	5.1 to 40V/2A Adjustable Output Voltage; Small Size		G	1007
GS-R405/2*	5V/4A Fixed Output; Small Size	50.8 • 50.8 • 14.7	G	1007
GS-R412/2*	12V/3A Fixed Output; Small Size	50.8 • 50.8 • 14.7	G	1007
GS-R415/2*	15V/3A Fixed Output; Small Size	50.8 • 50.8 • 14.7	G	1007
GS-R424/2*	24V/2A Fixed Output; Small Size	50.8 • 50.8 • 14.7	G	1007
GS-R4840N	–40V/–1A Negative Output	85.5 • 67 • 21.3	H3	▲
GS-R51212*	Triple Output Voltage; +5V/3.5A; ± 12V/0.1A (Auxiliary Isolated Outputs) Reset Output	85.5 • 67 • 21.3	H1	1017
GS-R51212S	Triple Output Voltage; +5V/4.5A; ± 12V/0.35A (Auxiliary Isolated And Externally Adjustable Outputs); Reset Output	101.6 • 50.8 • 16	R1	1021
GS-R51515S	Triple Output Voltage; +5V/4.5A; ± 15V/0.3A (Auxiliary Isolated And Externally Adjustable Outputs); Reset Output	101.6 • 50.8 • 16	R1	1021

*Common features: short-circuit protection, soft start, thermal protection, crowbar protection for the load, common input-output ground.

**Common features: short-circuit protection, softstart, remote load voltage sense, remote inhibit/enable synchronization output, parallel operation with equal current sharing, common input-output ground.

POWER CONTROLLER & MOTOR DRIVER MODULES

Type Number	Description	Dimensions L . W . H (mm)	Package	Page/DB
GS-D050	0.5A Chopped Bipolar Stepper Motor Driver	50.8 . 50.8 . 13.5	GD	905
GS-D200	2.0A Chopped Bipolar Stepper Motor Driver	85.5 . 67 . 21.3	HD	921
GS-D200S	2.5 A Chopped Bipolar Stepper Motor Driver	85.5 . 67 . 21.3	HD	921
GS-D200M	2.5 A Microstep Driver	85.5 . 67 . 21.3	HM	937
GS-C200	Programmable Intelligent Stepper Motor Controller With 25 Different Commands	85.5 . 67.5 . 22	L	865
GS-C200S	Programmable Intelligent Stepper Motor Controller With 29 Different Commands	85.5 . 67.5 . 22	L	865

POWER CONTROLLER AND MOTOR DRIVER BOARDS

Type Number	Description	Dimensions L . W . H (mm)	Package	Page/DB
GS-D250M	2.5 A Microstep Motor Driver	160 . 100 . 28	M	951
GS-D350M	5.6 A Microstep Motor Driver	160 . 100 . 48	N	959
GS-D500	70V/5A Step and Microstep Motor Driver Board	213 . 119 . 53	Q	971
GS-D550	5.6 A Chopped 2 And 5 Phases Stepper Motor Driver	160 . 100 . 48	N	981
GS-DC200	Board With a GS-C200 Controller and a GS-D200 Driver	160 . 100 . 24	O	993
GS-DC200S	Board With A GS-C200 Controller and a GS-D200S Driver	160 . 100 . 24	O	993
GS-DC200SS	Board With a GS-C200S Controller and a GS-D200S Driver	160 . 100 . 24	O	993

PROTECTION CONNECTOR

Type Number	Description	Dimensions L . W . H (mm)	Package	Page/DB
GS-P8-A	Bidirectional Data Line Protector (American Version With Female Screws 4.40 UNC)	56 . 17.5 . 25.4	P	▲
GS-P8-E	Bidirectional Data Line Protector (European Version With Female Screws M3)	56 . 17.5 . 25.4	P	▲

SERIAL ACCESS EEPROM MEMORIES

Serial access EEPROMs guarantee 1,000,000 Erase/Write cycle endurance.

With SGS-THOMSON major advantage in EEPROM, 1,000,000 Erase/Write cycle endurance, combined with 2.5V low voltage operation and memory protect features, the EEPROM has become the memory for reference data storage in many kinds of equipment. They are ideally suited for printers, telephone sets and all equipment requiring non-volatile set-up or temporary data storage.

SGS-THOMSON's EEPROMs are suitable for use with I^2C and MICROWIRE® serial bus interfaces.

I^2C Serial Bus EEPROM Range

Size	Part Number	Organisation	V_{CC} Range	Feature	Package	Page/DB
1k bit	ST24C01BX	128 x 8	4.5 to 5.5V		PDIP8	w, af
	ST24C01MX	128 x 8	4.5 to 5.5V		PSO8	w, af
	ST25C01BX	128 x 8	2.5 to 5.5V	Low Voltage	PDIP8	w, af
	ST25C01MX	128 x 8	2.5 to 5.5V	Low Voltage	PSO8	w, af
2k bit	ST24C02ABX	256 x 8	4.5 to 5.5V		PDIP8	w, af
	ST24C02AMX	256 x 8	4.5 to 5.5V		PSO8	w, af
	ST25C02ABX	256 x 8	2.5 to 5.5V	Low Voltage	PDIP8	w, af
	ST25C02AMX	256 x 8	2.5 to 5.5V	Low Voltage	PSO8	w, af
4k bit	ST24C04BX	512 x 8	4.5 to 5.5V	Write Protect	PDIP8	w, af
	ST24C04MX	512 x 8	4.5 to 5.5V	Write Protect	PSO8	w, af
	ST24C04MLX	512 x 8	4.5 to 5.5V	Write Protect	PSO14	w, af
	ST25C04BX	512 x 8	2.5 to 5.5V	Write Protect	PDIP8	w, af
	ST25C04MX	512 x 8	2.5 to 5.5V	Write Protect	PSO8	w, af
8k bit	ST24C08BX	1k x 8	4.5 to 5.5V	Write Protect	PDIP8	w, af
	ST25C08BX	1k x 8	2.5 to 5.5V	Write Protect	PDIP8	w, af
16k bit	ST24C16BX	2k x 8	4.5 to 5.5V	Write Protect	PDIP8	w, af

Note: In the Part Number X means three temperature ranges: 1 = 0 to 70 °C, 6 = –40 to 85 °C, 3 = –40 to 125 °C.

MICROWIRE Serial Bus EEPROM Range

Size	Part Number	Organisation	V_{CC} Range	Feature	Package	Page/DB
256 bit	ST93C06BX	32x8 or 16x16	4.5 to 5.5V	Dual Organisation	PDIP8	w, af
	ST93C06MX	32x8 or 16x16	4.5 to 5.5V	Dual Organisation	PSO8	w, af
1k bit	ST93C46ABX	128x8 or 64x16	4.5 to 5.5V	Dual Organisation	PDIP8	w, af
	ST93C46AMX	128x8 or 64x16	4.5 to 5.5V	Dual Organisation	PSO8	w, af
	ST93C46TMX	128x8 or 64x16	4.5 to 5.5V	90° Turn Pin Out	PSO8	w, af
	ST93CS46BX	64 x 16	4.5 to 5.5V	Write Protect	PDIP8	w, af
	ST93CS46MX	64 x 16	4.5 to 5.5V	Write Protect	PSO8	w, af
	ST93CS46MLX	64 x 16	4.5 to 5.5V	Write Protect	PSO14	w, af
	ST93CS47BX	64 x 16	2.5 to 5.5V	Low Voltage	PDIP8	w, af
	ST93CS47MX	64 x 16	2.5 to 5.5V	Low Voltage	PSO8	w, af
	ST93CS47MLX	64 x 16	2.5 to 5.5V	Low Voltage	PSO14	w, af
2k bit	ST93C56BX	128x8 or 256x16	4.5 to 5.5V	Dual Organisation	PDIP8	w, af
	ST93C56MLX	128x8 or 256x16	4.5 to 5.5V	Dual Organisation	PSO14	w, af
	ST93CS56BX	128 x 16	4.5 to 5.5V	Write Protect	PDIP8	w, af
	ST93CS56MX	128 x 16	4.5 to 5.5V	Write Protect	PSO8	w, af
	ST93CS56MLX	128 x 16	4.5 to 5.5V	Write Protect	PSO14	w, af
	ST93CS57BX	128 x 16	2.5 to 5.5V	Low Voltage	PDIP8	w, af
	ST93CS57MX	128 x 16	2.5 to 5.5V	Low Voltage	PSO8	w, af
	ST93CS57MLX	128 x 16	2.5 to 5.5V	Low Voltage	PSO14	w, af
4k bit	ST93C66BX	256x16 or 512x8	4.5 to 5.5V	Dual Organisation	PDIP8	w, af
	ST93C66MLX	256x16 or 512x8	4.5 to 5.5V	Dual Organisation	PSO14	w, af
	ST93CS66BX	256 x 16	4.5 to 5.5V	Write Protect	PDIP8	w, af
	ST93CS67BX	256 x 16	2.5 to 5.5V	Low Voltage	PDIP8	w, af

Note: In the Part Number X means three temperature ranges: 1 = 0 to 70 °C, 6 = –40 to 85 °C, 3 = –40 to 125 °C.

EPROM - ROM - FLASH MEMORIES

EPROMs are manufactured in two types, UV eraseable and OTP (One Time Programable). Three process technologies are used, NMOS 1.5 micron and CMOS 1.2 and 0.8 micron.

EPROM sizes range from 16k bits up to 4 Megabits, with a 16 Megabit device, in 0.6 micron process technology, in development.

ROMs are manufactured in a high speed CMOS process technology and feature 100ns access time. Sizes range up to 1 Megabit.

FLASH products are being introduced in a range that will extend initially up to 4 Megabit.

CMOS UV EPROM

Size	Part Number	Organisation	Speed (ns)						Feature	Page/DB
			80	100	120	150	200	250		
64k bit	TS27C64A	8k x 8					■	■		w, af
256k bit	M27C256B	32k x 8			■	■	■	■		w, af
512k bit	M27C512	64k x 8	New	New	■	■	■	■		w, af
	M27C516	32k x 16			■	■	■	■	x16 Organisation	w, af
1M bit	M27C1000	128k x 8	New	■	■	■	■	■	ROM Compatible	w, af
	M27C1001	128k x 8	New	■	■	■	■	■		w, af
	M27C1024	64k x 16			■	■	■	■	x16 Organisation	w, af
2M bit	M27C2001	256k x 8	New	■	■	■	■	■		w, af
4M bit	M27C4001	512k x 8	■	■	■	■	■		High Speed	w, af
	M27C4002	256k x 16	New	■	■	■	■		High Speed, x16	w, af

Notes:
■ = V_{CC} range ± 5%
■ = V_{CC} range ± 10%

For information on new products, contact local Sales Office.

NMOS UV EPROM

Size	Part Number	Organisation	Speed (ns)						Feature	Page/DB
			170	200	250	300	350	450		
16k bit	M2716	2k x 8					■	■		w, af
32k bit	M2732	4k x 8					■	■		w, af
64k bit	M2764A	8k x 8		■	■	■				w, af
128k bit	M27128A	16k x 8		■	■	■				w, af
256k bit	M27256	32k x 8	■	■	■	■				w, af
512k bit	M27512	64k x 8		■	■	■				w, af

Notes:
■ = V_{CC} range ± 5%
■ = V_{CC} range ± 10%

OTP ROM

Size	Part Number	Organisation	Speed (ns)						Package			Page/DB
			100	120	150	200	250	300	PDIP	PLCC	PSO	
NMOS												
64k bit	ST2764A	8k x 8					■	■	●			w, af
128k bit	ST27128A	16k x 8					■	■	●			w, af
256k bit	ST27256	32k x 8					■	■	●			w, af
CMOS												
256k bit	M27C256B	32k x 8			■	■			●	●	New	w, af
512k bit	M27C512	64k x 8							●	●	New	w, af
	M27C516	32k x 16			■	●				●		w, af
1M bit	M27C1001	128k x 8			■	■			New	New		w, af
	M27C1024	64k x 16			■	■			New	New		w, af
4M bit	M27C4002	256k x 16	■			■				New		w, af

Notes:
● = Available
= V_{CC} range ± 5%
■ = V_{CC} range ± 10%

For information on new products, contact local Sales Office.

MASK ROM

Size	Part Number	Organisation	Speed	Package	Page/DB
				PDIP	
512k bit	M23C512	64k x 8	100ns	●	w, af
1M bit	M23C1000	128k x 8	100ns	●	w, af
	M23C1001	128k x 8	100ns	●	w, af

Note: Mask program ROMs require the memory content to be provided with the purchase contract. A mask charge applies, also a minimum quantity purchase.

FLASH

Size	Part Number	Organisation	Speed	Package				Page/DB
				PDIP	PLCC	PSO	PSSO	
256k bit	M28F256	32k x 8	100-150ns	●	●	New		w, af
512k bit	M28F512	64k x 8	100-150ns	New	New	New	New	w, af
1M bit	M28F1001	128k x 8	100-150ns	New	New	New	New	w, af
	M28F1024	64k x 16	100-150ns		New			w, af

For information on new products, contact local Sales Office.

STATIC RAM

Static RAM products cover three ranges. They are manufactured in advanced CMOS process technologies down to 0.7 micron.

The Fast SRAM range is suitable for high speed computer applications, for example data cache memory.

The Specialty SRAM range consists of two families, cache TAGRAM™ for implementing fast computer cache memory systems and fast BiPORT™ FIFOs for inter-device communication.

The Non-Volatile RAM range, ZEROPOWER™ and TIMEKEEPER™, are specially designed SRAM devices with very low standby power consumption. They implement on one chip an SRAM together with a power supply voltage detector and switch. They are packaged in plastic dual-in-line packages with a "top-hat" which carries a lithium back-up battery. The TIMEKEEPER chip also integrates a very low power consumption oscillator and clock, the "top-hat" includes both a battery and a crystal.

FAST SRAM

Size	Part Number	Speed (ns)	Organisation	Feature	Package
4k bit	IMS1203*	25, 35, 45	4k x 1	Separate I/O	PSDIP18
	IMS1223*	25, 35, 45	1k x 4	Common I/O	PSDIP18
16k bit	IMS1403*	25, 35, 45	16k x 1	Separate I/O	PSDIP20
	IMS1423*	25, 35, 45	4k x 4	Common I/O	PSDIP20
64k bit	IMS1600*	25, 35, 45	64k x 1	Separate I/O	PSDIP22
	M621064	10, 12, 15	64k x 1	Separate I/O	PSOJ24
	IMS1620*	25, 35, 45	16k x 4	Common I/O	PSDIP22, PSOJ24
	IMS1624*	25, 35, 45	16k x 4	Output Enable	PSDIP24, PSOJ24
	IMS1625*	20, 25	16k x 4	Common I/O	PSDIP22
	M624016	10, 12, 15	16k x 4	Common I/O	PSOJ24
	IMS1629*	20, 25	16k x 4	Output Enable	PSDIP24
	IMS1635*	20, 25, 35	8k x 8	Common I/O	PSDIP28
	M628008	10, 12, 15	8k x 8	Output Enable	PSOJ28
256k bit	IMS1800*	25, 35, 45	256k x 1	Separate I/O	PSDIP24, PSOJ24
	M621256	12, 15, 20	256k x 1	Separate I/O	PSDIP24, PSOJ24
	IMS1820*	25, 35, 45	64k x 4	Common I/O	PSDIP24, PSOJ24
	IMS1824*	25, 35, 45	64k x 4	Output Enable	PSOJ28
	M624064	12, 15, 20	64k x 4	Common I/O	PSDIP24, PSOJ24
	M624065	12, 15, 20	64k x 4	Output Enable	PSDIP28, PSOJ28
	IMS1830	25, 35, 45	32k x 8	Output Enable	PSDIP28
	M628032	12, 15, 20	32k x 8	Output Enable	PSDIP28, PSOJ28
	M629032	10, 12, 15	32k x 9	Output Enable	PSOJ32
1M bit	M621100	17, 20, 25	1M x 1	Separate I/O	PSOJ28
	M624256	17, 20, 25	256k x 4	Common I/O	PSOJ28
	M624257	17, 20, 25	256k x 4	Output Enable	PSOJ28
	M628128	17, 20, 25	128k x 8	Output Enable	PSDIP32, PSOJ32
	M629128	17, 20, 25	128k x 9	Output Enable	PSOJ32

Note: * Not for new designs

BiPORT FIFO

Organisation	Part Number	Speed (ns)	Feature	Package
1k x 5 bit	MK4505M	15, 20, 25	Master	PSDIP24
	MK4505S	15, 20, 25	Slave	PSDIP20
512 x 9 bit	MK4501*	65, 80, 100, 120, 150, 200		PDIP28, PLCC32
	MK45H01, 11	25, 35, 50, 65, 120	Fast	PDIP28, PLCC32, PSDIP28
1k x 9 bit	MK45H02, 12	25, 35, 50, 65, 120	Fast	PDIP28, PLCC32, PSDIP28
2k x 9 bit	MK4503*	65, 80, 100, 120, 150, 200		PDIP28
	MK45H03, 13	25, 35, 50, 65, 120	Fast	PDIP28, PLCC32, PSDIP28
4k x 9 bit	MK45H04, 14	25, 35, 50, 65, 120	Fast	PDIP28, PLCC32, PSDIP28
8k x 9 bit	MK45H08	25, 35, 50, 65, 120	Fast	PDIP28

Note: * Not for new designs

CACHE MEMORIES

Organisation	Part Number	Speed (ns)	Feature	Package
4k x 4 bit	MK41H80*	20, 22, 25, 35	TAGRAM	PSDIP22
	MK41S80	10, 12, 15, 20, 25	Very Fast TAGRAM	PSDIP22, PSOJ24
8k x 8 bit	MK48S74	20, 25, 35	TAGRAM	PSDIP28, PSOJ28
	MK48S80	17, 20, 25	Very Fast TAGRAM	PSDIP28, PSOJ28
2k x 20 bit	MK4202	17, 20, 25	20 bit wide TAGRAM	PLCC68
4k x 10 bit	MK45180	17, 20	SnoopTAG	PLCC68
32k x 9 bit	MK62486	14, 19, 25	BRAM	PLCC44
	MK62940	14, 19, 25	BRAM	PLCC44

Note: * Not for new designs

ZEROPOWER

Size	Part Number	Organisation	Speed (ns)	Feature	Package
16k bit	MK48C02A, 12A	2k x 8	150, 200, 250	External Battery	PDIP28, PLCC32
	MK48Z02, 12	2k x 8	120, 150, 200, 250		PHDIP24 Battery Top Hat
	MKI48Z02, 12	2k x 8	150, 200, 250	–40 to 85 °C	PHDIP24 Battery Top Hat
64k bit	MK48Z08, 18	8k x 8	100		PHDIP28 Battery Top Hat
	MK48Z09, 19	8k x 8	100	Power Fail Interrupt	PHDIP28 Battery Top Hat
	MKI48Z18	8k x 8	100	–40 to 85 °C	PHDIP28 Battery Top Hat
256k bit	MK48Z30, 30A	32k x 8	70, 120	10 yrs Life 25 °C	PHDIP28 Battery Top Hat
	MK48Z32, 32A	32k x 8	70, 120	10 yrs Life 0-70 °C	PHDIP28 Battery Top Hat

TIMEKEEPER

Size	Part Number	Organisation	Speed (ns)	Feature	Package
256 bit	MK41T56	64 x 8	Serial I/O	I^2C Bus	PSDIP8
	MK48T85	64 x 8		External Battery	PLCC28
	MK48T87	64 x 8		Real Time Clock	PHDIP24 Battery Top Hat
	MK48T87A	64 x 8		Real Time Clock, RAM Clear	PHDIP24 Battery Top Hat
16k bit	MK48T02, 12	2k x 8	150, 200, 250	Software Calibration	PHDIP24 Battery Top Hat
64k bit	MK48T08, 18	8k x 8	100, 150	Software Calibration	PHDIP28 Battery Top Hat

DATASHEETS
INTEGRATED CIRCUITS

ESM1600B

QUAD COMPARATOR INTERFACE CIRCUIT

- MINIMUM HYSTERESIS VOLTAGE AT EACH INPUT : 0.3 V
- OUTPUT CURRENT : 15 mA
- LARGE SUPPLY VOLTAGE RANGE : + 10 V to + 35 V
- INTERNAL THERMAL PROTECTION
- INPUT AND OUTPUT CLAMPING PROTECTION DIODES.

The ESM1600B can operate in a wide supply voltage range (standard operational amplifier ± 15 V supply or single + 12 V or + 24 V supplies used in industrial electronic sets).

Moreover, internal thermal protection circuitry cuts out the output current of the four comparators when power dissipation becomes excessive.

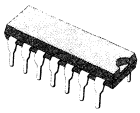
DESCRIPTION

The ESM1600B is a quadruple comparator intented to provide an interface between signal processing and transmitting lines in very noisy industrial surroundings.

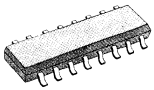
Output of each comparator, used as line driver, supplies a constant current (PNP output stage) and is specially well protected against powerful overvoltages. The open collector output circuit allows the connection of several comparators to a single transmitting line.

The ESM1600B can operate as receiver on a line transmitting noisy high-voltage signals. Hysteresis effect, internally implemented on inputs of each comparator provides an excellent noise immunity. In addition, each input is also protected against overvoltages.

DIP-14/2
(Plastic)



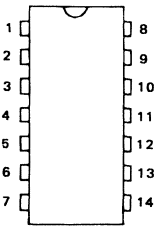
SO16J



ORDER CODES : ESM1600B (DIP-14)
ESM1600BFP (SO16J)

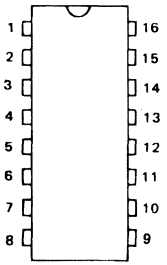
PIN CONNECTIONS (top view)

DIP-14



1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - Output 4
12 - Non-inverting input 4
13 - Inverting input 4
14 - V_{CC}

SO16J

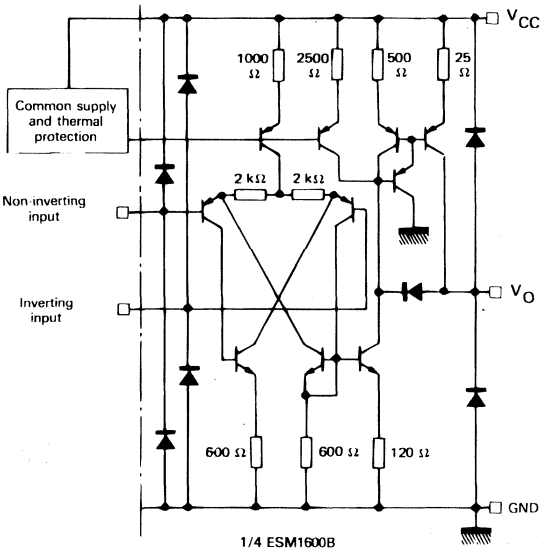


1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - N.C.
9 - N.C.
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - Output 4
14 - Non-inverting input 4
15 - Inverting input 4
16 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	45	V
V_{ID}	Differential Input Voltage	45	V
V_I	Input Voltage	– 0.7 to + 45	V
$I_{O\ (max)}$	Output Current	Internally Limited	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{op}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

SCHEMATIC DIAGRAM



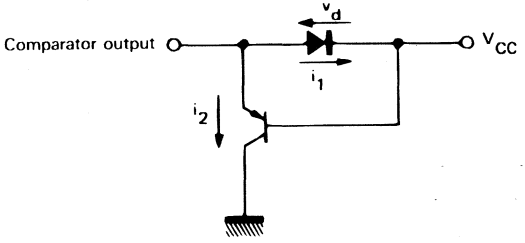
1/4 ESM1600B

ELECTRICAL CHARACTERISTICS V_{CC} = + 35 V, - 25 °C ≤ T_{amb} ≤ + 85 °C (unless otherwise specified)

Symbol	Parameter	Value			Unit	Fig.
		Min.	Typ.	Max.		
V_I^+ V_I^-	Input Voltage Range - Note 1 Non-inverting Input Inverting Input	 0 2	 – –	 33 33	V	–
V_C	Input Control Voltage (2 V < V_{CM} < 33 V) - Note 2	150	–	500	mV	1
I_{IB}	Input Bias Current - Note 3	–	1	5	µA	–
I_{SC}	Short-circuit Output Current V_{CC} = + 10 to + 35 V	 6	 –	 25	mA	2
V_{CC}–V_O	Output Saturation Voltage (high level) - (I_O = – 10 mA)	–	1	1.5	V	3
I_{OL} I_{OH}	Output Off-state Current (V_I^+ = 2 V, V_I^- = 33 V)	–	1	5	µA	4
I_{CC}	Supply Current R_L = ∞ for the 4 Comparators R_L Common for the 4 Comparators	 – –	 3 9	 5 12	mA	5
S_{VO}	Output Slew-rate (R_L = 3 kΩ, T_{amb} = + 25 °C)	1	–	–	V/µs	–
V_F	Input Protective Diode Forward Voltage (I = 20 mA, T_{amb} = + 25 °C)	–	–	1.5	V	–
–	Energy of Pulses against which Circuit Output is Protected. (T_{amb} = + 25 °C) - Note 4	–	–	20	mJ	–
–	Pulsed Current Applied to Protective Output Diodes (T_{amb} = + 25 °C) - Note 5	–	0.4	–	A	6

Notes :

1. When negative input is biased between 0 and 2 volts output is always low.
2. Comparator hysteresis voltage on positive input on the one hand and negative input on the other hand equals sum of input control voltages V_{C1} + V_{C2} or V_{C3} + V_{C4}.
3. Input current flows out of the circuit owing to PNP input stage. This current is constant and independent of output level. So no load change is transmitted to inputs.
4. By definition, a circuit is immunized against powerful signals when no durable characteristic change occurs after the application of these signals and when the circuit has not been destroyed.
   In industrial surroundings, parasitic signals contain usually high voltage (over 200 V) AC harmonics having variable impedance of 500 Ω to 10 KΩ.
   The power dissipation of these signals is divided between clamping diodes and the V_{CC}. Simulation is used to determine the maximum energy level. The injected current value cannot in any case exceed 3 A.
5. Output protective diodes are tested individually by means of positive and negative discharge voltages of a capacitor. The negative discharge control occurs through a single diode. During positive discharge, due to the properties of integration, a grounded collector PNP transistor appears in parallel with the clamping diode connected to V_{CC}. A part of the current flows through this transistor, V_{CE} being greater than V_{CC}. If T is the total discharge duration, energy dissipated in the circuit is :



$$W = \int_0^T [\, i_1 \cdot vd + i_2 \,(VCC + vd)\,]\, dt$$

For a certain injected current, the lower the current I_2, that is to say the lower the PNP current gain the smaller the energy is dissipated in the circuit. Topology and technological processes have been chosen to shorten this current gain.

Figure 1: Input bias current

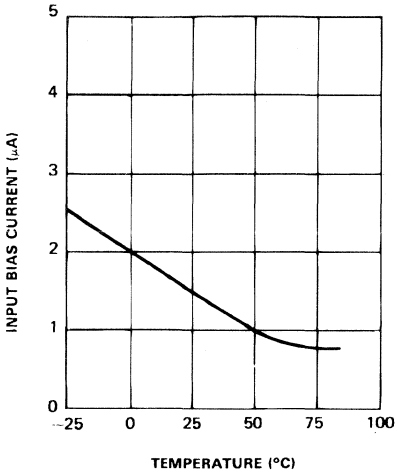


Figure 2: Output saturation voltage

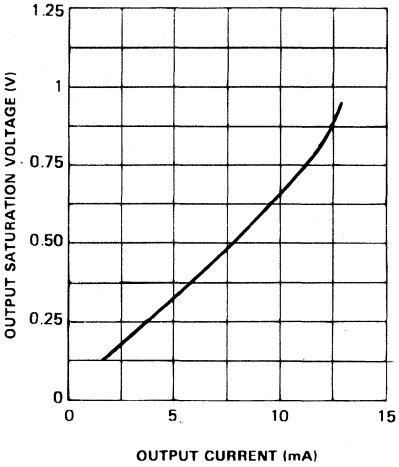


Figure 3: Output saturation voltage

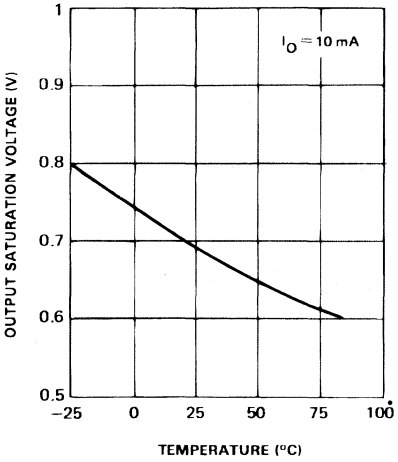
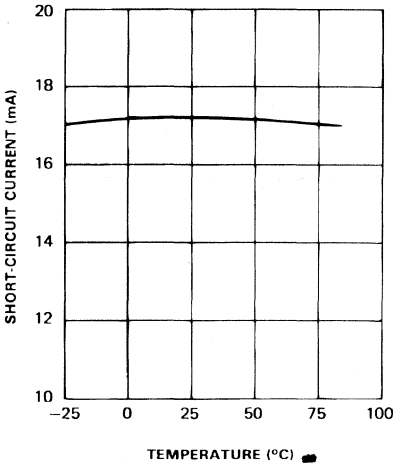


Figure 4: Short circuit corrent



TYPICAL APPLICATIONS

Figure 5 : Conversion of DTL, TTL, MOS Signals on a Transmitting Line.

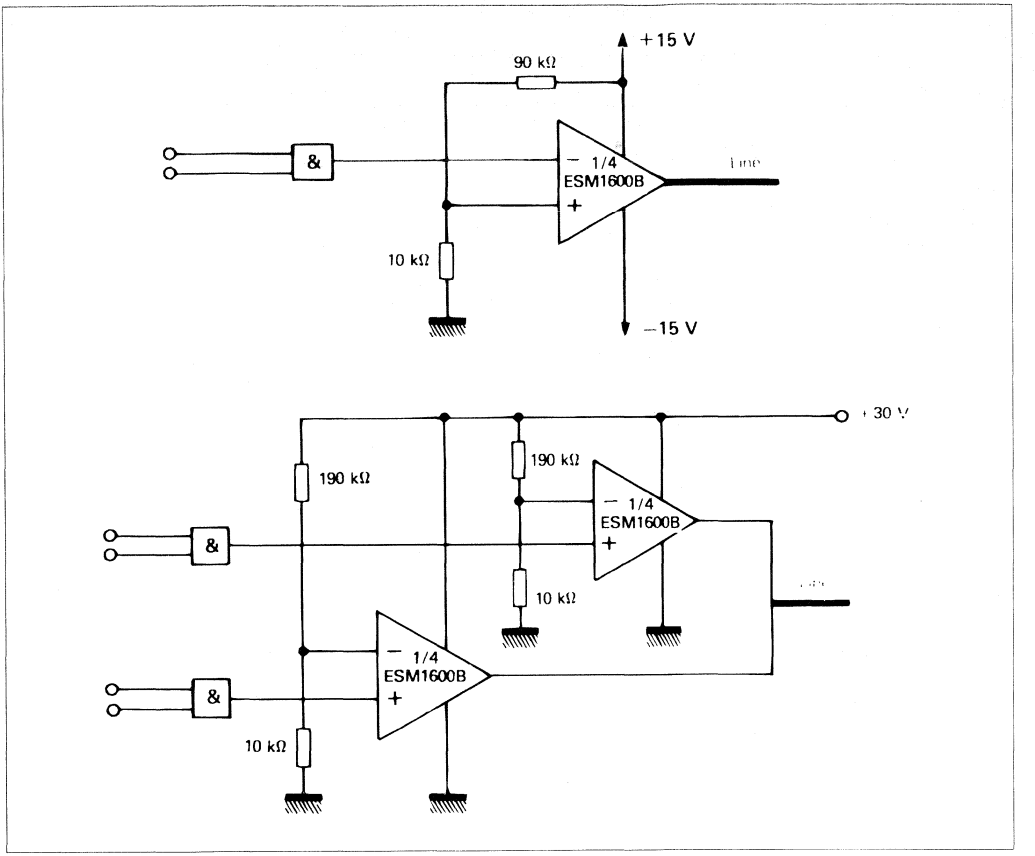
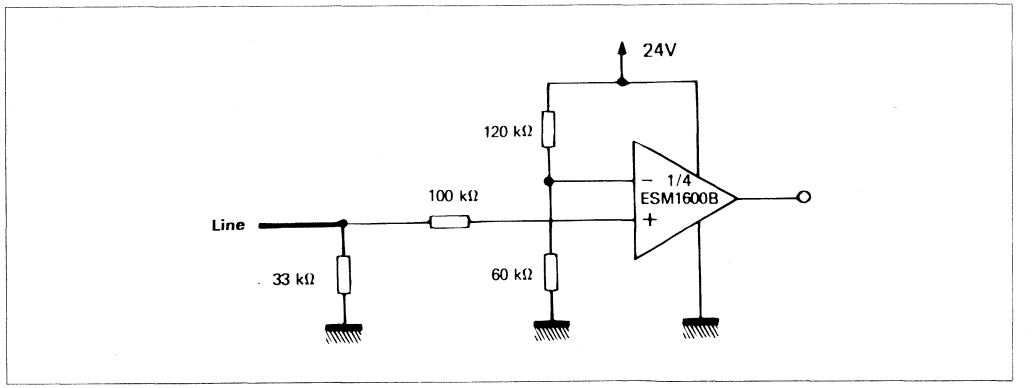


Figure 6 : Reception of Highly Noisy Signals.



TEST CIRCUIT

Figure 7.

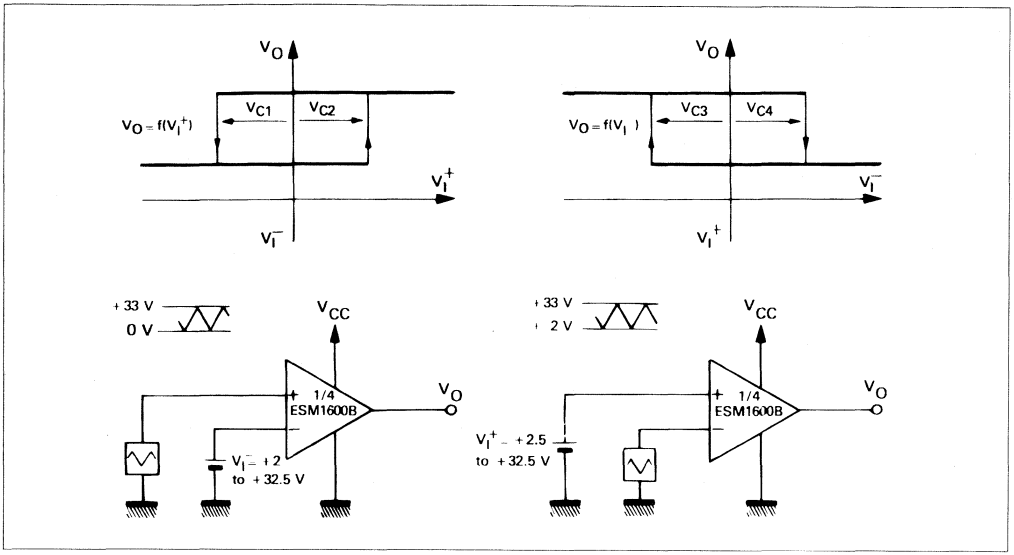


Figure 8.

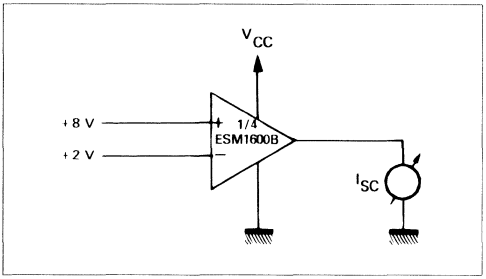


Figure 9.

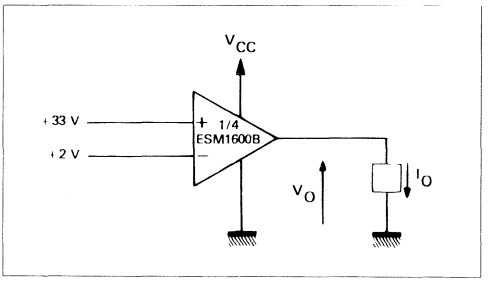


Figure 10.

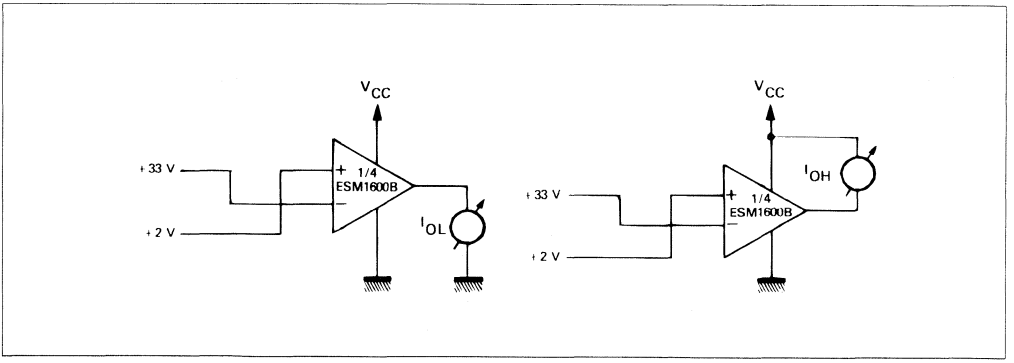


Figure 11.

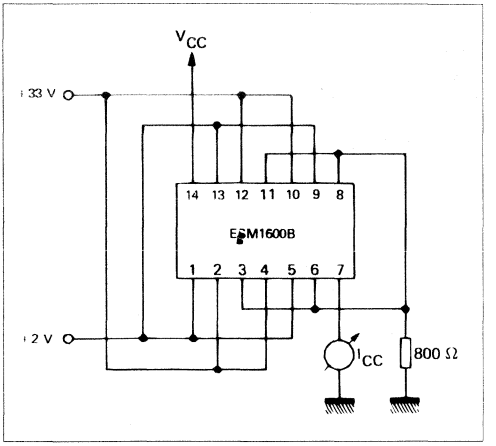


Figure 12.

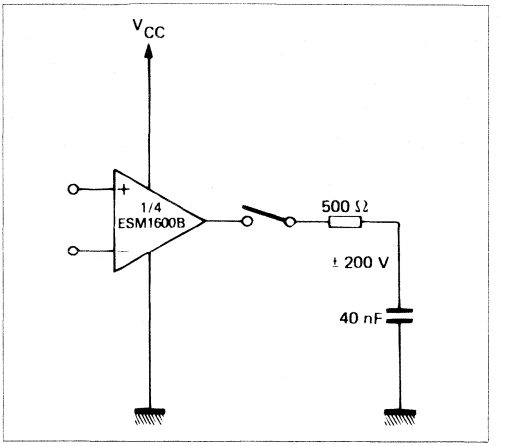
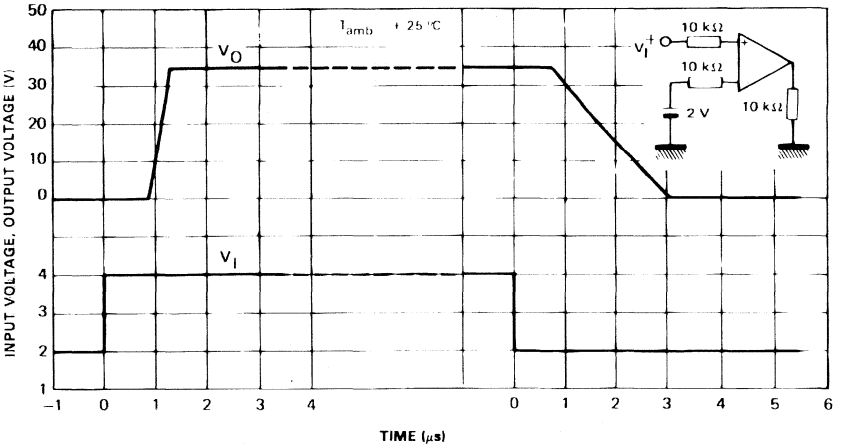


Figure 13 : Response Time.



SGS-THOMSON MICROELECTRONICS

ESM1602B

QUAD COMPARATOR INTERFACE CIRCUIT

- MINIMUM HYSTERESIS VOLTAGE AT EACH INPUT : 0.3 V
- OUTPUT CURRENT : 15 mA
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 35 V
- INTERNAL THERMAL PROTECTION
- INPUT AND OUTPUT CLAMPING PROTECTION DIODES

DESCRIPTION

The ESM1602B is a quadruple comparator intended to provide an interface between signal processing and transmitting lines in very noisy industrial surroundings.

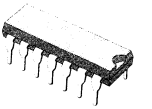
Output of each comparator, used as line driver, is well protected against powerful overvoltages. The output is a common emitter stage including complementary transistors. This arrangement ensures that no simultaneous conduction of high and low stages can occur in the presence of noise signals. Short-circuit currents toward V_{CC} and ground are limited to the same value.

The ESM1602B can operate as receiver on a line transmitting noisy high-voltage signals. It has the same input stage as ESM1600B. Hysteresis effect, internally implemented on inputs of each comparator provides an excellent noise immunity. In addition each input is also protected against overvoltages.

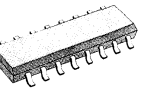
The ESM1602B can operate in a wide supply voltage range (standard operational amplifier ± 15 V supply or single + 12 V or + 24 V supplies used in industrial electronic sets).

Moreover, internal thermal protection circuitry cuts out the output current of the four comparators when power dissipation becomes excessive.

DIP-14/2
(Plastic)



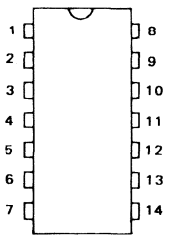
SO-16J



ORDER CODES : ESM1602B (DIP-14)
ESM1602BFP (SO-16J)

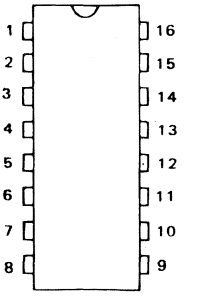
PIN CONNECTION (top view)

DIP-14



1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - Output 4
12 - Non-inverting input 4
13 - Inverting input 4
14 - V_{CC}

SO-16J

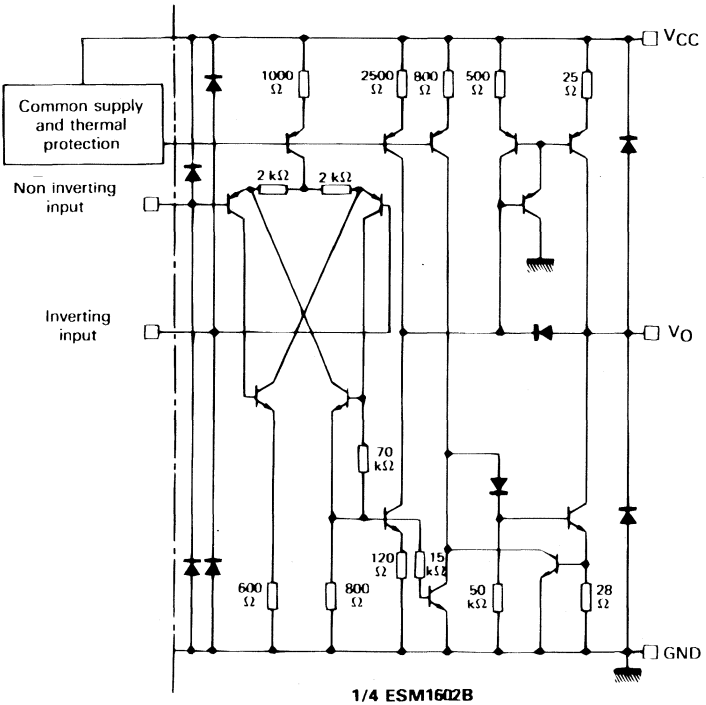


1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - N.C.
9 - N.C.
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - Output 4
14 - Non inverting input 4
15 - inverting input 4
16 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	45	V
V_{ID}	Differential Input Voltage	45	V
V_I	Input Voltage	– 0.7 to + 45	V
$I_{O(max)}$	Output Current	Internally Limited	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{op}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

SCHEMATIC DIAGRAM

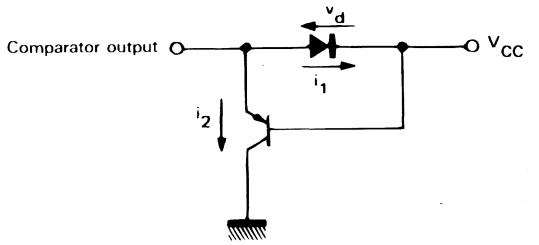


1/4 ESM1602B

ELECTRICAL CHARACTERISTICS V_{CC} = + 35 V, − 25 °C ≤ T_{amb} ≤ + 85 °C
(unless otherwise specified)

Symbol	Parameter	Value			Unit	Fig.
		Min.	Typ.	Max.		
V_I^+ V_I^-	Input Voltage Range - Note 1 Non-inverting Input Inverting Input	 0 2	 – –	 33 33	V	–
V_C	Input Control Voltage (2 V < V_{CM} < 33 V) - Note 2	150	–	500	mV	8
I_{IB}	Input Bias Current - Note 3	–	1	5	µA	–
I_{SC}	Short-circuit Output Current V_{CC} = + 10 to + 35 V	 6	 –	 25	mA	 9
V_{CC}-V_O	Output Saturation Voltage (high level) - (I_O = − 10 mA)	–	1	1.5	V	11
V_O	Output Saturation Voltage (low level) - (I_O = + 10 mA)	–	1	1.6	V	12
I_{CC}	Supply Current R_L = ∞ for the 4 Comparators R_L Common for the Comparators	 – –	 4 10	 6 13	mA	 13,14
S_{VO}	Output Slew-rate (R_L = 3 KΩ, T_{amb} = + 25 °C)	1	–	–	V/µs	–
V_F	Input Protective Diode Forward Voltage (I = 20 mA, T_{amb} = + 25 °C)	–	–	1.5	V	–
–	Energy of Pulses against which Circuit Output is Protected (T_{amb} = + 25 °C) - Note 4	 –	 –	 20	mJ	–
–	Pulsed Current Applied to Protective Output Diodes (T_{amb} = + 25 °C) - Note 5	 –	 0.4	 –	A	15

Notes : 1. When negative input is biased between 0 and 2 volts output is always low.
2. Comparator hysteresis voltage on positive input on the one hand and negative input on the other hand equals sum of input control voltages V_{C1} + V_{C2} or V_{C3} + V_{C4}.
3. Input current flows out of the circuit owing to PNP input stage. This current is constant and independent of output level. So no load change is transmitted to inputs.
4. By definition, a circuit is immunized against powerful signals when no durable characteristic change occurs after the application of these signals and when the circuit has not been destroyed.
In industrial surroundings, parasitic signals contain usually high voltage (over 200 V) AC harmonics having variable impedance of 500 Ω to 10 KΩ.
The power dissipation of these signals is divided between clamping diodes and the V_{CC}. Simulation is used to determine the maximum energy level. The injected current value cannot in any case exceed 3 A.
5. Output protective diodes are individually by means of positive and negative discharge voltages of a capacitor. The negative discharge control occurs through a single diode. During positive discharge, due to the properties of integration, a grounded collector PNP transistor appears in parallel with the clamping diode connected to V_{CC}. A part of the current flows through this transistor, V_{CE} being greater than V_{CC}. If T is the total discharge duration, energy dissipated in the circuit is :



$$W = \int_0^T [\, i_1 \cdot v_d + i_2 (V_{CC} + v_d) \,] \, dt$$

For a certain injected current, the lower the current I_{2}, that is to say the lower the PNP current gain the smaller the energy is dissipated in the circuit. Topology and technological processes have been chosen to shorten this current gain.

Fig. 1 – INPUT BIAS CURRENT.

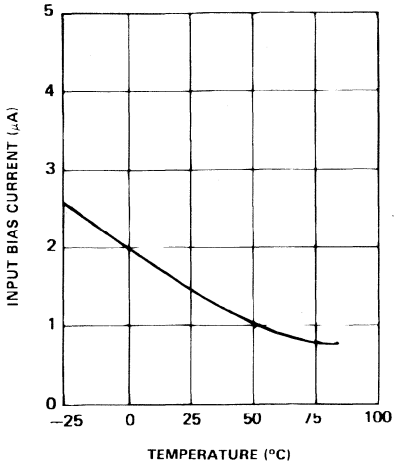


Fig. 2 – OUTPUT SATURATION VOLTAGE.

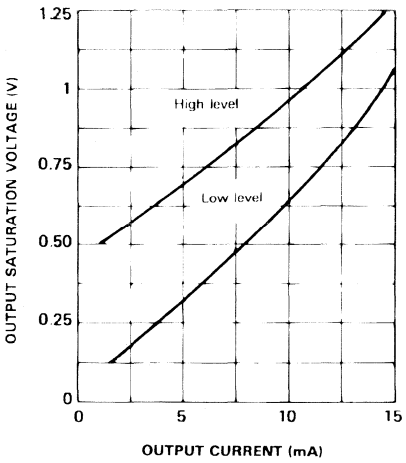


Fig. 3 – OUTPUT SATURATION VOLTAGE.

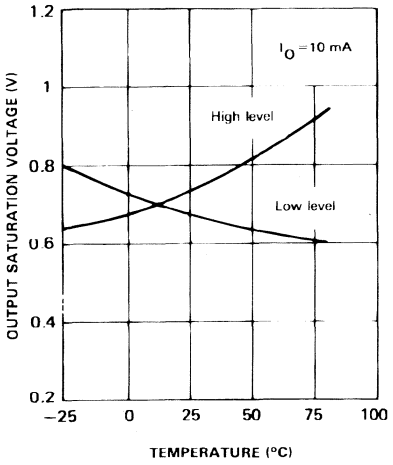
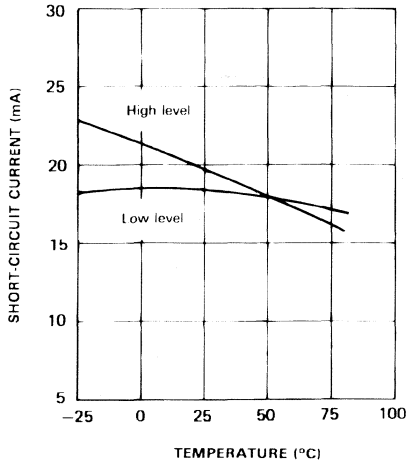


Fig. 4 – SHORT CIRCUIT CURRENT.



TYPICAL APPLICATIONS

Figure 5 : Conversion of DTL, TTL, MOS Signals on a Transmitting Line.

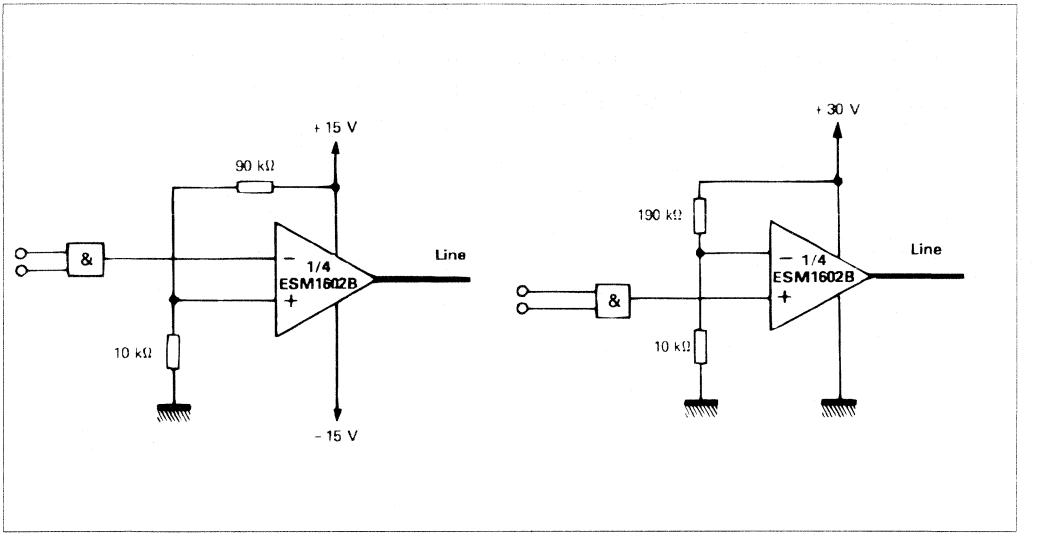


Figure 6 : Reception of Highly Noisy Signals.

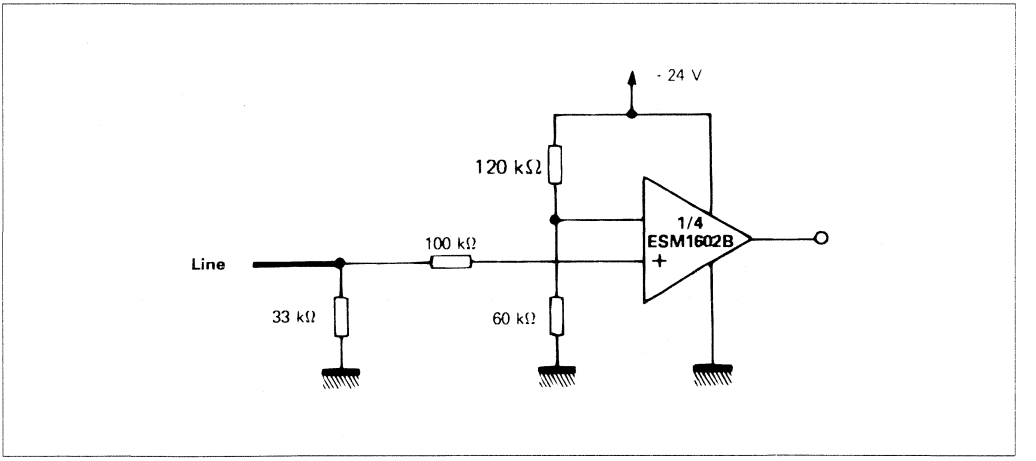
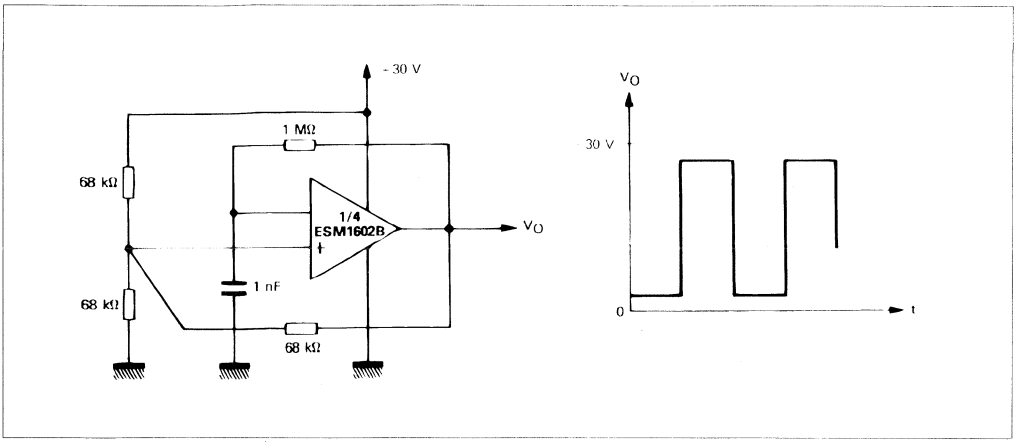


Figure 7 : Free-running Square Wave Oscillator.



TEST CIRCUITS

Figure 8.

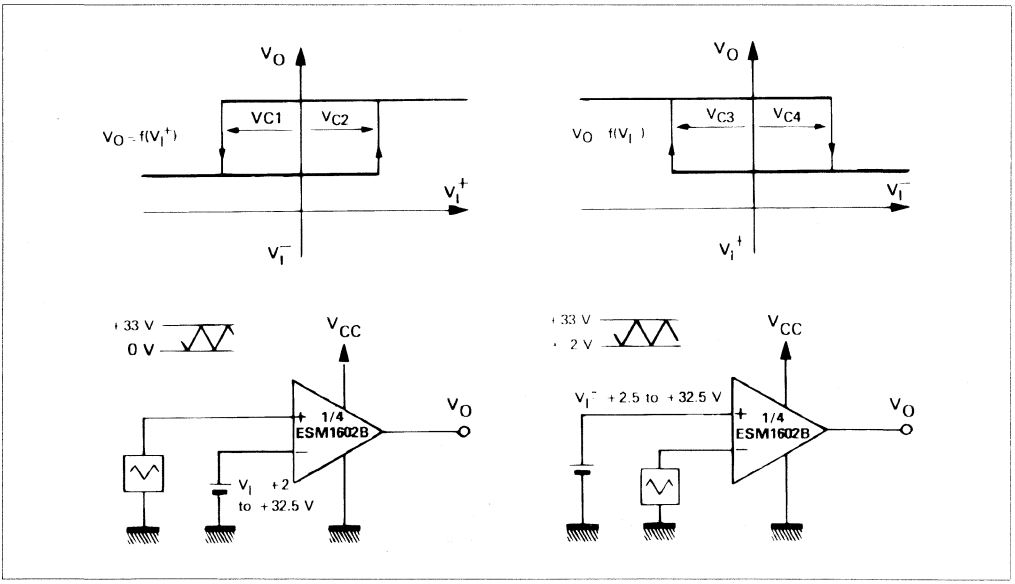


Figure 9.

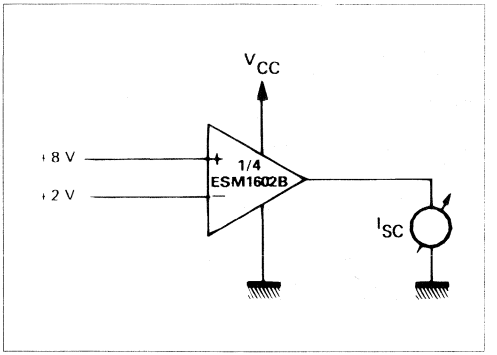


Figure 10.

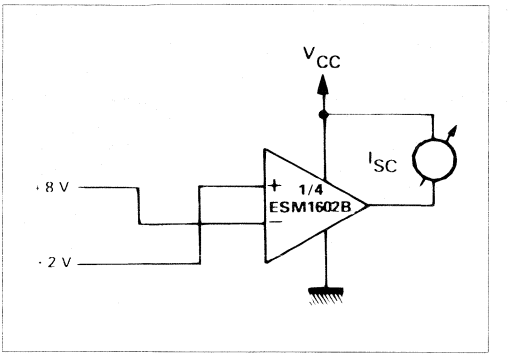


Figure 11.

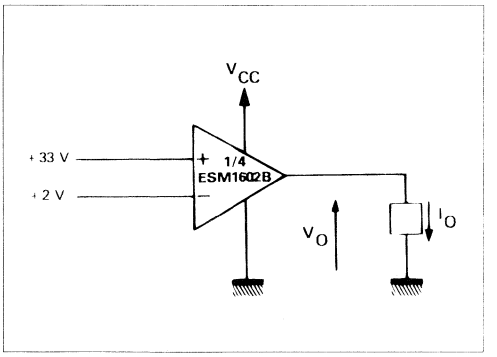


Figure 12.

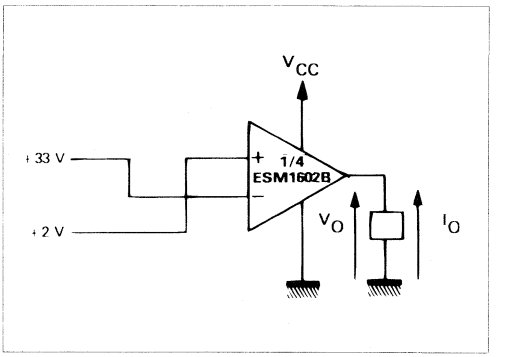


Figure 13.

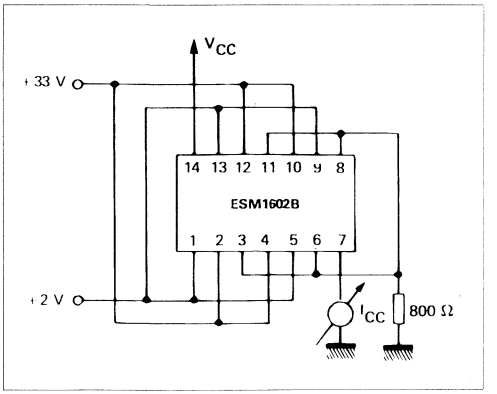


Figure 14.

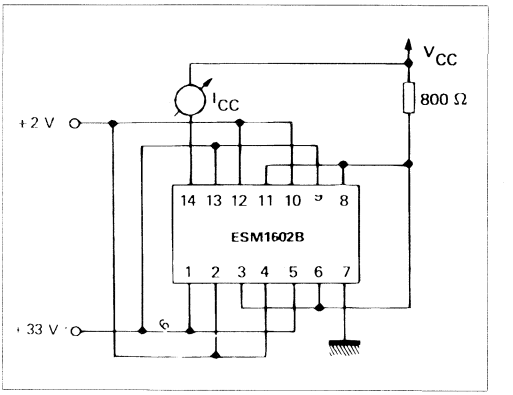


Figure 15.

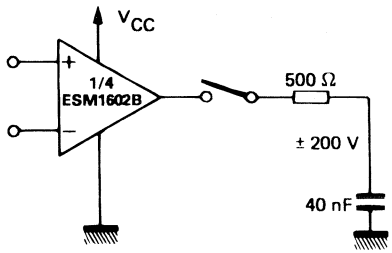
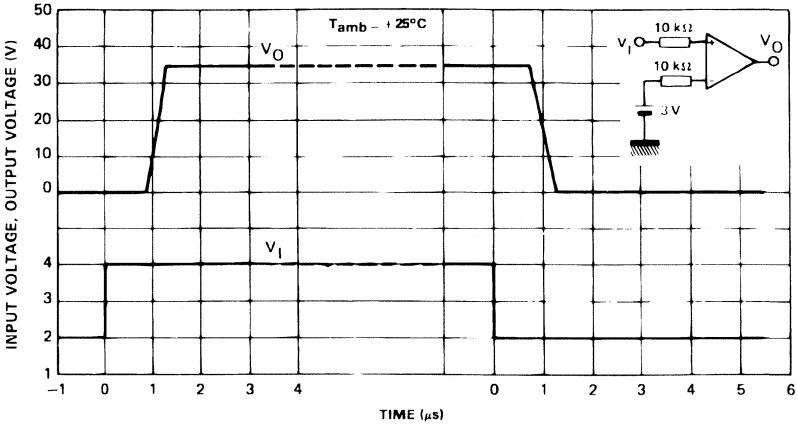


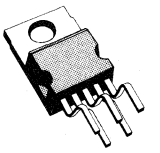
Figure 16 : Response Time.



4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A peak)
- HIGH CURRENT GAIN (10.000 typ.)
- OPERATION UP TO ± 20 V
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30 V/ µs)

The L149 is a general purpose power booster in Pentawatt® package consisting of a quasi-complementary darlington output stage with the associated biasing system an inhibit facility.
The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.



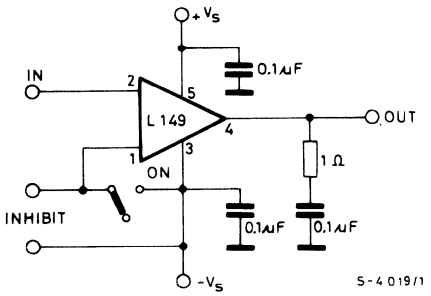
Pentawatt®

ORDER CODE : L149V

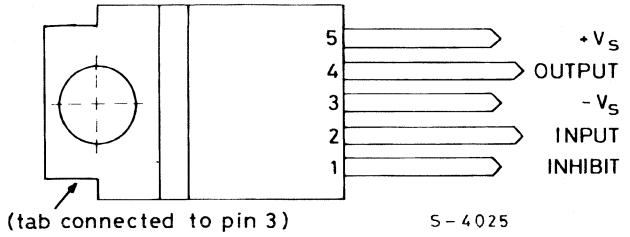
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 20	V
V_i	Input Voltage		V_s
$V_5 - V_4$	Upper Power Transistor V_{CE}	40	V
$V_4 - V_3$	Lower Power Transistor V_{CE}	40	V
I_o	DC Output Current	3	A
I_o	Peak Output Current (internally limited)	4	A
V_{INH}	Input Inhibit Voltage	$- V_s + 5$ $- V_s - 1.5$	V V
P_{tot}	Power Dissipation at T_{case} = 75 °C	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

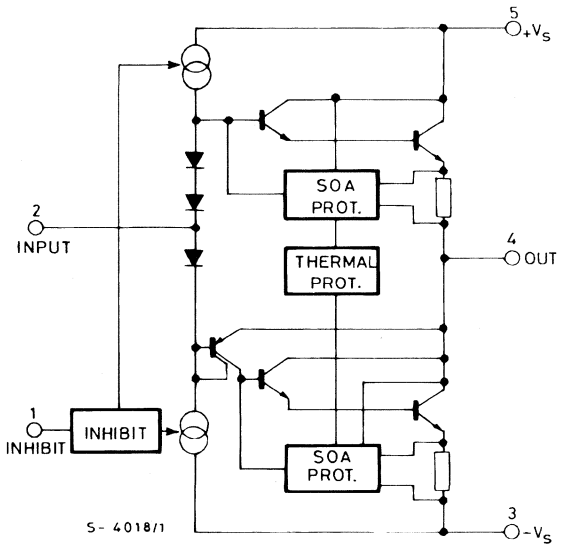
TEST CIRCUIT



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_S = ± 16V)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage					± 20	V
I_d	Quiescent drain current	V_S = ± 16V			30		mA
I_{in}	Input current	V_S = ± 16V	V_i = OV		200	400	µA
h_{FE}	DC current gain	V_S = ± 16V	I_o = 3A	6000	10000		–
G_v	Voltage gain	V_S = ± 16V	I_o = 1.5A		1		–
V_{CEsat}	Saturation voltage (for each transistor)	I_o = 3A				3.5	V
V_{os}	Input offset voltage	V_S = ± 16V				0.3	V
V_{INH}	Inhibit input voltage (pins 1-3)	ON condition				± 0.3	V
		OFF condition		± 1.8			
R_{INH}	Inhibit input resistance				2.0		KΩ
SR	Slew rate				30		V/ µs
B	Power bandwidth	V_o = ± 10V, d = 1 %, R_L = 8Ω			200		KHz

APPLICATION INFORMATION

Figure 1 : High slew-rate power operational amplifier (SR = 13V/ µs).

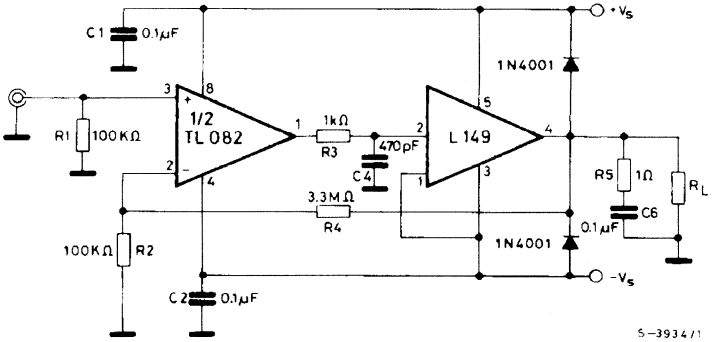


Figure 2 : Maximum saturation voltage vs. output current.

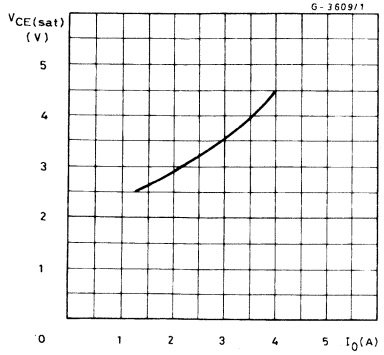


Figure 3 : Current limiting characteristics..

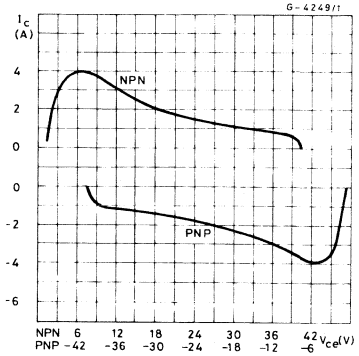


Figure 4 : Supply voltage rejection vs. frequency.

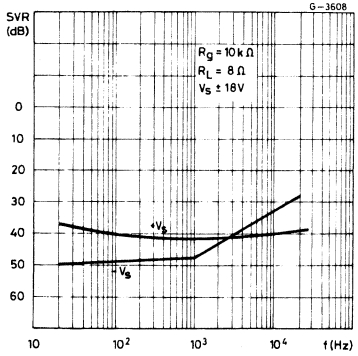


Figure 5 : Distortion vs. output power (f = 1 KHz).

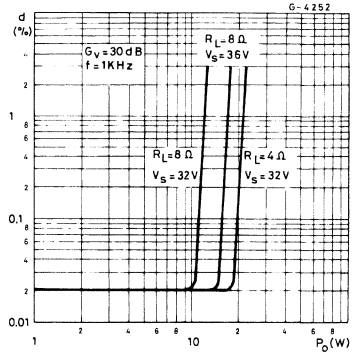


Figure 6 : Distortion vs. output power (f = 10 KHz).

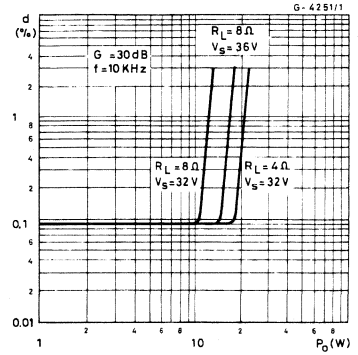
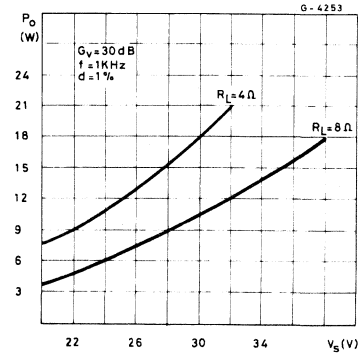


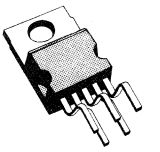
Figure 7 : Output power vs. supply voltage.



3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt®

ORDER CODE : L165V

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_S	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

APPLICATION CIRCUITS

Figure 1 : Gain > 10.

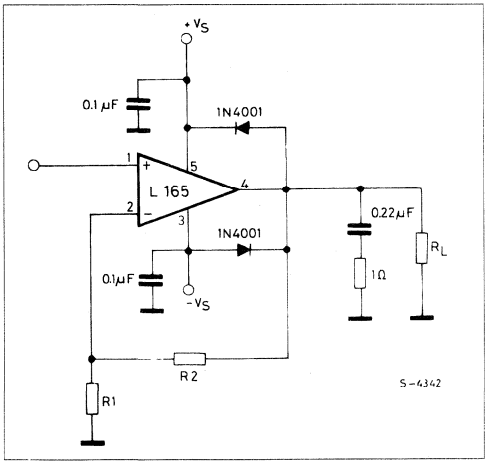
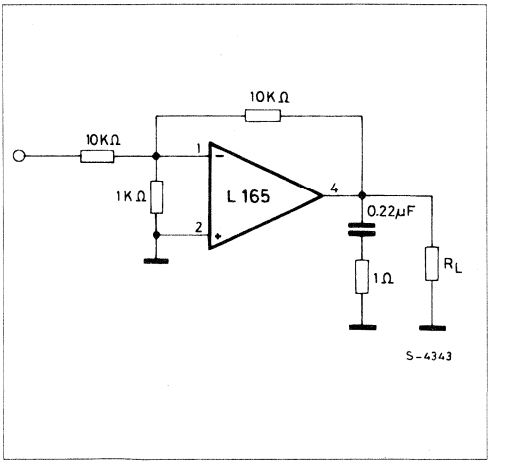
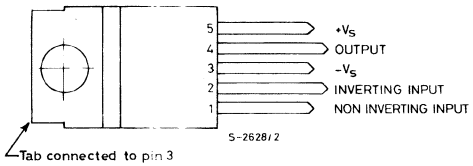


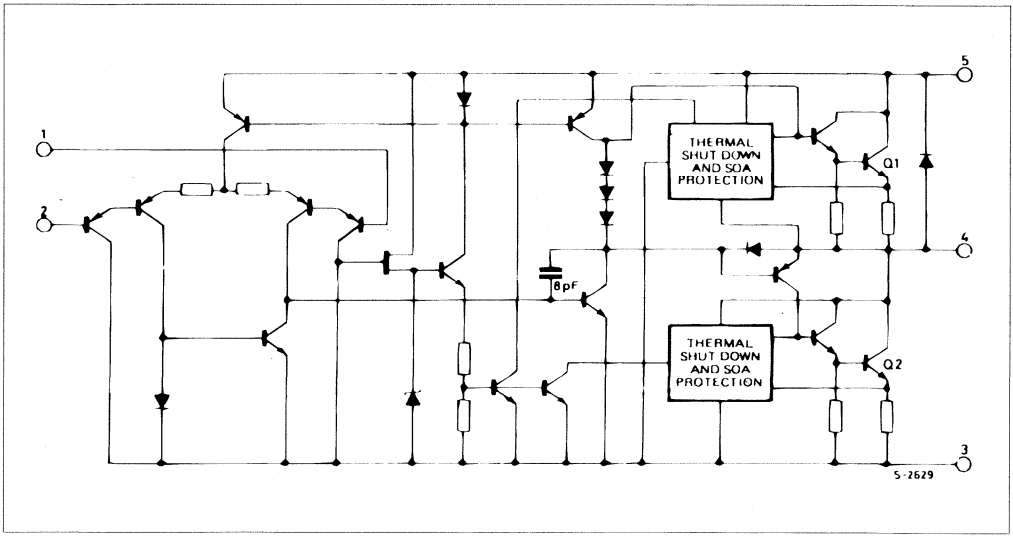
Figure 2 : Unity gain configuration.



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = ± 15 V, T_j = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 18	V
I_d	Quiescent Drain Current	V_s = ± 18 V		40	60	mA
I_b	Input Bias Current			0.2	1	µA
V_{os}	Input Offset Voltage			± 2	± 10	mV
I_{os}	Input Offset Current			± 20	± 200	nA
SR	Slew-rate	G_v = 10		8		V/µs
		G_v = 1 (°)		6		
V_o	Output Voltage Swing	f = 1 kHz I_p = 0.3 A		27		V_{pp}
		f = 1 kHz I_p = 3 A		24		
		f = 10 kHz I_P = 0.3 A		27		V_{PP}
		f = 10 kHz I_P = 3 A		23		
R	Input Resistance (pin 1)	f = 1 KHz	100	500		KΩ
G_v	Voltage Gain (open loop)			80		dB
e_N	Input Noise Voltage	B = 10 to 10 000 Hz		2		µV
i_N	Input Noise Current			100		pA
CMR	Common-mode Rejection	R_g ≤ 10 KΩ G_v = 30 dB		70		dB
SVR	Supply Voltage Rejection	R_g = 22 KΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz, G_v = 10		60	dB	dB
		R_g = 22 KΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz, dBG_v = 100		40		dB
	Efficiency	f = 1 kHz, R_L = 4 Ω, I_p = 1.6 A ; P_o = 5 W		70		%
		f = 1 kHz, R_L = 4 Ω, I_p = 3 A ; P_o = 18 W		60		%
T_{sd}	Thermal Shut-down Case Temperature	P_{tot} = 12 W		110		°C
		P_{tot} = 6 W		130		

Figure 3 : Open loop frequency response.

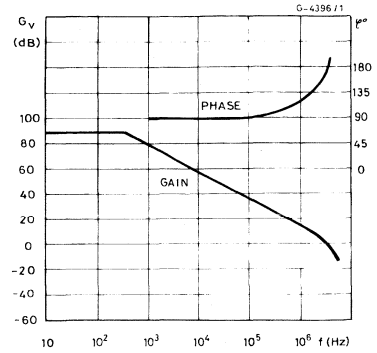


Figure 4 : Closed loop frequency response (circuit of figure 2).

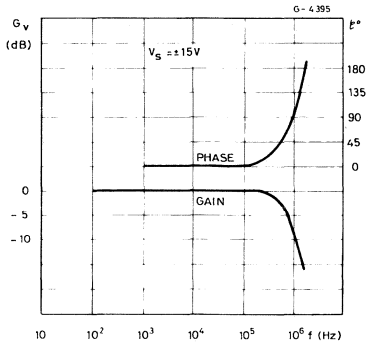


Figure 5 : Large signal frequency response.

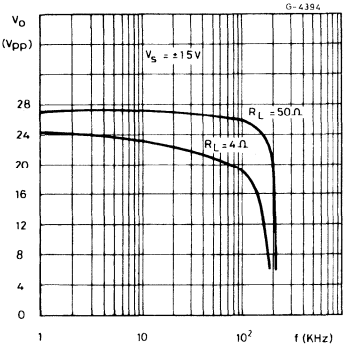


Figure 6 : Maximum output current vs. voltage [VCE] across each output transistor.

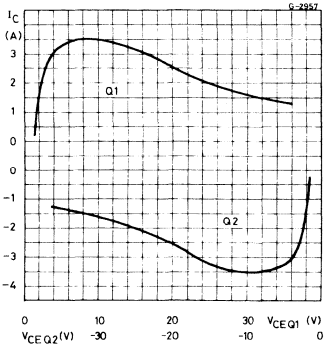


Figure 7 : Safe operating area and collector characteristics of the protected power transistor.

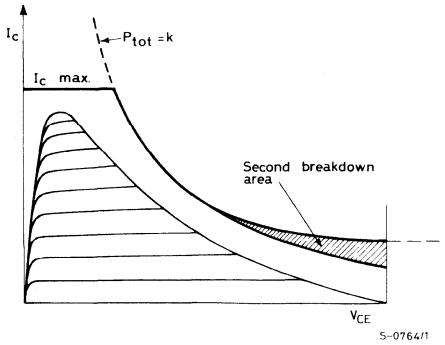


Figure 8 : Maximum allowable power dissipation vs. ambient temperature.

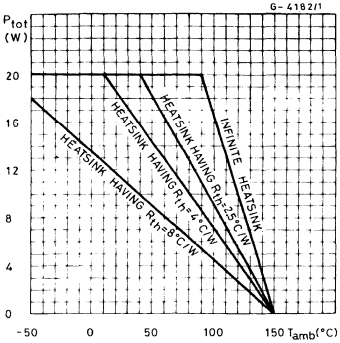
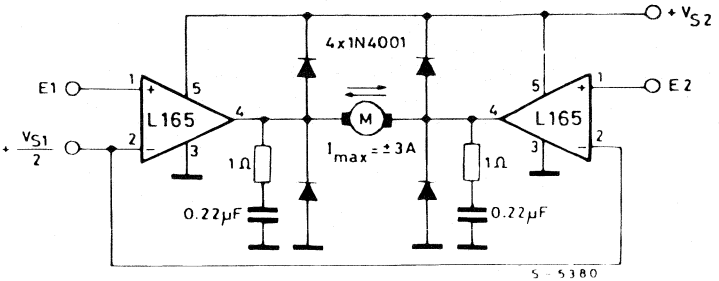
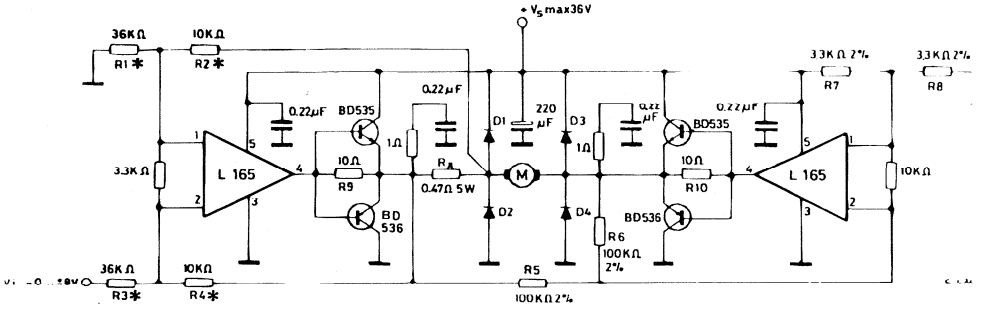


Figure 9 : Bidirectional DC motor control with TTL/CMOS/μP compatible inputs.



Must be $V_{S2} \geq V_{S1}$ E1, E2 = logic inputs
V_{S1} = logic supply voltage

Figure 10 : Motor current control circuit with external power transistors (I_{motor} > 3.5A).

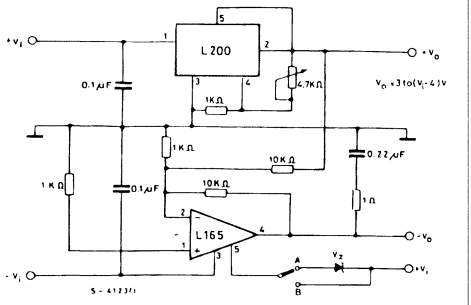


D1 to D4 : $V_F \leq 1.2$ @ I = 4A
trr ≤ 500 ns

Note : The input voltage level is compatible with L291 (5-BIT D/A converter).

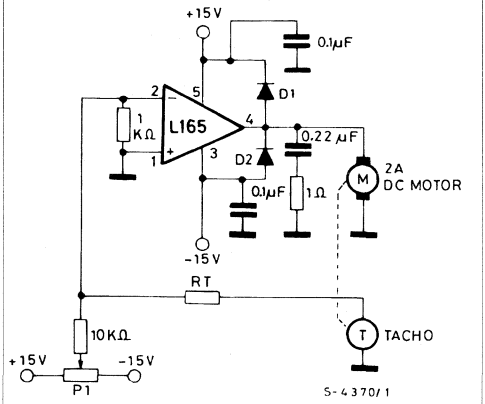
The transfer function is : $\frac{I_M}{V_I} = \frac{R4}{Rx\ R3}$

Figure 11 : High current tracking regulator.



A : for $\pm 18 \leq V_i \leq \pm 32$
Note : V_Z must be chosen in order to verify
$2\,V_i - V_Z \leq 36V$
B : for $V_i \leq \pm 18V$

Figure 12 : Bidirectional speed control of DC motor (Compensation networks not shown).



D1, D2 : VF ≤ 1.2V @ I = 2A
trr ≤ 500 ns

Figure 13 : Split power supply.

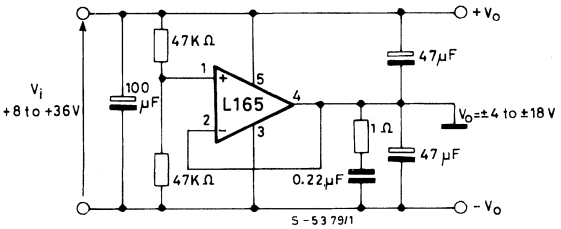
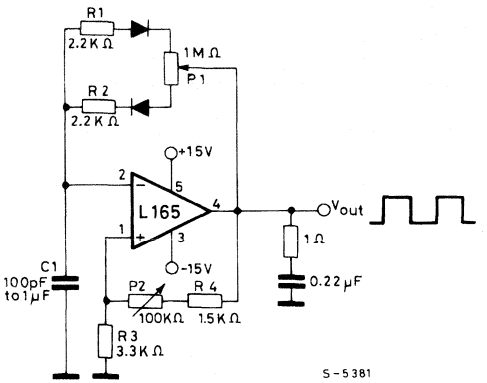


Figure 14 : Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust

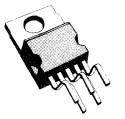
P2 : frequency adjust (f = 700 Hz with C1 = 10 nF, P2 = 100 KΩ, f = 25 Hz with C1 = 10 nF, P2 = 0)

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

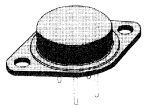
- ADJUSTABLE OUTPUT CURRENT UP TO 2 A (GUARANTEED UP TO T_j = 150 °C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85 V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60 V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

DESCRIPTION

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60 V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



Pentawatt®



TO–3 (4 lead)

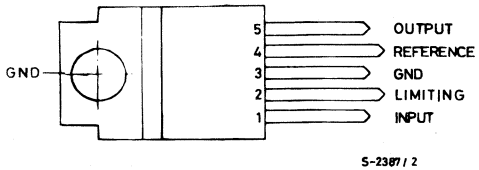
ABSOLUTE MAXIMUM RATINGS

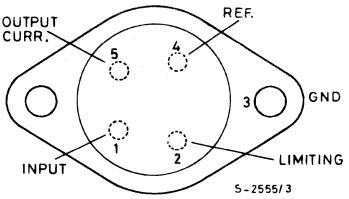
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	40	V
V_i	Peak Input Voltage (10 ms)	60	V
ΔV_{i-o}	Dropout Voltage	32	V
I_o	Output Current	internally limited	
P_{tot}	Power Dissipation	internally limited	
T_{stg}	Storage Temperature	– 55 to 150	°C
T_{op}	Operating Junction Temperature for L200C	– 25 to 150	°C
	for L200	– 55 to 150	°C

THERMAL DATA

			TO–3	Pentawatt®
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35 °C/W	50 °C/W

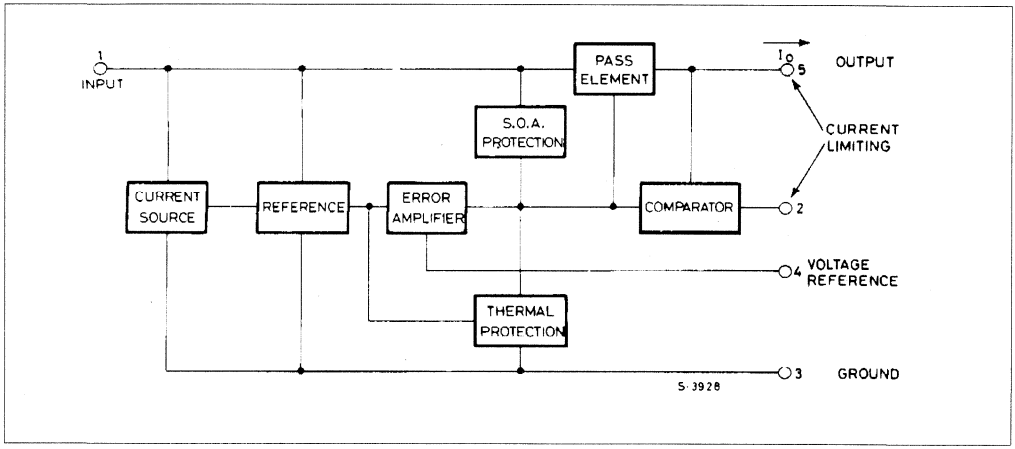
CONNECTION DIAGRAMS AND ORDER CODES (top views)





Type	Pentawatt®	TO-3
L200		L200 T
L200 C	L200 CH L200 CV	L200 CT

BLOCK DIAGRAM



APPLICATION CIRCUITS

Figure 1 : Programmable Voltage Regulator with Current Limiting.

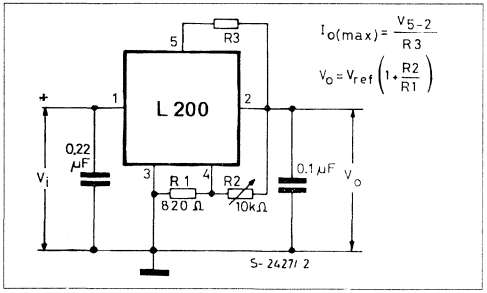
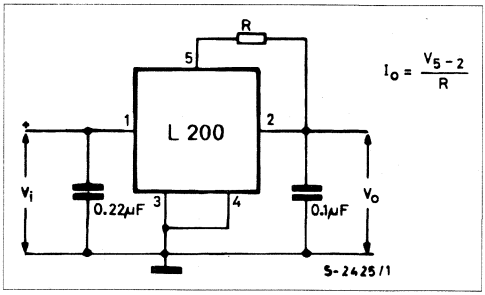
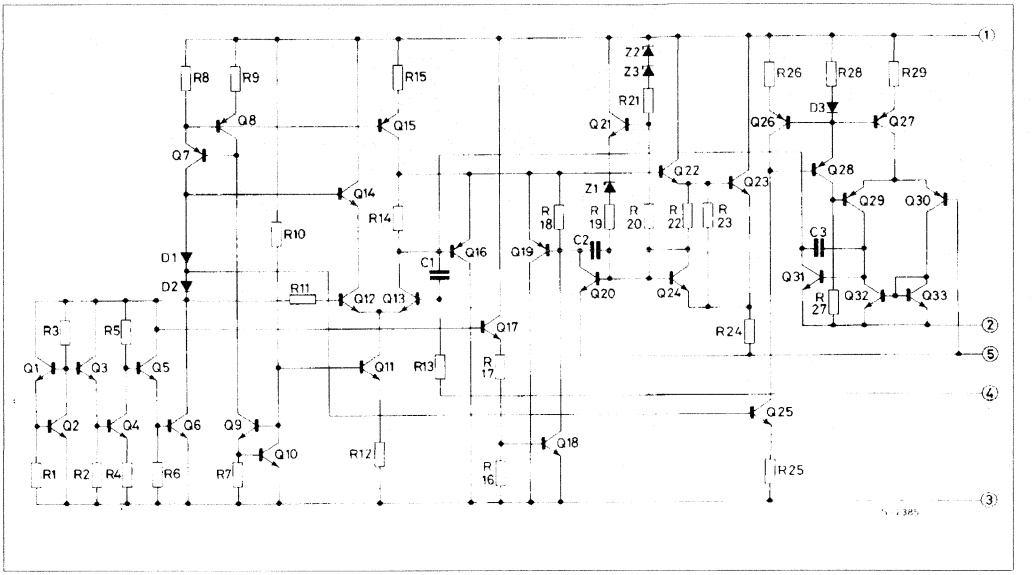


Figure 2 : Programmable Current Regulator.



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent Drain Current (pin 3)	V_i = 20 V		4.2	9.2	mA
e_N	Output Noise Voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output Voltage Range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage Load Regulation (note 1)	ΔI_o = 2 A ΔI_o = 1.5 A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line Regulation	V_o = 5 V V_i = 8 to 18 V	48	60		dB
SVR	Supply Voltage Rejection	V_o = 5 V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB
ΔV_{i-o}	Droupout Voltage between Pins 1 and 5	I_o = 1.5 A $\Delta V_o \leq 2$ %		2	2.5	V
V_{ref}	Reference Voltage (pin 4)	V_i = 20 V I_o = 10 mA	2.64	2.77	2.86	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{ref}	Average Temperature Coefficient of Reference Voltage	V_i = 20 V I_o = 10 mA for T_j = – 25 to 125 °C for T_j = 125 to 150 °C		– 0.25 – 1.5		mV/°C mV/°C
I_4	Bias Current at Pin 4			3	10	µA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average Temperature Coefficient (pin 4)			– 0.5		%/°C
Z_o	Output Impedance	V_i = 10 V $V_o = V_{ref}$ I_o = 0.5 A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

V_{SC}	Current Limit Sense Voltage between Pins 5 and 2	V_i = 10 V $V_o = V_{ref}$ I_5 = 100 mA	0.38	0.45	0.52	V
$\frac{\Delta V_{SC}}{\Delta T \cdot V_{SC}}$	Average Temperature Coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current Load Regulation	V_i = 10 V ΔV_o = 3 V I_o = 0.5 A I_o = 1 A I_o = 1.5 A		1.4 1 0.9		% % %
I_{SC}	Peak Short Circuit Current	$V_i - V_o$ = 14 V (pins 2 and 5 short circuited)			3.6	A

Note 1 : A load step of 2 A can be applied provided that input-output differential voltage is lower than 20 V (see Figure 3).

Note 2 : The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Figure 3 : Typical Safe Operating Area Protection.

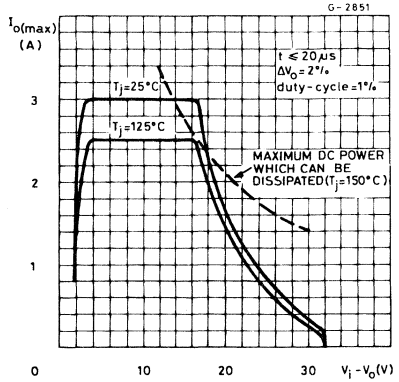


Figure 4 : Quiescent Current vs. Supply Voltage.

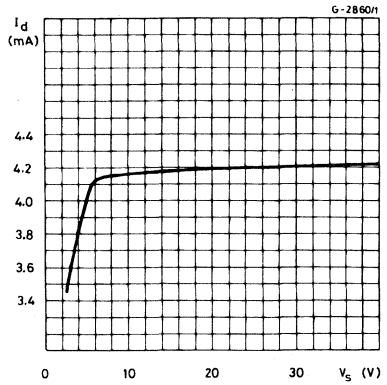


Figure 5 : Quiescent Current vs. Junction Voltage.

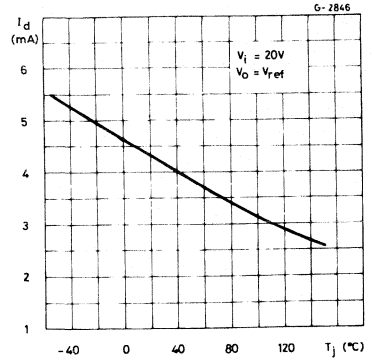


Figure 6 : Quiescent Current vs. Output Current.

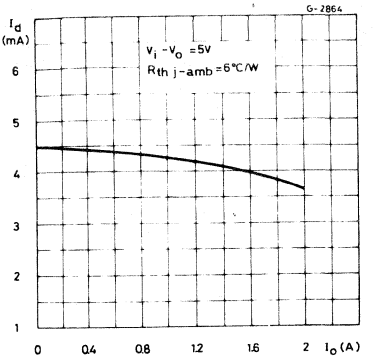


Figure 7 : Output Noise Voltage vs. Output Voltage.

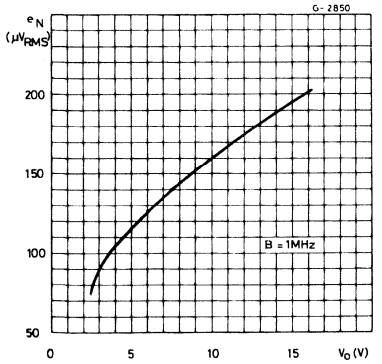


Figure 8 : Output Noise Voltage vs. Frequency.

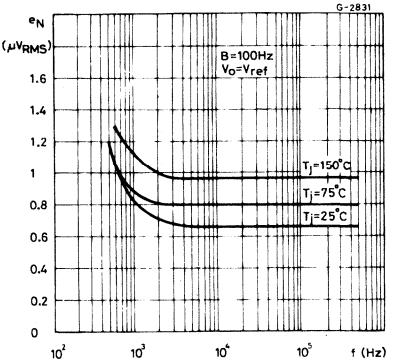


Figure 9 : Reference Voltage vs. Junction Temperature.

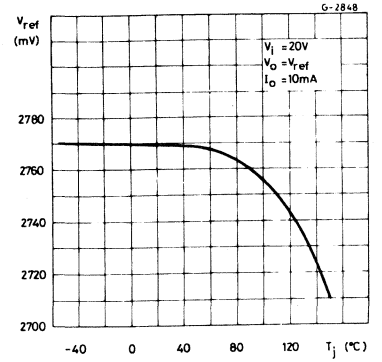


Figure 10 : Voltage Load Regulation vs. Junction Temperature.

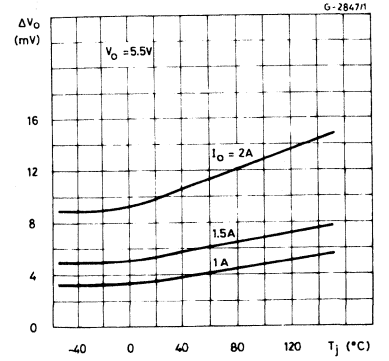


Figure 11 : Supply Voltage Rejection vs. Frequency.

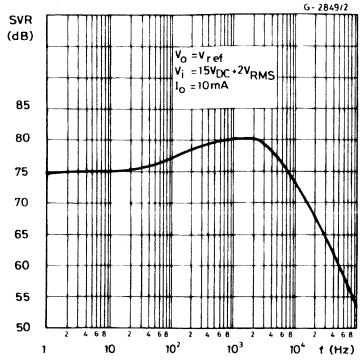


Figure 12 : Dropout Voltage vs. Junction Temperature.

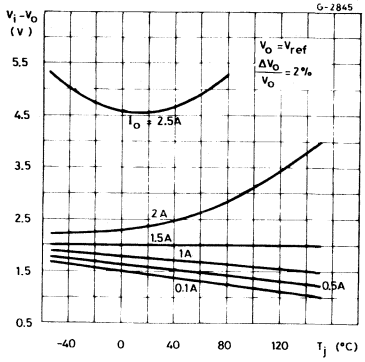


Figure 13 : Output Impedance vs. Frequency.

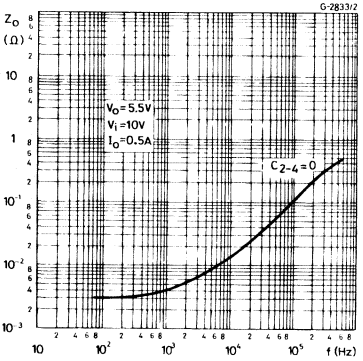


Figure 14 : Output Impedance vs. Output Current.

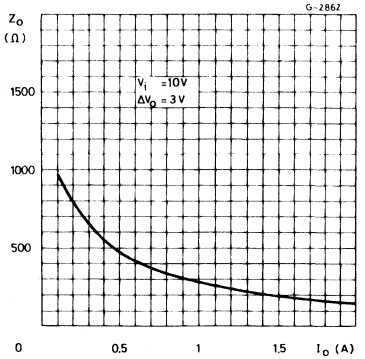


Figure 15 : Voltage Transient Response.

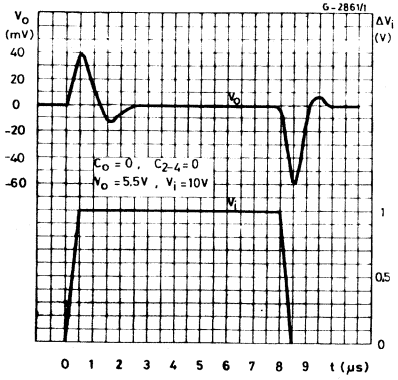
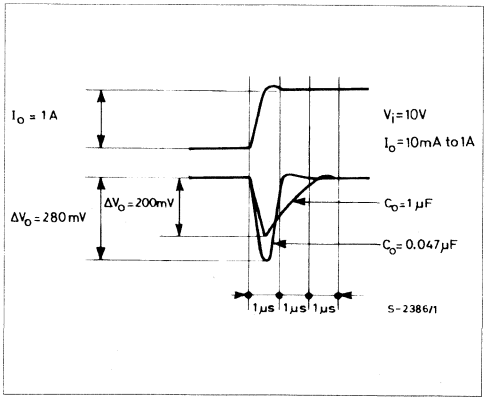


Figure 16 : Load Transient Response.



SGS-THOMSON MICROELECTRONICS

Figure 17 : Load Transient Response.

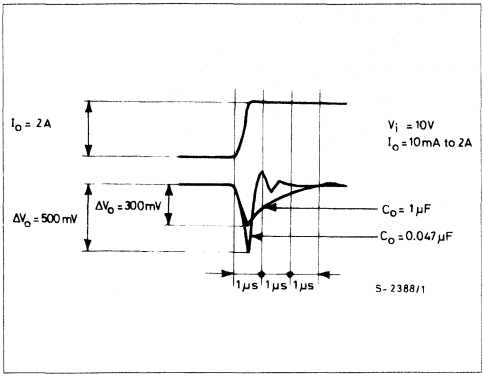
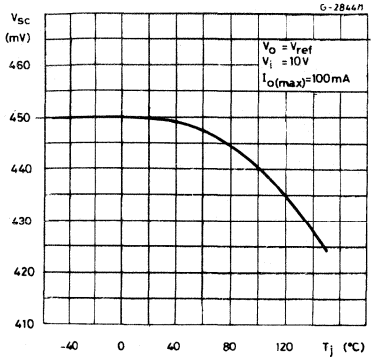


Figure 18 : Current Limit Sense Voltage vs. Junction Temperature.



APPLICATION CIRCUITS

Figure 19 : Programmable Voltage Regulator.

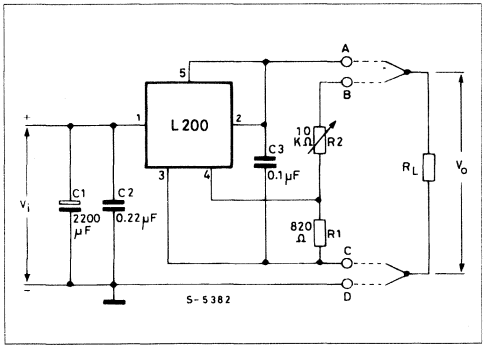


Figure 20 : P.C. Board and Components Layout of Figure 19.

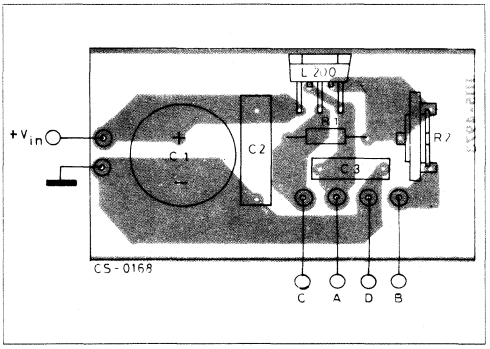


Figure 21 : High Current Voltage Regulator with Short Circuit Protection.

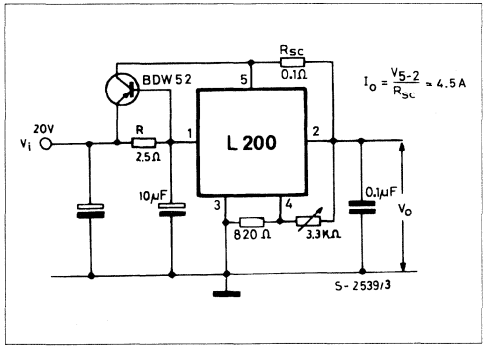


Figure 22 : Digitally Selected Regulator with Inhibit.

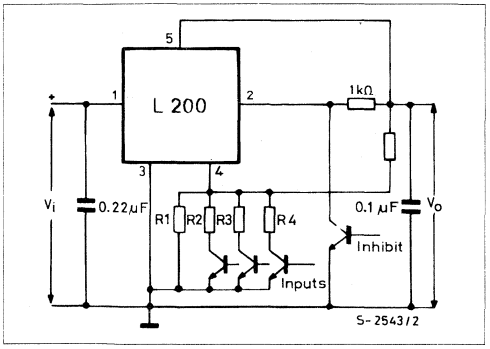
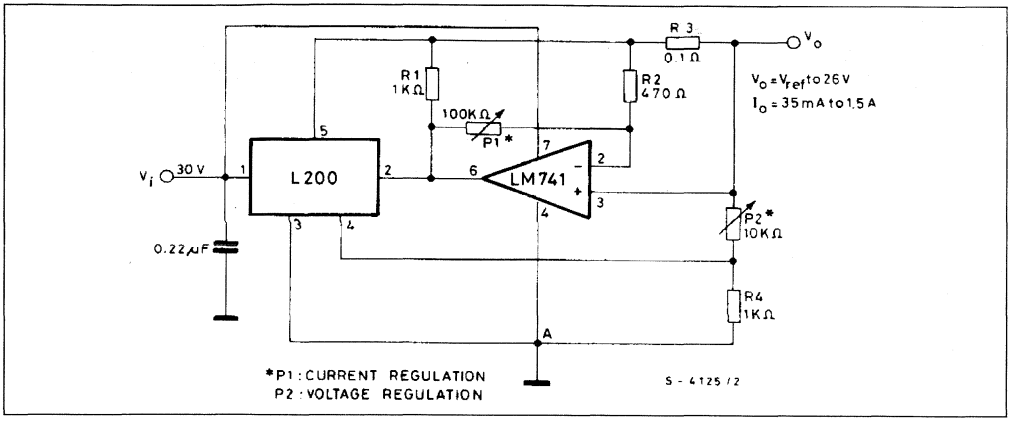


Figure 23 : Programmable Voltage and Current Regulator.



Note : Connecting point A to a negative voltage (for example – 3 V/10 mA) it is possible to extend the output voltage range down to 0 V and to obtain the current limiting down to this level (output short-circuit condition).

Figure 24 : High Current Regulator with NPN Pass Transistor.

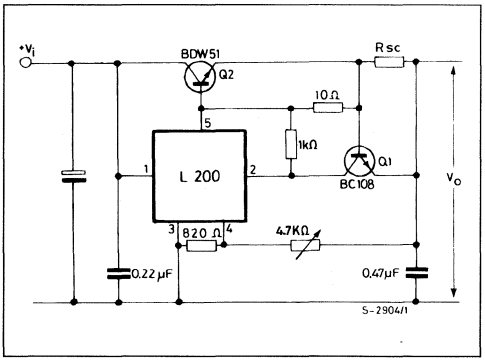
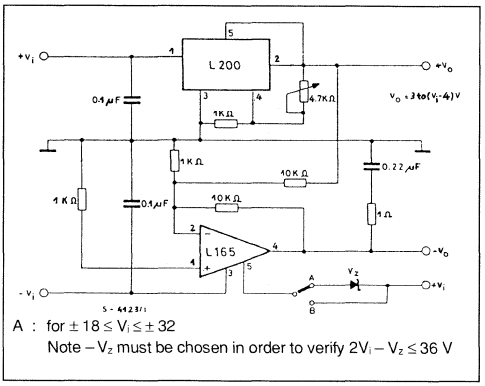


Figure 25 : High Current Tracking Regulator.



A : for $\pm 18 \leq V_i \leq \pm 32$

Note $-V_z$ must be chosen in order to verify $2V_i - V_z \leq 36$ V

Figure 26 : High Input and Output Voltage.

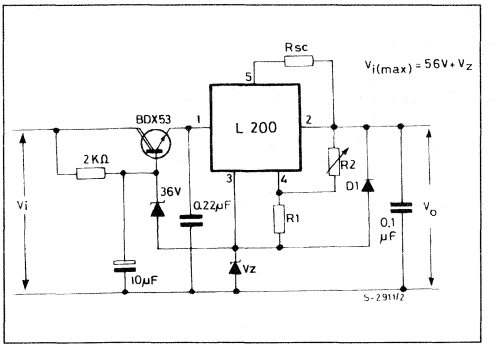
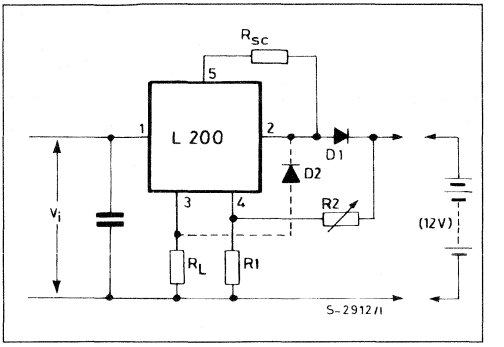


Figure 27 : Constant Current Battery Charger.



The resistors R_1 and R_2 determine the final charging voltage and R_{SC} the initial charging current. D_1 prevents discharge of the battery throught the regulator.

The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12 V/50 mA rating this will indicate incorrect connection.

Figure 28 : 30 W Motor Speed Control.

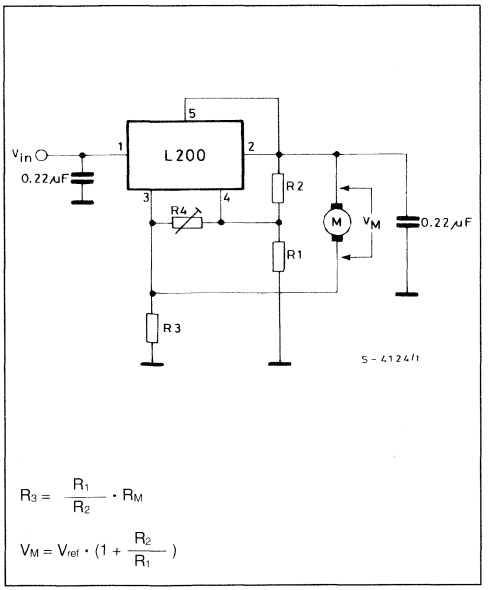


Figure 29 : Low Turn on.

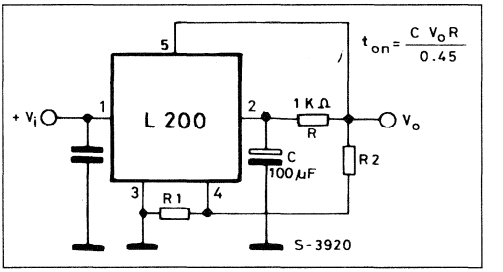
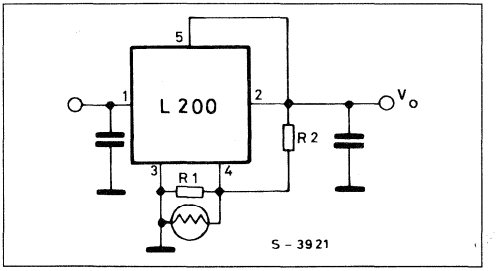


Figure 30 : Light Controller.

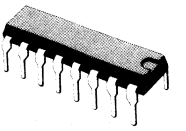


DUAL POWER OPERATIONAL AMPLIFIERS

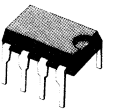
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)



Minidip Plastic

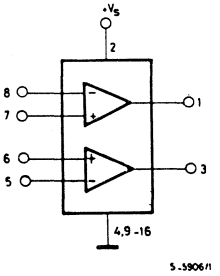
ORDERING NUMBERS:

L272 L272M

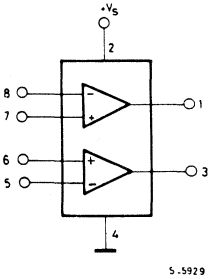
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L272)**, T_{amb} = 50°C **(L272M)** T_{case} = 75°C **(L272)**	1.2 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

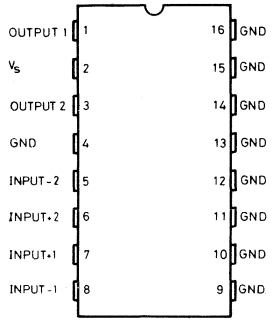


L272

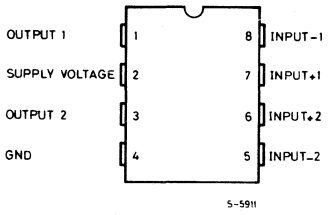


L272M

CONNECTION DIAGRAM
(Top view)

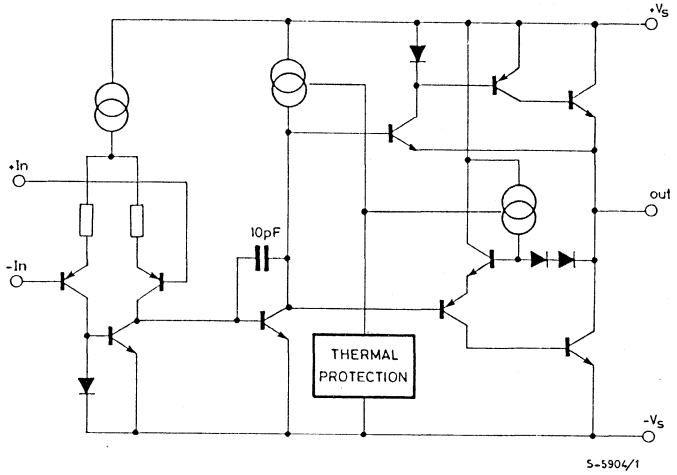


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

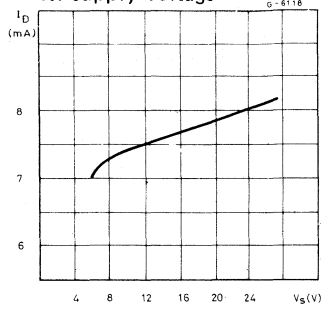


Fig. 2 -- Quiescent drain current vs. temperature

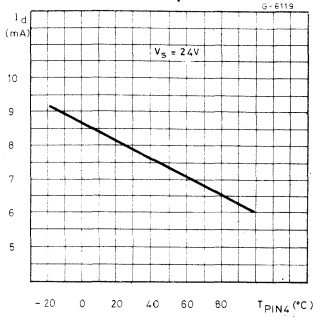


Fig. 3 - Open loop voltage gain

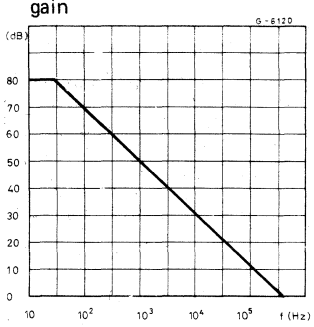


Fig. 4 -- Output voltage swing vs. load current

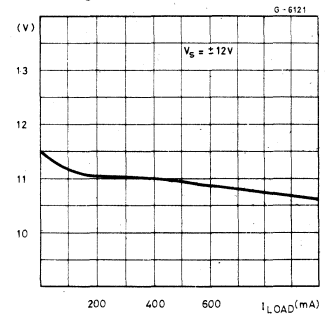


Fig. 5 -- Output voltage swing vs. load current

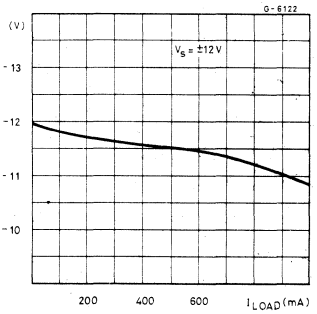


Fig. 6 - Supply voltage rejection vs. frequency

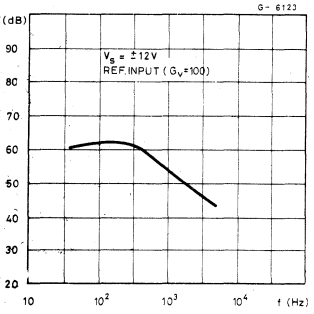


Fig. 7 - Channel separation vs. frequency

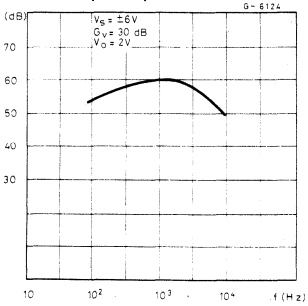
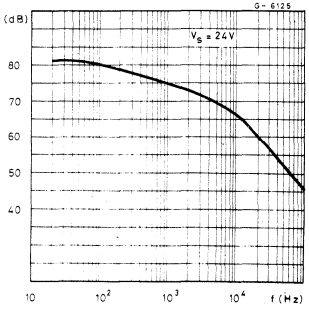


Fig. 8 -- Common mode rejection vs. frequency



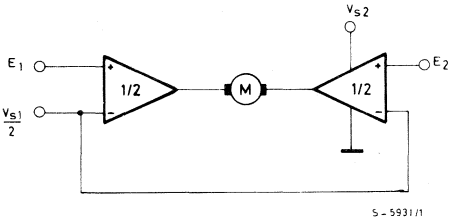
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF +1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

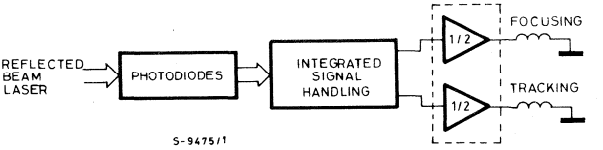


Fig. 11 - Capstan motor control in video recorders

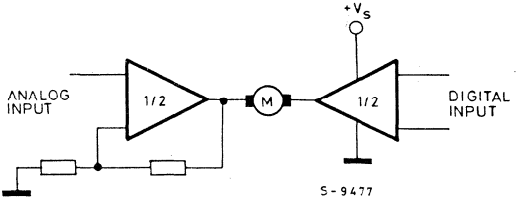
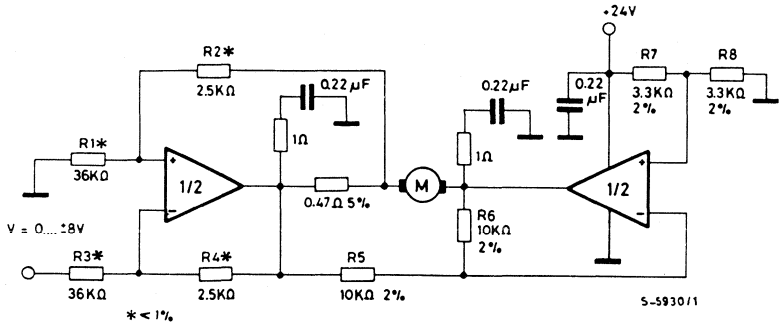


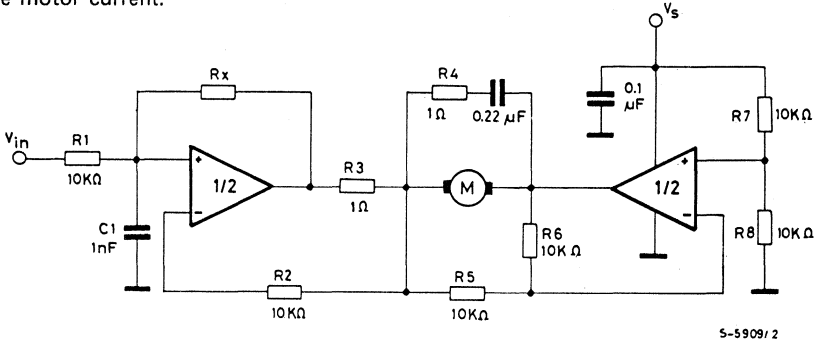
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_i - \frac{V_s}{2}) + |R_o|. I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

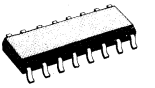


DUAL POWER OPERATIONAL AMPLIFIER

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc. The high gain and high output power capability provide superior performance wheatever an operational amplifier/power booster combination is required.



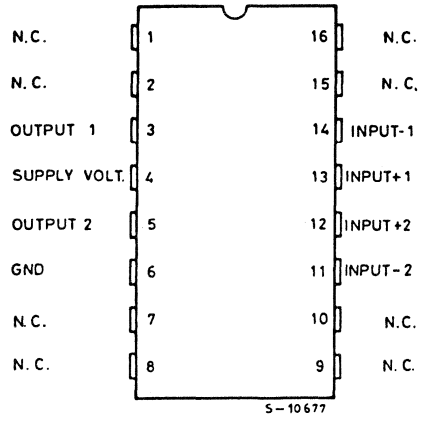
SO-16J

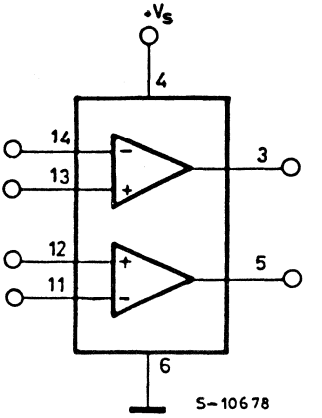
ORDERING NUMBER: L272D

ABSOLUTE MAXIMUM RATINGS

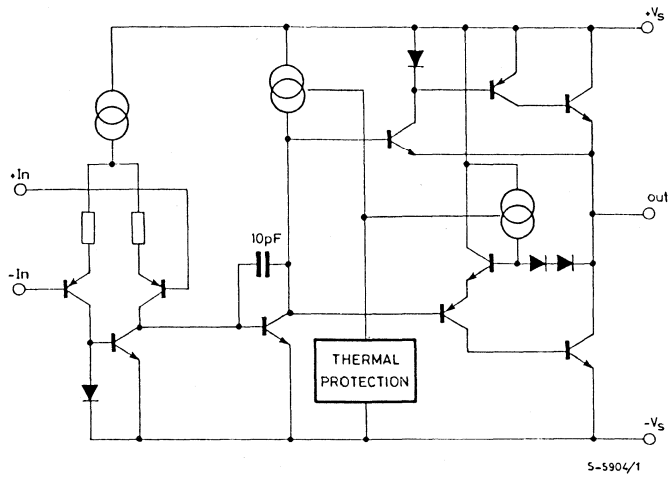
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	1.2	W
T_{op}	Operating Temperature Range	−40 to +85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

CONNECTION DIAGRAMS





SCHEMATIC DIAGRAM (one only)



THERMAL DATA

$R_{thj-alumina(*)}$	Thermal resistance junction-alumina	max 50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

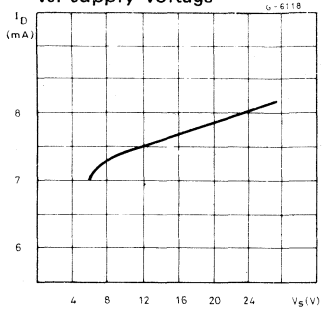


Fig. 2 - Quiescent drain current vs. temperature

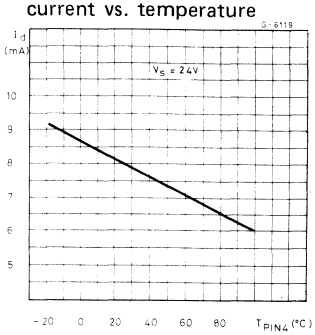


Fig. 3 - Open loop voltage gain

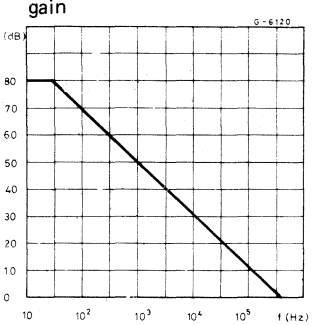


Fig. 4 - Output voltage swing vs. load current

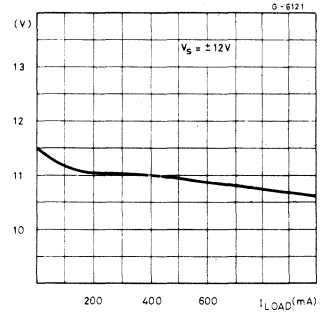


Fig. 5 - Output voltage swing vs. load current

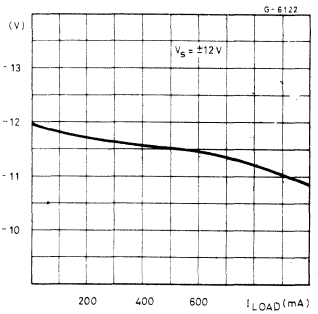


Fig. 6 - Supply voltage rejection vs. frequency

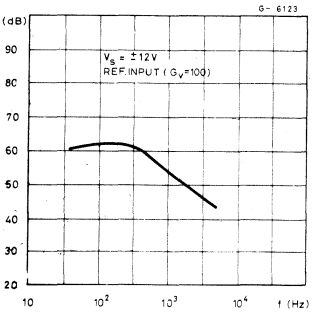


Fig. 7 - Channel separation vs. frequency

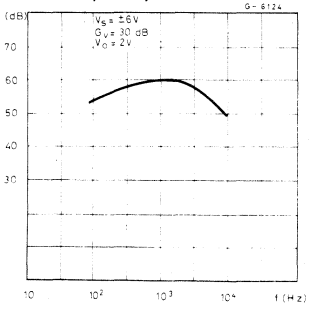
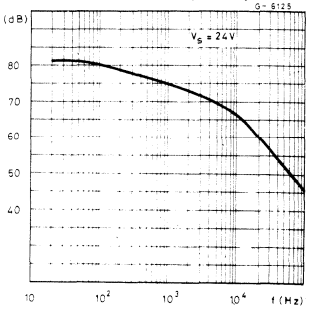


Fig. 8 - Common mode rejection vs. frequency

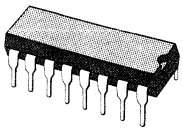


TACHOMETER CONVERTER

The L290, a monolithic LSI circuit in a 16-lead dual inline plastic package, is intended for use with the L291 and L292 which together from a complete **3-chip DC motor positioning system** for applications such as carriage/daisy-wheel position control in typewriters.

The L290/1/2 system can be directly controlled by a microprocessor. The L290 integrates the following functions :

- tacho voltage generator (F/V converter)
- reference voltage generator
- position pulse generator



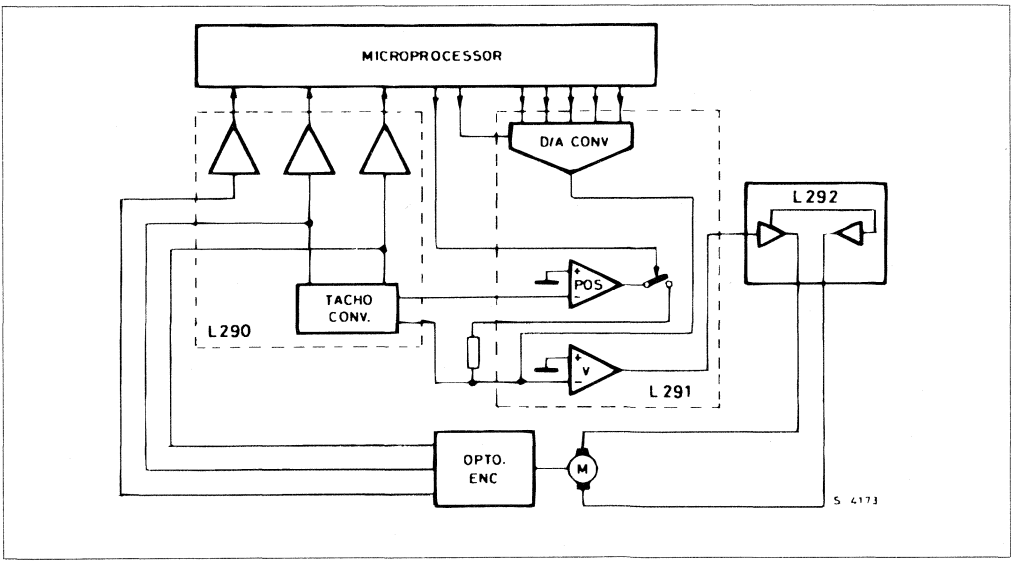
DIP-16 Plastic
(0.25)

ORDER CODE : L290B

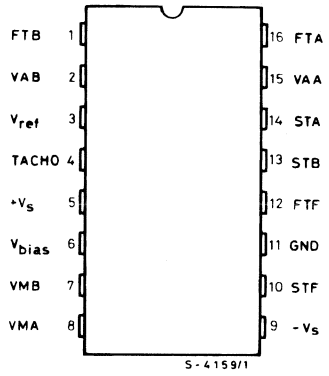
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
V_i (FTA, FTB, FTF)	Input Signals	± 7	V
P_{tot}	Total Power Dissipation T_{amb} = 70 °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

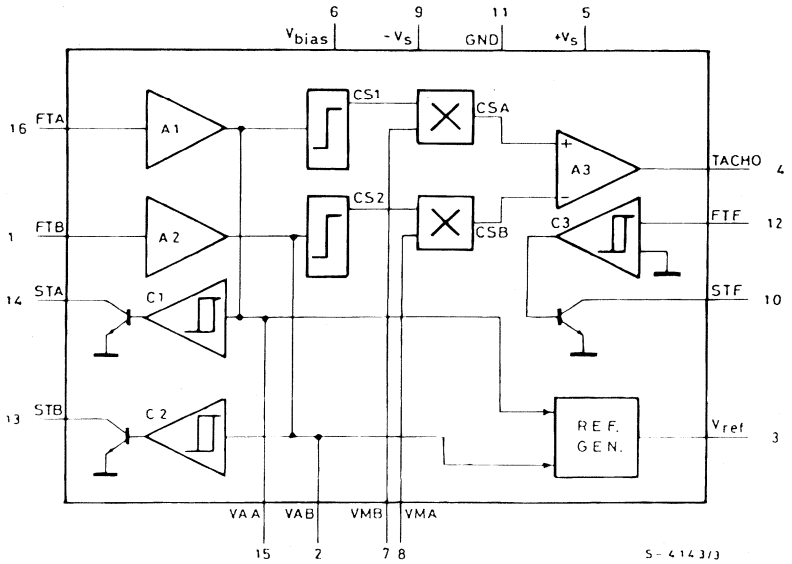
SYSTEM BLOCK DIAGRAM



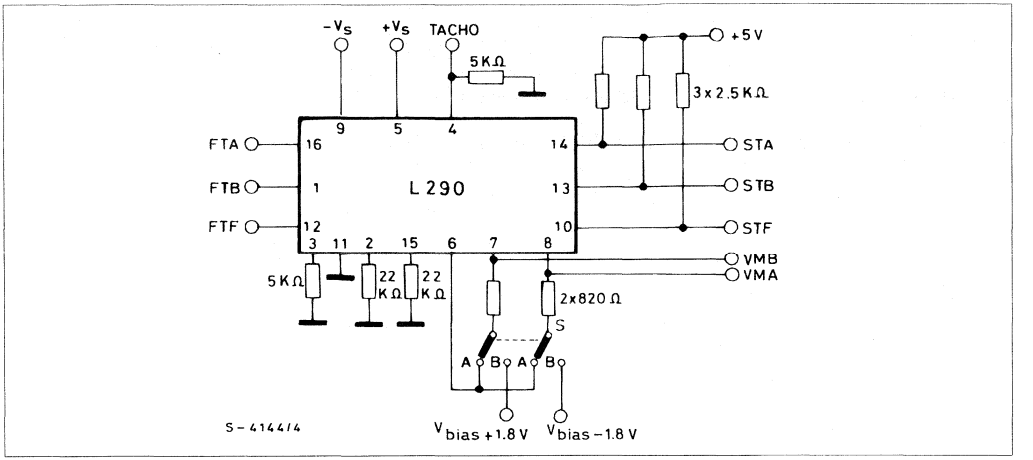
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S in (A), $V_s = \pm 12$ V, $T_{amb} = 25$ °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 10		± 15	V
I_d	Quiescent Drain Current	$V_s = \pm 15$ V		13	20	mA

INPUT AMPLIFIERS (A_1 and A_2)

FTA, FTB	Input Signal from Encoder (pin 1, 16)	f_{max} = 20 KHz	± 0.4		± 0.6	V_p
V_{os}	Output Offset Voltage (pin 2, 15)	FTA = FTB = 0 V			± 55	mV
I_b	Input Bias Current (pin 1, 16)			0.15		µA
G_v	Voltage Gain	f = 10 KHz FTA = FTB = ± 0.6 V_p	22	23	24	dB
V_0	Output Voltage Swing (pin 2, 15)	FTA = FTB = ± 1V_p	± 9.5			V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit

COMPARATORS WITH HYSTERESIS (C_1, C_2, and C_3)

V_{THP} (°)	Positive Threshold Voltage (pin 2, 12, 15)	C_1 and C_2	550		850	mV
		C_3	700		900	mV
V_{THN} (°°)	Negative Threshold Voltage (pin 2, 12, 15)	C_1 and C_2	55		175	mV
		C_3	570		830	mV
ΔFTF	Threshold Hysteresis	C_3	72		120	mV
V_L	Output Voltage (low level) (pin 10, 13, 14)	I_0 = 2 mA FTA = FTB = FTF = 0 V		0.2	0.4	V
I_{leak}	(pins 10, 13, 14)	FTA = FTB = 0.5 V V_{CE} = 5 V FTF = 1 V			1	μA

REFERENCE GENERATOR

V_{ref}	DC Reference Voltage (pin 3)	FTA = FTB = ± 0.5 V_p (*) I_{ref} = 1 mA	4.5	5	5.5	V
I_{ref}	Output Current (pin 3)				1.4	mA

"TACHO" AMPLIFIER (A_3)

V_{os}	Output Offset Voltage (pin 4)	FTA = ± 15 mV FTB = 0.5 V			± 80	mV
V_o	DC Output Voltage (pin 4)	FTA = FTB = ± 0.5 V_p (**) V_{01}	5.4	6	6.6	V
		VMA = VMB = ± 1.25 V_p (***) V_{02}	− 5.4	− 6	− 6.6	
ΔV_0		V_{01} + V_{02}	− 150		+ 150	mV
V_0	Output Voltage Swing (pin 4)	FTA = FTB = 0.5 V	9			V
		Sin (B) FTA = FTB = − 0.5 V	− 9			
V_{MA} V_{MB}	Multiplier Input Voltage (pin 7, 8)			± 1.25	± 1.7	V_p
V_{bias}	Bias Voltage (pin 6)	FTA and FTB Floating	− 6.5		− 8	V

(°) : FTA = FTB = FTF = 0 / 1V

(°°) : FTA = FTB = FTF = 1V / 0

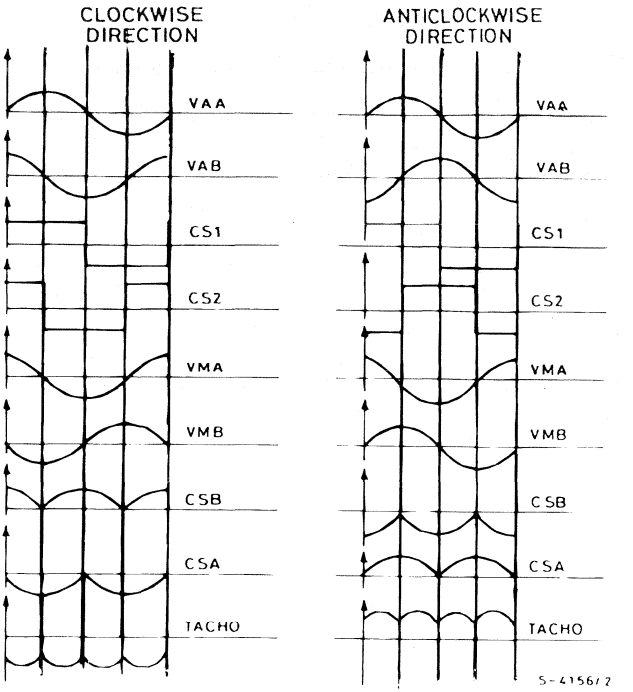
Note : Phase relationship between the signals :

* FTA : 0° FTB : 90°

** FTA : 0° FTB : − 90° V_{MA} = 90° V_{MB} = 0°

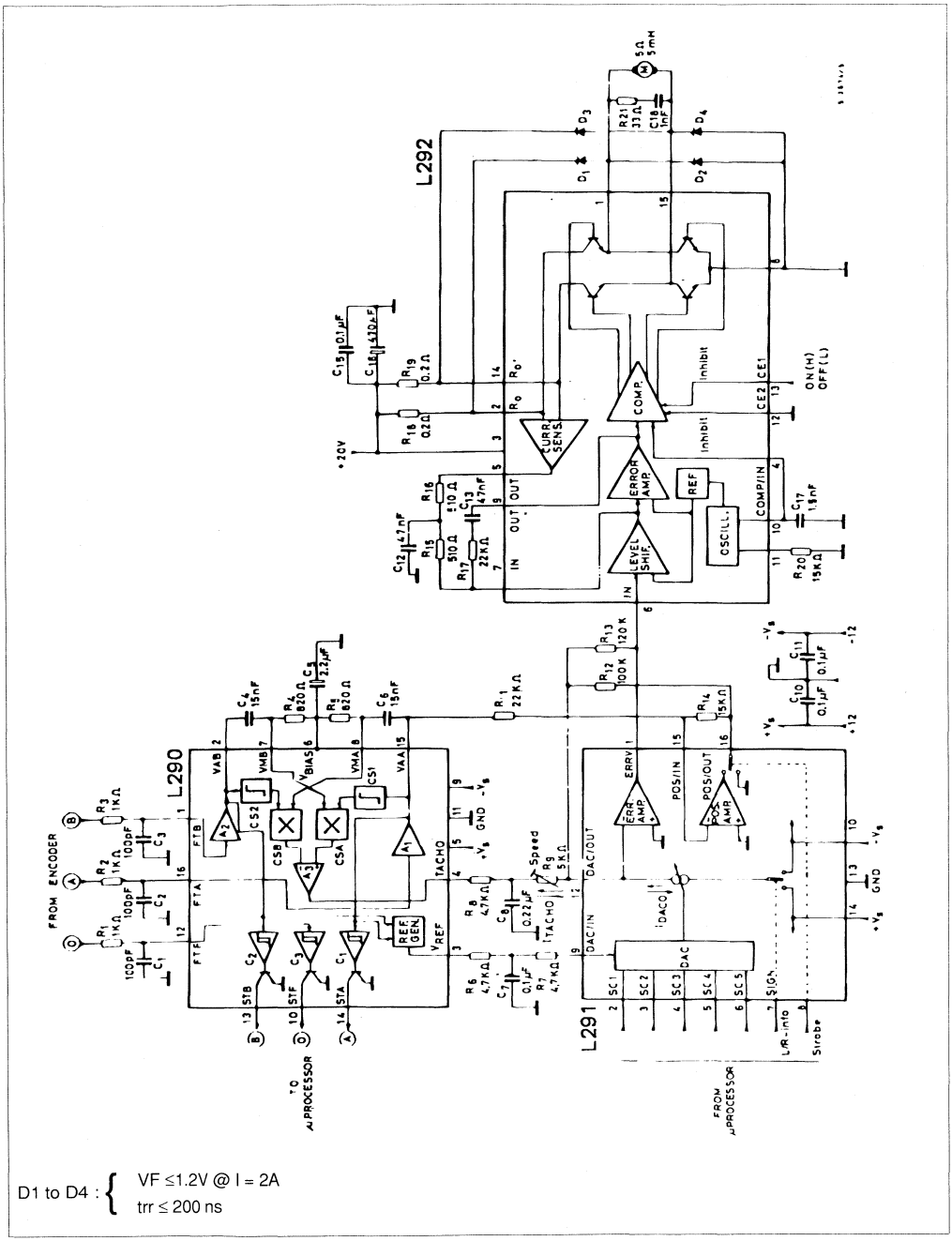
*** FTA : 0° FTB : 90° V_{MA} = 90° V_{MB} = 180°

WAVEFORMS (Neglecting threshold voltage level of the comparators).



SYSTEM DESCRIPTION : refer to the L292 data sheet.

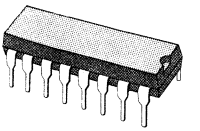
Figure 1 : Complete application circuit.



SGS-THOMSON MICROELECTRONICS

5 BIT – D/A CONVERTER AND POSITION AMPLIFIER

- 5 BIT D/A CONVERTER (1/2 LSB MAX LINEARITY ERROR) ;
- ERROR AMPLIFIER ;
- POSITION AMPLIFIER.



DIP-16
(Plastic 0.25)

ORDER CODE : L291B

DESCRIPTION

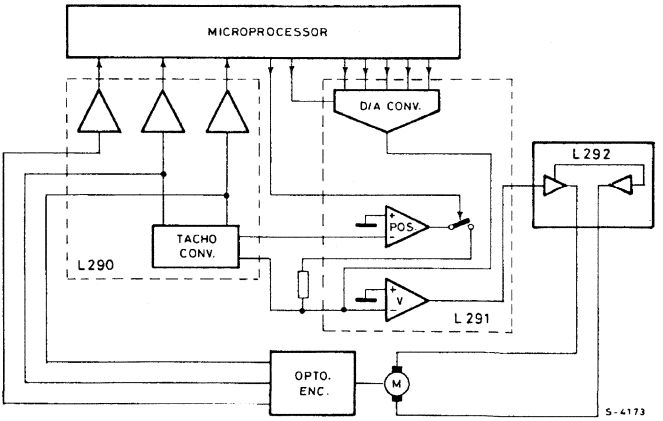
The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete 3 chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.

The L290/291/292 system can be directly controlled by a microprocessor.

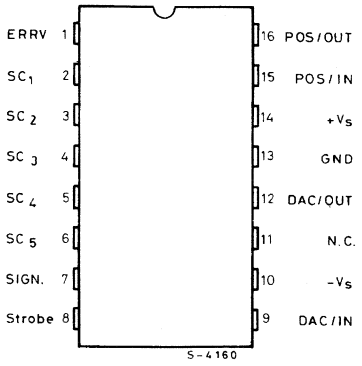
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
P_{tot}	Total Power Dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

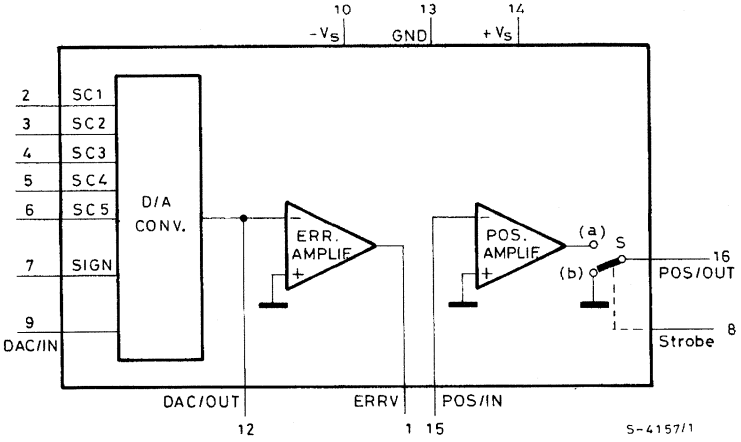
SYSTEM BLOCK DIAGRAM



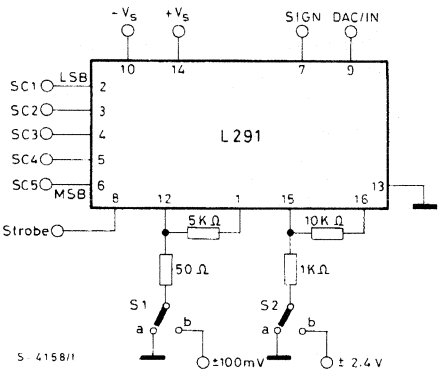
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (refer to the circuit, S1 and S2 in (a), V_S = ± 12 V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		± 10		± 15	V
I_d	Quiescient Drain Current			6.5	10	mA

POSITION AMPLIFIER

V_{strobe}	Enable Voltage Level	V_L(S in (a)) *	0		0.8	V
		V_H(S in (b)) *	2.4		+ V_S	V
V_{os}	Output Offset Voltage (pin 16)	$V_{strobe} = V_L$; G_v = 20 dB			± 50	mV
I_b	Input Bias Current (pin 15)	$V_{strobe} = V_L$			0.3	µA
V_o	Output Voltage Swing (pin 16)	$V_{strobe} = V_L$; S2 in(b) ; V_S = ± 10.8 V	± 9			V
V_R	Residual Output Voltage (pin 16)	$V_{strobe} = V_H$			± 20	mV

* See block diagram and the note for Position Amplifier.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit

D/A CONVERTER

I_{ref}	Current Reference Input Range (pin 9)		0.3		1.2	mA
V_{os}	Current Reference Offset Voltage (pin 9)	I_{ref} = 0.3 to 1.2 mA All Inputs High			± 20	mV
I_o	Output Current Range (pin 12)				1.4	mA
I_o	Output Current (pin 12)	I_{ref} = 0.722 mA SC1 to SC5 = L SIGN = L(I_{o1})	− 1.358	− 1.4	− 1.442	mA
		SIGN = H(I_{o2})	+ 1.358	+ 1.4	+ 1.442	
ΔI_o		$I_{o1} + I_{o2}$	− 21		+ 21	µA
	Linearity Error	I_{ref} = 0.722 mA			1.61	%FS
I_{os}	Pin 12 Output Offset Current (including Error Amplifier bias current)	All Inputs High			± 0.4	µA
V_L	Low Voltage Level (digital inputs)	SC1 = LSB	0		0.8	V
V_H	High Voltage Level (digital inputs)	SC5 = MSB	2.4		+ V_S	V
I_L	Digital Inputs Current (low state)	V_L = 0.4V			− 50	µA
I_H	Digital Inputs Current (high state)	V_H = + V_S			1	µA

ERROR AMPLIFIER

V_{os}	Output Offset Voltage (pin 1)	I_{ref} = 0.5 mA ; All Inputs High G_v = 40 dB			± 200	mV
I_o	Output Current (pin 1)				± 5	mA
V_o	Output Voltage Swing (pin 1)	All Inputs High S1 in (b) ; R_L = 10 KΩ	± 7.4		± 8.4	Vp

D/A CONVERTER

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref}.

The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5 MSB	SC4	SC3	SC2	SC1 LSB	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	O
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to ± 1/2 LSB (or ± 1.61% Full Scale) ; that guarantees its monotonicity.

ERROR AMPLIFIER

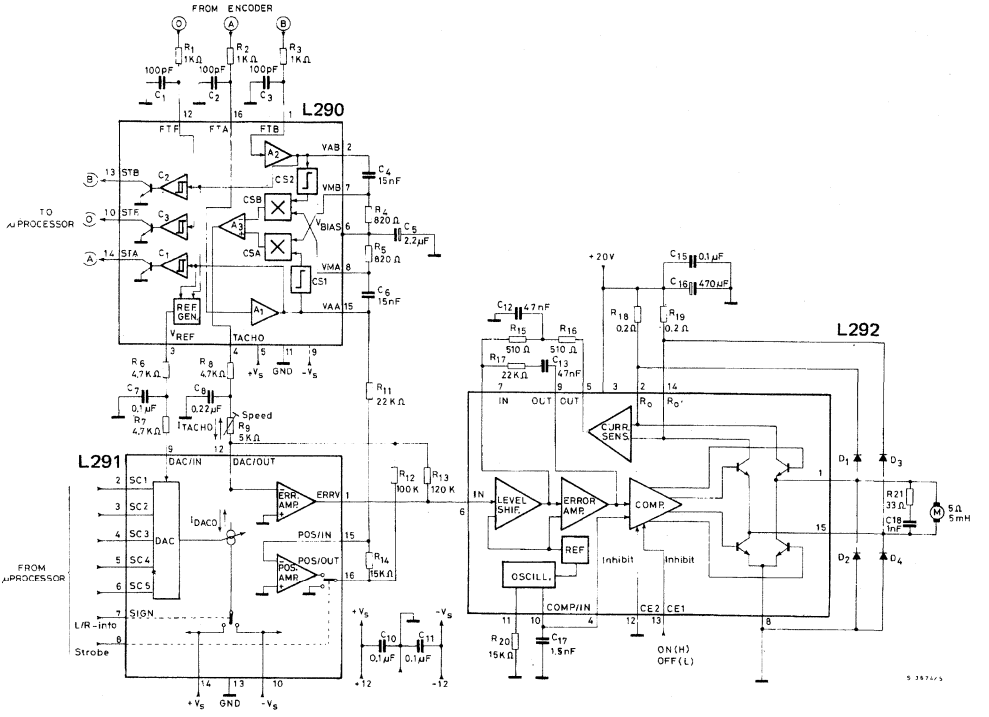
In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

POSITION AMPLIFIER

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when V_{strobe} = Low ; pin 16 is grounded for V_{strobe} = High.

SYSTEM DESCRIPTION : refer to the L292 data sheet.

Figure 1 : Complete Application Circuit.



D1 to D4 : { $V_F \leq 1.2V$ @ I = 2A
trr ≤ 200 ns

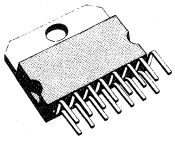
SWITCH–MODE DRIVER FOR DC MOTORS

- DRIVING CAPABILITY : 2 A, 36 V, 30 KHz
- 2 LOGIC CHIP ENABLE
- EXTERNAL LOOP GAIN ADJUSTEMENT
- SINGLE POWER SUPPLY (18 TO 36 V)
- INPUT SIGNAL SYMMETRIC TO GROUND
- THERMAL PROTECTION

DESCRIPTION

The L292 is a monolithic LSI circuit in 15-lead Multiwatt ® package. It is intended for use, together with L290 and L291, as a complete **3-chip motor positioning system** for applications such as carriage/daisy-wheel position control in typewrites.

The L290/1/2 system can be directly controlled by a microprocessor.



Multiwatt 15

ORDER CODE : L292

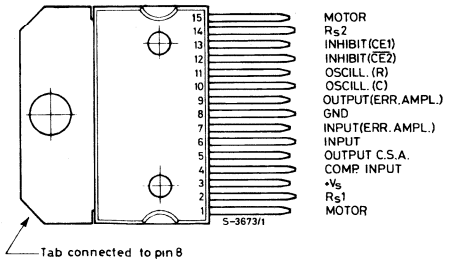
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply	36	V
V_i	Input Voltage	– 15 to + V_s	V
$V_{inhibit}$	Inhibit Voltage	0 to V_s	V
I_o	Output Current	2.5	A
P_{tot}	Total Power Dissipation (T_{case} = 75 °C)	25	W
T_{stg}	Storage and Junction Temperature	– 40 to + 150	°C

TRUTH TABLE

Vinhibit		Output Stage Condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal Operation
H	L	Disabled
H	H	Disabled

CONNECTION DIAGRAM (top view)



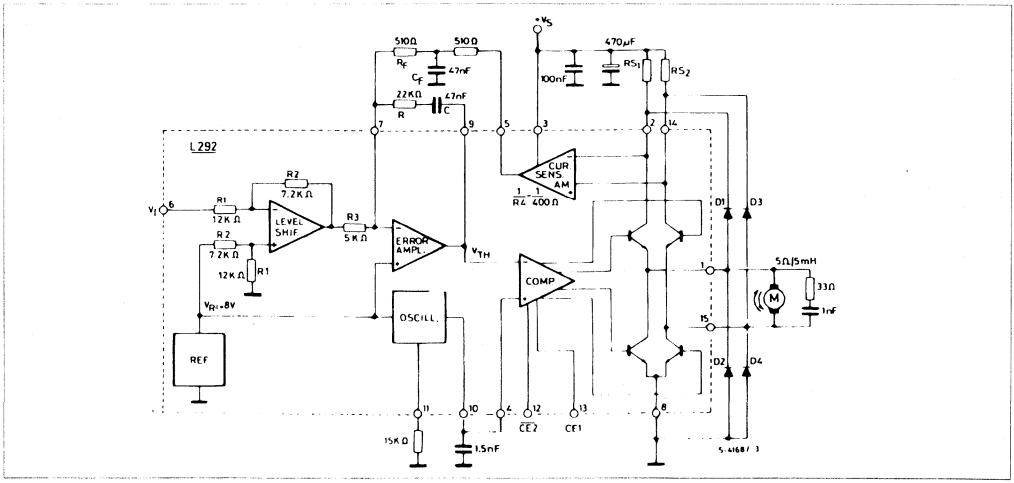
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 36 V, T_{amb} = 25 °C, f_{osc} = 20 KHz unless otherwise specified)

	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			18		36	V
I_d	Quiescent Drain Current	V_s = 20 V (offset null)			30	50	mA
V_{os}	Input Offset Voltage (pin 6)		I_o = 0			± 350	mV
$V_{inh.}$	Inhibit Low Level (pin 12,13)					2	V
	Inhibit High Level (pin 12,13)			3.2			V
$I_{inh.}$	Low Voltage Condition	$V_{inh.}$(L) = 0.4 V				− 100	μA
	High Voltage Conditions	$V_{inh.}$(H) = 3.2 V				10	μA
I_i	Input Current (pin 6)	V_I = − 8.8 V				− 1.8	mA
		V_I = + 8.8 V				0.5	mA
V_i	Input Voltage (pin 6)	$R_{S1} = R_{S2}$ = 0.2 Ω	I_o = 2 A		9.1		V
			I_o = −2 A		− 9.1		V
I_o	Output Current	V_I = ± 9.8 V $R_{S1} = R_{S2}$ = 0.2 Ω		± 2			A
V_D	Total Drop Out Voltage	(inluding sensing resistors)	I_o = 2 A			5	V
			I_o = 1 A			3,5	V
V_{RS}	Sensing Resistor Voltage Drop	T_j = 150 °C	I_o = 2 A			0.44	V
$\frac{I_o}{V_i}$	Transconductance	$R_{S1} = R_{S2}$ = 0.2 Ω		205	220	235	mA / V
		$R_{S1} = R_{S2}$ = 0.4 Ω			120		mA / V
f_{osc}	Frequency Range (pin 10)			1		30	KHz

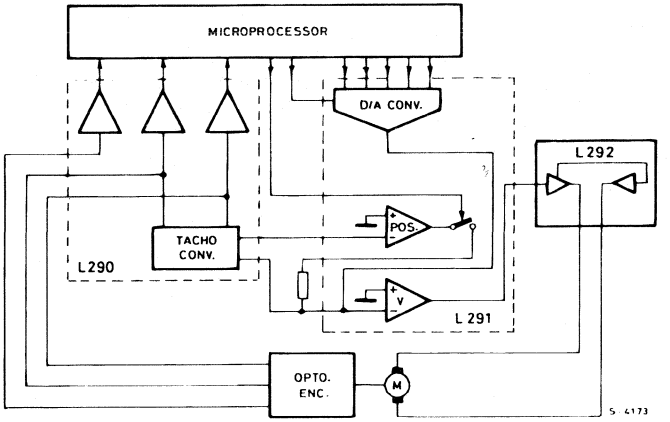
BLOCK DIAGRAM AND TEST CIRCUIT



SYSTEM DESCRIPTION

The L290, L291 and L292 are intended to be used as a 3-chip microprocessor controlled positioning system. The devices may be used separately - particularly the L292 motor driver - but since they will usually be used together, a description of a typical L290/1/2 system follows.

Figure 1 : System Block Diagram.



The system operates in two modes to achieve high speed, high-accuracy positioning.
Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel.
When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal thus reducing accelerating torque. The motor continues to run at top speed but under closed-loop control
As the target position is approached, the microprocessor lowers the value of the speed-demand word ; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.
At that time, the microprocessor orders a switch to the position mode, (strobe signal at pin 8 of L291) and within 3 to 4 ms the L292 drives the motor to a null position, where it is held by electronic "detenting".
The mechanical/electrical interface consists of an optical encoder which generates two sinusoidal signals 90° out of phase (leading according to the motor direction) and proportional in frequency to the speed of rotation. The optical encoder also provides an output at one position on the disk which is used to set the initial position.
The opto encoder signals, FTA and FTB are filtered by the networks R_2 C_2 and R_3 C_3 (referring to Fig.4) and are supplied to the FTA/FTB inputs on the L290.
The main function of the L290 is to implement the following expression :

$$\text{Output signal (TACHO)} = \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

Thus the mean value of TACHO is proportional to the rotation speed and its polarity indicates the direction of rotation.
The above function is performed by amplifying the input signals in A_1 and A_2 to obtain V_{AA} and V_{AB} (typ.7 V_p). From V_{AA} and V_{AB} the external differentiator RC networks R_5 C_6 and R_4C_4 give the signals V_{MA} and V_{MB} which are fed to the multipliers.

The second input to each multiplier consists of the sign of the first input of the other multiplier before differentiation, these are obtained using the comparators C_{S1} and C_{S2}. The multiplier outputs, C_{SA} and C_{SB}, are summed by A_3 to give the final output signal TACHO. The peak-to-peak ripple signal of the TACHO can be found from the following expression :

$$V_{ripple\ p\text{-}p} = \frac{\pi}{4}(\sqrt{2} - 1) \cdot V_{thaco\ DC}$$

The max value of TACHO is :

$$V_{tacho\ max} = \frac{\pi}{4}\sqrt{2} \cdot V_{thaco\ DC}$$

Using the comparators C_1 and C_2 another two signals from V_{AA} and V_{AB} are derived — the logic signals STA and STB.
These signals are used by the microprocessor to determine the position by counting the pulses.
The L290 internal reference voltage is also derived from V_{AA} and V_{AB} :

$$V_{ref} = |V_{AA}| + |V_{AB}|$$

This reference is used by the D/A converter in the L291 to compensate for variations in input levels, temperature changes and ageing.
The "one pulse per rotation" opto encoder output is connected to pin 12 of the L290 (FTF) where it is squared to give the STF logic output for the microprocessor.
The TACHO signal and V_{ref} are sent to the L291 via filter networks R_8 C_8 R_9 and R_6 C_7 R_7 respectively. Pin 12 of this chip is the main summing point of the system where TACHO and the D/A converter output are compared.
The input to the D/A converter consists of 5 bit word plus a sign bit supplied by the microprocessor. The sign bit represents the direction of motor rotation. The (analogue) output of the D/A converter – DAC/OUT – is compared with the TACHO signal and the resulting error signal is amplified by the error amplifier, and subsequently appears on pin 1.
The ERRV signal (from pin 1, L291) is fed to pin 6 of the final chip, the L292 H-bridge motor-driver.This input signal is bidirectional so it must be converted to a positive signal because the L292 uses a single supply voltage. This is accomplished by the first stage - the level shifter, which uses an internally generated 8 V reference.
This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_{20}, C_{17} - pins 11 and 10) where :

$$1f_{osc} = \frac{1}{2RC} \qquad (\text{with } R \geq 8.2\ K\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30 KHz.
Motor currrent is regulated by an internal loop in the L292 which is performed by the resistors R_{18}, R_{19} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.
The choice of the external components in these RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements.The values shown in the diagram are for a 5Ω, 5 mH motor. (See L292 Transfer Function Calculation in Application Information).
The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.
The interval between one side of the bridge switching off and the other switching on, τ , is programmed by C_{17} in conjunction with an internal resistor $R\tau$.
This can be found from :

$$\tau = R\tau \cdot C_{pin\ 10}.\ (C_{17} \text{ in the diagram})$$

Since $R\tau$ is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5 μs $C_{pin\ 10}$ should be around 1.5 nF.
The current sense resistors R_{18} and R_{19} should be high precision types (maximum tolerance ± 2 %) and the recommended value is given by :

$$R_{max} \cdot I_{o\ max} \leq 0.44\ V$$

It is possible to synchronize two L292's, if desired, using the network shown in fig. 2.
Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively).
Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18 V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generates spikes as high as 1.5 V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see fig. 3).

Figure 2.

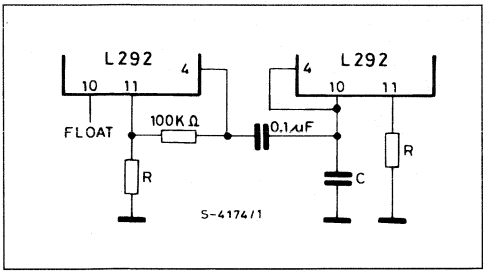


Figure 3.

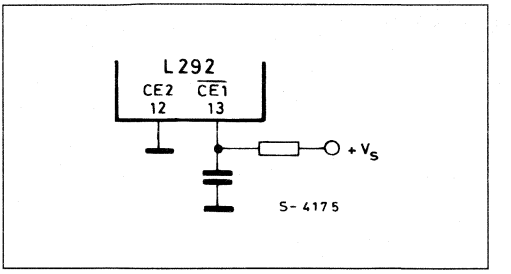
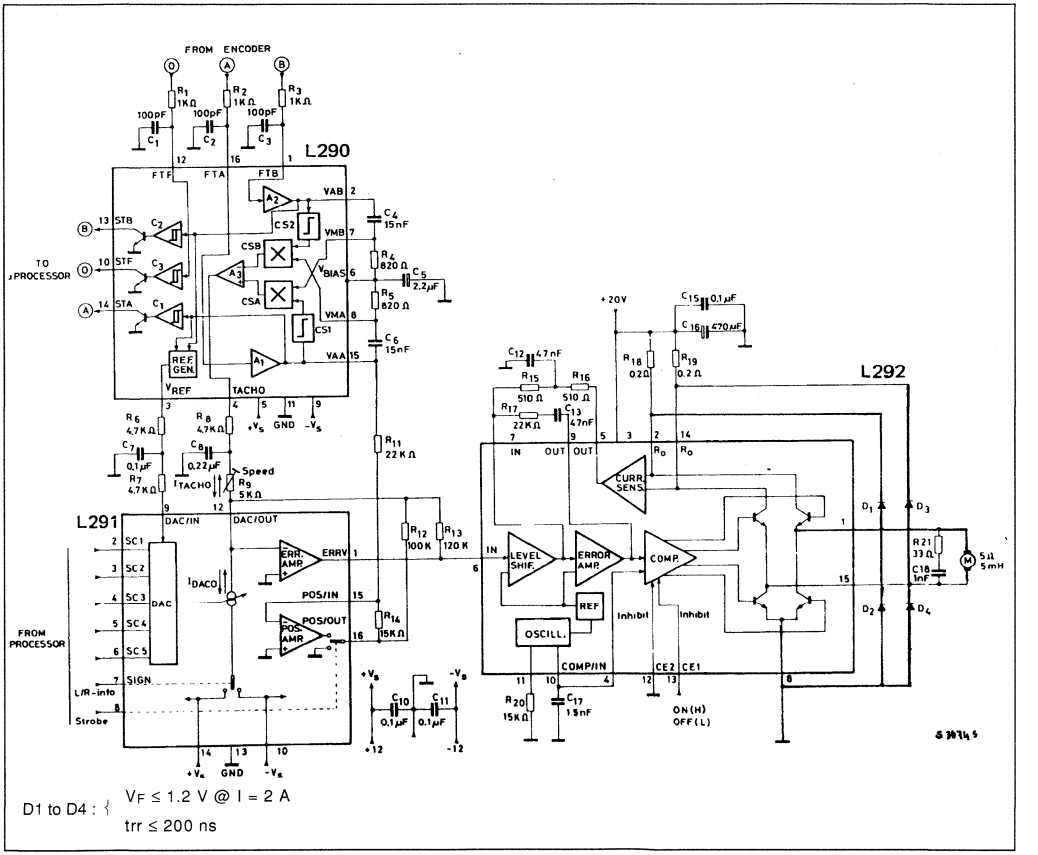


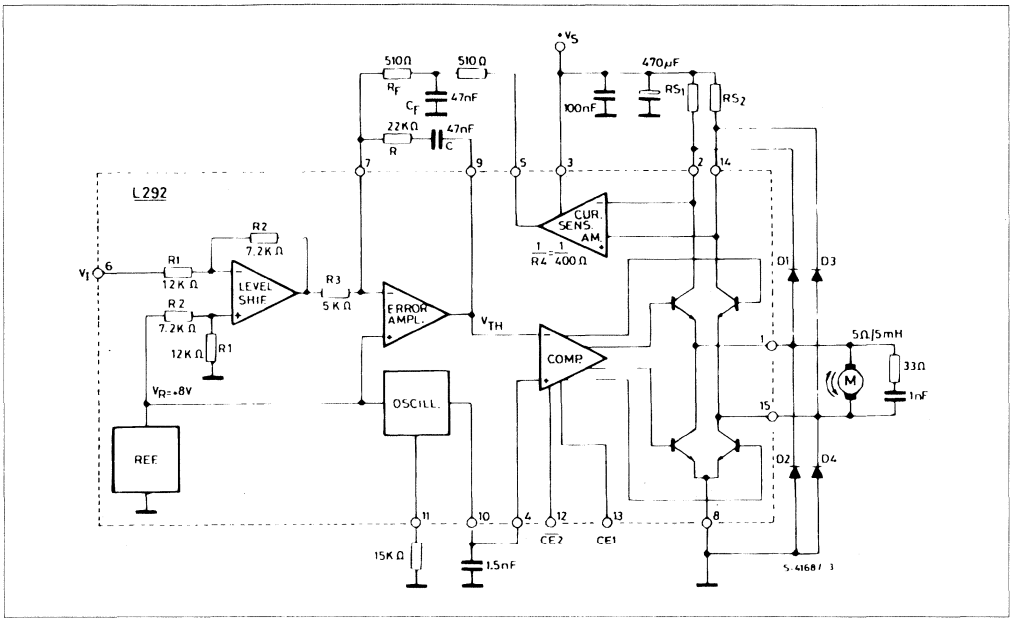
Figure 4 : Application Circuit.



APPLICATION INFORMATION

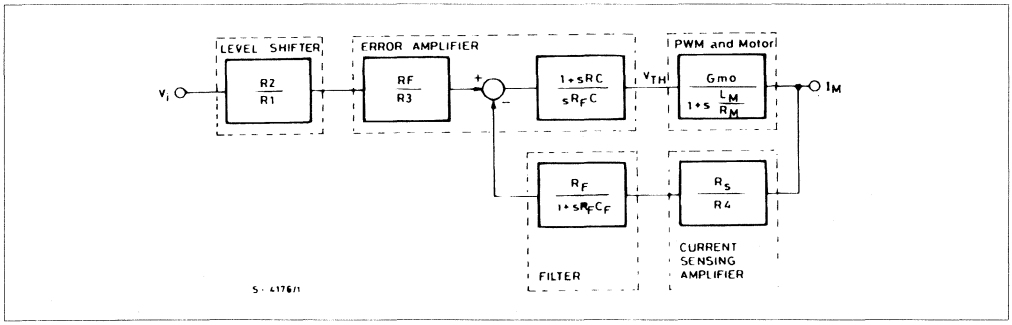
This section has been added in order to help the designer for the best choise of the values of external components.

Figure 5 : L292 Block Diagram.



The schematic diagram used for the Laplace analysis of the system is shown in fig. 6.

Figure 6.



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3}\ \Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance, R_M = Motor resistance, I_M = Motor current

$G_{mo} = \left.\frac{I_M}{\quad}\right|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current(I_M)).

Neglecting the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes :

$$G_{mo} = \frac{1}{R_M} \frac{2\,V_S}{V_R} \qquad \text{where : } V_S = \text{supply voltage},\ V_R = 8\ V\ (\text{reference voltage}) \tag{1}$$

DC TRANSFER FUNCTION

In order to be sure that the current loop is stable the following condition is imposed :

$$1 + sRC = 1 + s\frac{L_M}{R_M} \qquad \text{(pole cancellation)} \tag{2}$$

$$\text{from which } RC = \frac{L_M}{R_M} \qquad \text{(Note that in practice R must greater than 5.6 K}\Omega\text{)}$$

The transfer function is then,

$$\frac{I_M}{V_I}(s) = \frac{R_2 R_4}{R_1 R_3} \; G_{mo} \; \frac{1 + s R_F C_F}{G_{mo} R_s + s R_4 C + s^2 R_F C_F R_4 C} \tag{3}$$

In DC condition, this is reduced to

$$\frac{I_M}{V_I}(o) = \frac{R_2 R_4}{R_1 R_3} \cdot \frac{1}{R_s} = \frac{0.044}{R_s} \left[\frac{A}{V}\right] \tag{4}$$

OPEN-LOOP GAIN AND STABILITY CRITERION

For $RC = L_M / R_M$, the open loop gain is:

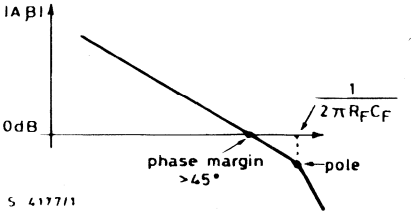
$$A\beta = \frac{1}{sR_F C} \cdot G_{mo} \frac{R_s}{R_4} \frac{R_F}{1 + s R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \frac{1}{s(1 + s R_F C_F)} \tag{5}$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_F C_F}$ must be $|A\beta| < 1$ (see fig .7), that is :

$$|A\beta|_f = \frac{1}{2\pi R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \frac{R_F C_F}{\sqrt{2}} < 1 \tag{6}$$

Figure 7 : Open Loop Frequency Response.



CLOSED-LOOP SYSTEM STEP RESPONSE

a) Small- signals analysis.

The transfer function (3) can be written as follows :

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_S} \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \qquad (7)$$

where $\omega_o = \sqrt{\frac{G_{mo} R_S}{R_4 C R_F C_F}}$ is the cutoff frequency

$$\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_S}}$$ is the dumping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal.

Examples :

1) $\xi = 1$ from which

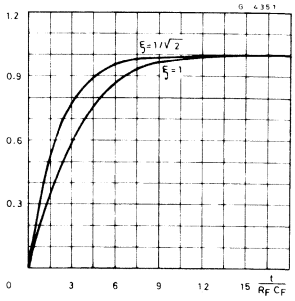
$$I_M(t) = \frac{0.044}{R_S}\left[1 - e^{-\frac{t}{2R_F C_F}}\left(1 + \frac{t}{4R_F C_F}\right)\right] . V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.044}{R_S}\left(1 - \cos\frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}}\right) V_i$$

Figure 8 : Small Signal Step Response (normalized amplitude vs. $t / R_F C_F$).



V_7 = 200 mV/div.
I_M = 100 mA/div.
t = 100 µs/div.
with V_I = 1.5 Vp.

It is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time : the voltage at pin 7 (inverting input of the error amplifier) is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.
The previous linear analysis is correct for this example.
Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is :

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \qquad \text{(phase margin = 45°)}$$

b) Large signal reponse
The large step signal response is limited by slew-rate and inductive load.
In this case, during the rise-time of the motor current, the L292 works in open-loop condition.

CLOSED LOOP SYSTEM BANDWIDTH.

A good choice for ξ is the value $1/\sqrt{2}$. In this case :

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_S} \cdot \frac{1 + s R_F C_F}{1 + 2s R_F C_F + 2s^2 R_F^2 C_F^2} \qquad (8)$$

The module of the transfer function is :

$$\left|\frac{I_M}{V_I}\right| = \frac{0.044}{R_S} \cdot \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}} \qquad (9)$$

The cutoff frequency is derived by the expression (9) by putting $\left|\frac{I_M}{V_I}\right| = 0.707 \cdot \frac{0.044}{R_S}$ (–3 dB), from which :

$$\omega_T = \frac{0.9}{R_F C_F} \qquad f_T = \frac{0.9}{2\pi R_F C_F}$$

Example :

a) Data

- Motors charasteristics: $L_M = 5$ mH, $R_M = 5\ \Omega$, $L_M / R_M = 1$msec
- Voltage and current charasteristics: $V_s = 20$ V, $I_M = 2$ A, $V_I = 9.1$ V
- Closed loop bandwidth : 3 kHz.

b) Calculation

- From relationship (4) :

$$R_s = \frac{0.044}{I_M} V_I = 0.2\ \Omega$$

and from (1) :

$$G_{mo} = \frac{2V_S}{R_M V_R} = 1\ \Omega^{-1}$$

- RC = 1 msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows :

$$\xi^2 = \frac{1}{2} = \frac{400\ C}{4R_F C_F . 0.2}$$

- The cutoff frequency is :

$$f_T = \frac{143 .10^{-3}}{R_F C_F} = 3\ \text{kHz}$$

c) Summarising

- $RC = 1.10^{-3}$ sec
- $\frac{1000\ C}{R_F C_F} = 1$
- $R_F C_F \cong 47\ \mu s$

$C = 47$ nF, $R = 22\ K\Omega$

For $R_F = 510\ \Omega \rightarrow C_F = 92$ nF

PUSH-PULL FOUR CHANNEL DRIVERS

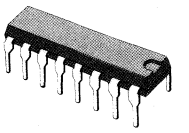
- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (NON REPETITIVE)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

The L293B and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

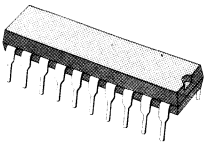
Additionally, the L293E has external connection of sensing resistors, for switchmode control.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

The L293B and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.



DIP-16 Plastic
(0.4)



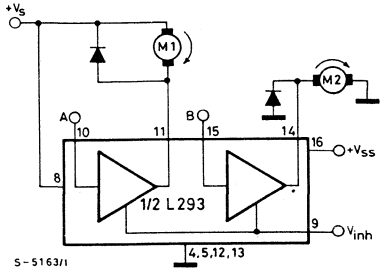
Powerdip
16+2+2

ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

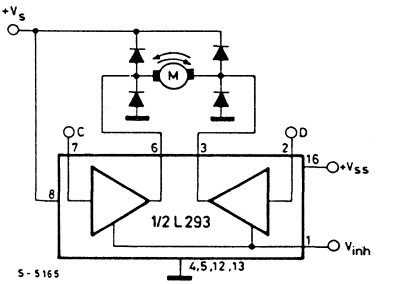
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

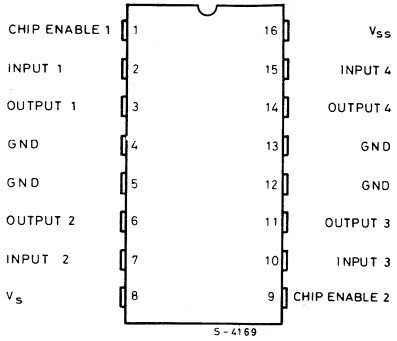
DC motor control

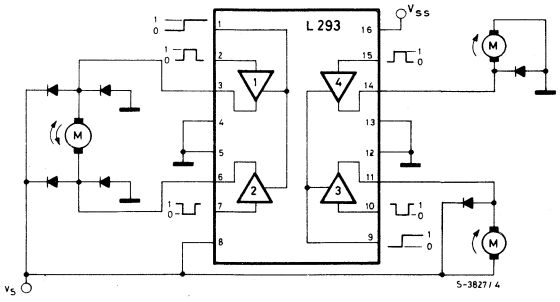


Bidirectional DC motor control

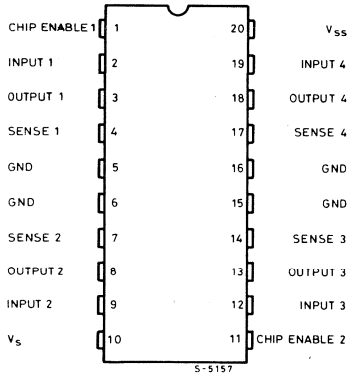


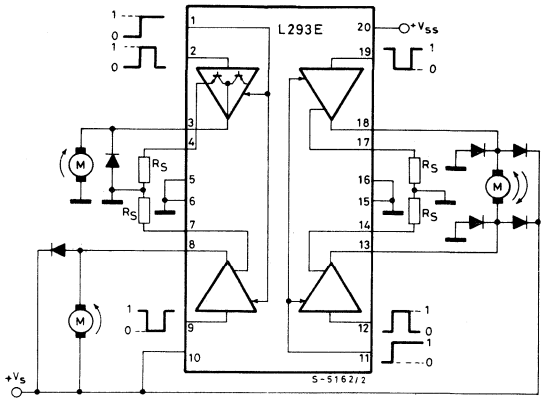
CONNECTION AND BLOCK DIAGRAM (L293)
(top view)



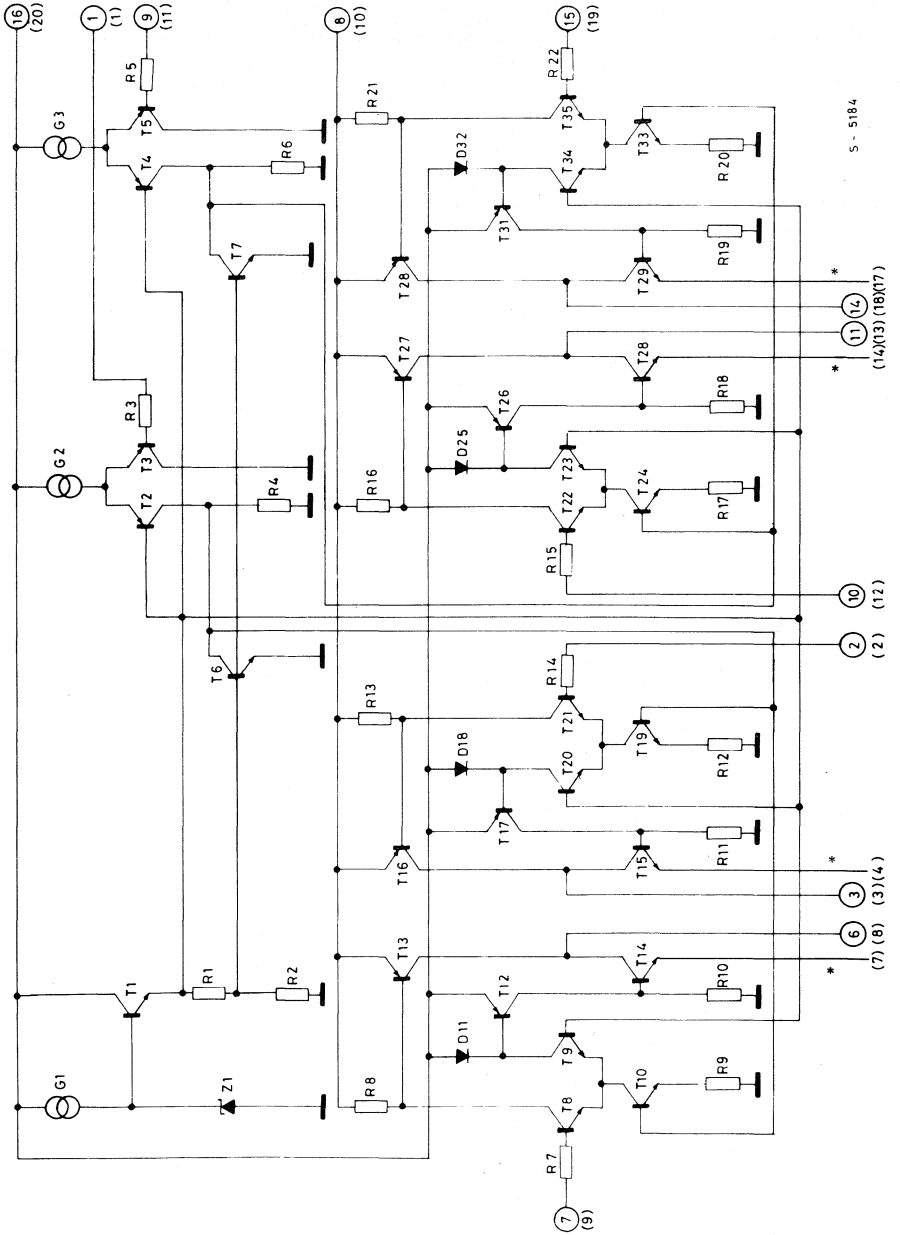


CONNECTION AND BLOCK DIAGRAM (L293E)
(top view)





SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).
○ Pins of L293 ( ) Pins of L293E

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S= 24V, V_{SS}= 5V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		V_{ss}		36	V
V_{ss}	Logic supply voltage		4.5		36	V
I_s	Total quiescent supply current	V_i = L I_o = 0 V_{inh}= H		2	6	mA
		V_i = H I_o = 0 V_{inh}= H		16	24	
		V_{inh}= L			4	
I_{ss}	Total quiescent logic supply current	V_i = L I_o = 0 V_{inh}= H		44	60	mA
		V_i = H I_o = 0 V_{inh}= H		16	22	
		V_{inh}= L		16	24	
V_{iL}	Input low voltage		-0.3		1.5	V
V_{iH}	Input high voltage	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{iL}	Low voltage input current	V_{IL} = 1.5V			-10	µA
I_{iH}	High voltage input current	$2.3V \leq V_{iH} \leq V_{ss} - 0.6V$		30	100	µA
V_{inhL}	Inhibit low voltage		-0.3		1.5	V
V_{inhH}	Inhibit high voltage	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{inhL}	Low voltage inhibit current	V_{inhL} = 1.5V		-30	-100	µA
I_{inhH}	High voltage inhibit current	$2.3V \leq V_{inhH} \leq V_{ss} - 0.6V$			± 10	µA
V_{CEsatH}	Source output saturation voltage	I_o = -1A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage	I_o = 1A		1.2	1.8	V
V_{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)				2	V
t_r	Rise time	0.1 to 0.9 V_o (*)		250		ns
t_f	Fall time	0.9 to 0.1 V_o (*)		250		ns
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o (*)		750		ns
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o (*)		200		ns

(*) See fig. 1.

(**) Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.}$ (°°)
H	H	H
L	L	H
H	X (°)	L
L	X (°)	L

(°) High output impedance.
(°°) Relative to the considerate channel.

Fig. 1 - Switching times

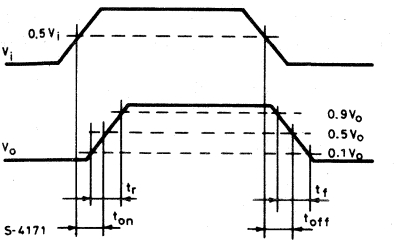


Fig. 2 - Saturation voltage vs. output current

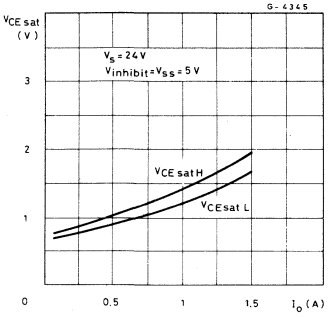


Fig. 3 - Source saturation voltage vs. ambient temperature

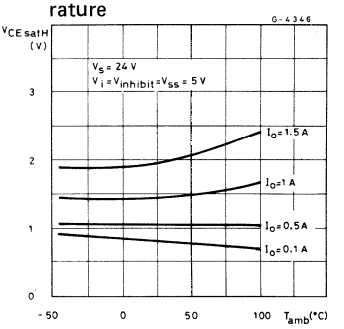


Fig. 4 - Sink saturation voltage vs. ambient temperature

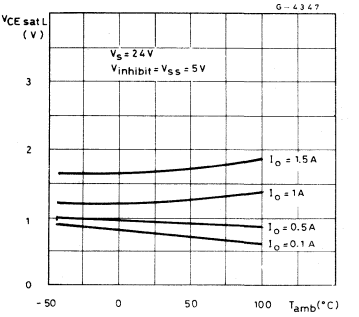


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

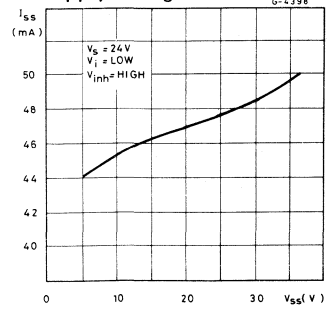


Fig. 6 - Output voltage vs. input voltage

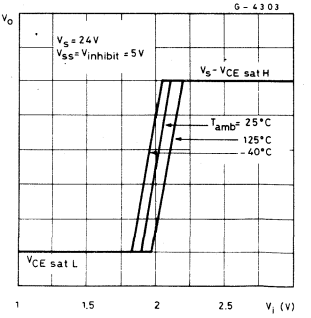
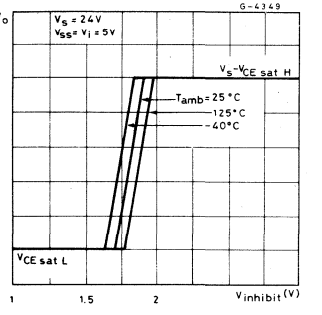
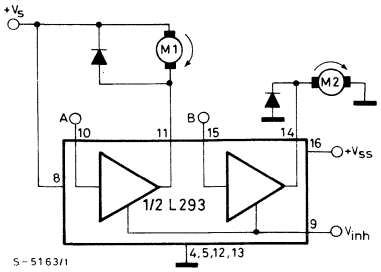


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION

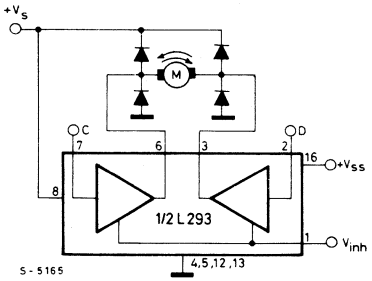
Fig. 8 - DC motor controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

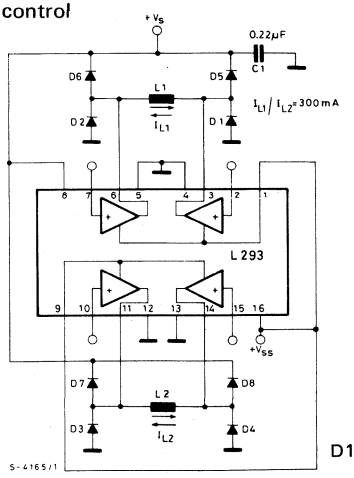
Fig. 9 - Bidirectional DC motor control



INPUTS		FUNCTION
V_{inh}= H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh}= L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

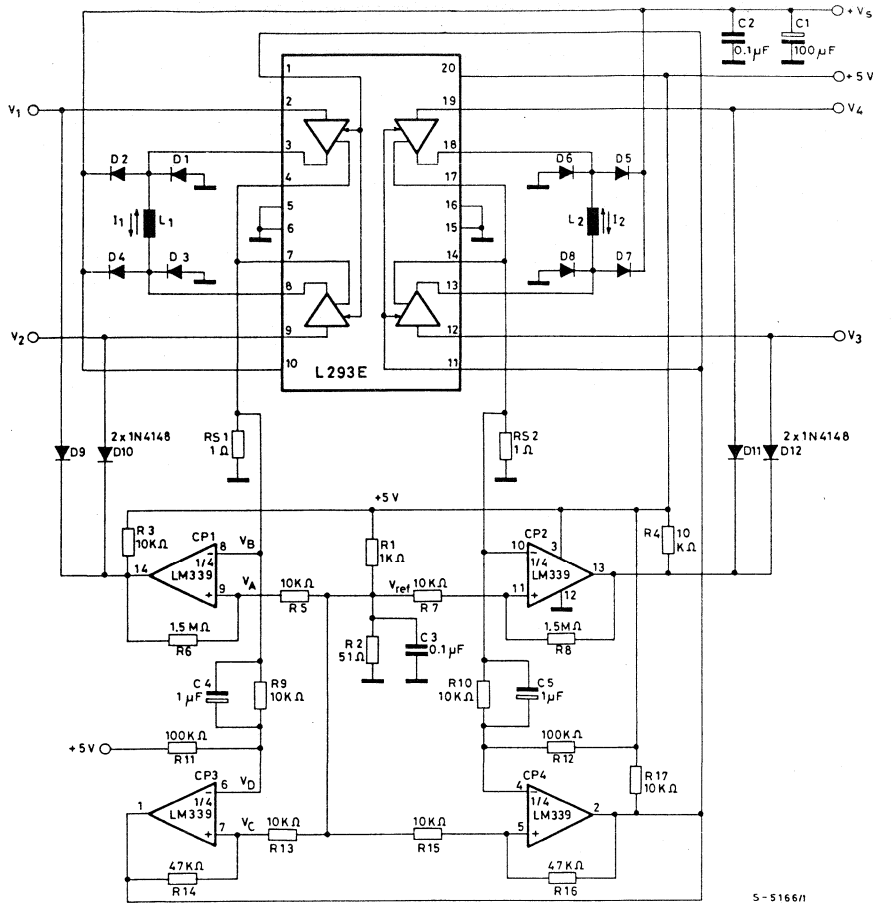
Fig. 10 - Bipolar stepping motor control



D1 - D8 = { $V_F \leqslant 1.2V$ @ I = 300 mA; trr $\leqslant$ 500 ns

APPLICATION INFORMATION (continued)

Fig. 11 - Stepping motor driver with phase current control and short circuit protection



D1 to D8 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 300 \text{ mA} \\ trr \leqslant 200 \text{ ns} \end{cases}$

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink

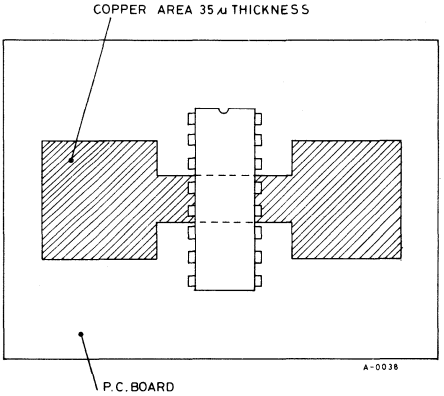
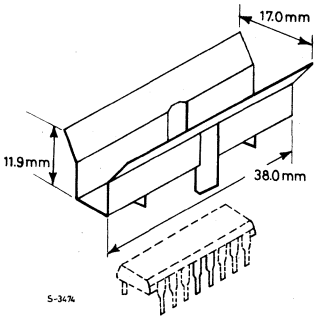


Fig. 13 - External heatsink mounting example (R_{th} = 30 °C/W)



PUSH-PULL FOUR CHANNEL/DUAL H-BRIDGE DRIVER

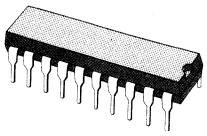
PRELIMINARY DATA

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- SEPARATE HIGH VOLTAGE POWER SUPPLY (UP TO 44V)

The L293C is a monolithic high voltage, high current integrated circuit four channel driver in a 20 pin DIP. It is designed to accept standard TTL or DTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.

The device may easily be used as a dual H-bridge driver: separate chip enable and high voltage power supply pins are provided for each H-bridge. In addition, a separate power supply is provided for the logic section of the device. This device is suitable for use in switching applications at frequencies up to 5 kHz.

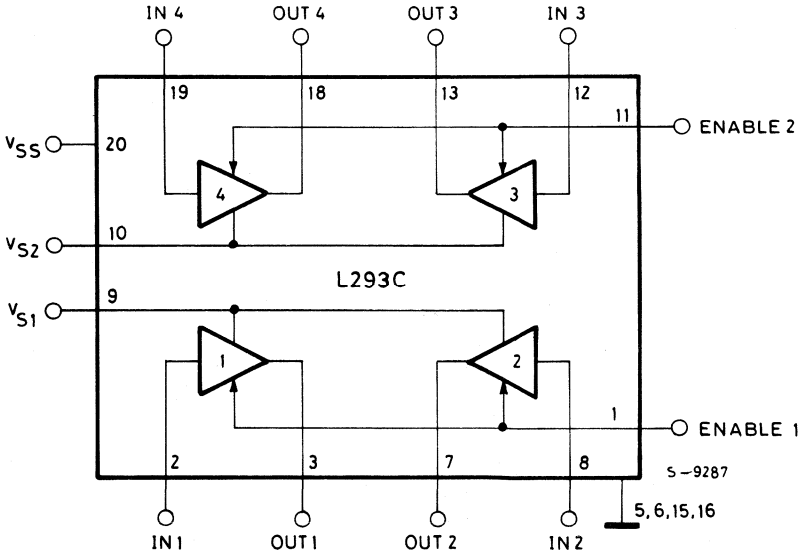
The L293C is assembled in a 20 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
(16+2+2)

ORDER CODE: L293C

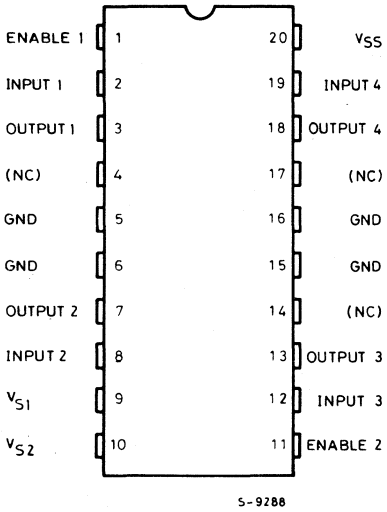
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_I	Input voltage	7	V
V_{EN}	Enable voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	1.2	A
P_{tot}	Total power dissipation at $T_{ground\text{-}pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

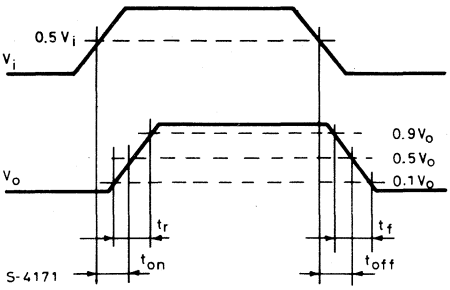


TRUTH TABLE

INPUT	ENABLE	OUTPUT
H	H	H
L	H	L
X	L	Z

Z = High output impedance
X = Don't care

SWITCHING TIMES



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S = 24V, V_{SS} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 9, 10)		V_{SS}		44	V
V_{SS}	Logic supply voltage (pin 20)		4.5		7	V
I_S	Total quiescent supply current (pin 9, 10)	V_i = L; I_o = 0; V_{EN} = H		2	6	mA
		V_i = H; I_o = 0; V_{EN} = H		16	24	
		V_{EN} = L			4	
I_{SS}	Total quiescent logic supply current (pin 20)	V_i = L; I_o = 0; V_{EN} = H		44	60	mA
		V_i = H; I_o = 0; V_{EN} = H		16	22	
		V_{EN} = L		16	24	
V_{IL}	Input low voltage (pin 2, 8, 12, 19)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 8, 12, 19)		2.3		V_{SS}	V
I_{IL}	Low voltage input current (pin 2, 8, 12, 19)	V_i = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 8, 12, 19)	$2.3V \leqslant V_i \leqslant V_{SS} - 0.6V$		30	100	μA
V_{ENL}	Enable low voltage (pin 1, 11)		-0.3		1.5	V
V_{ENH}	Enable high voltage (pin 1, 11)		2.3		V_{SS}	V
I_{ENL}	Low voltage enable current (pin 1, 11)	V_{ENL} = 1.5V		-30	-100	μA
I_{ENH}	High voltage enable current (pin 1, 11)	$2.3V \leqslant V_{ENH} \leqslant V_{ss} - 0.6$			± 10	μA
$V_{CE(sat)H}$	Source output saturation voltage (pins 3, 7, 13, 18)	I_o = -0.6A		1.4	1.8	V
$V_{CE(sat)L}$	Sink output saturation voltage (pins 3, 7, 13, 18)	I_o = +0.6A		1.2	1.8	V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

(*) See switching times diagram

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

PRELIMINARY DATA

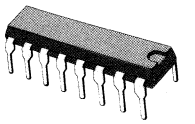
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON RE-PETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VILTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

The L293D is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

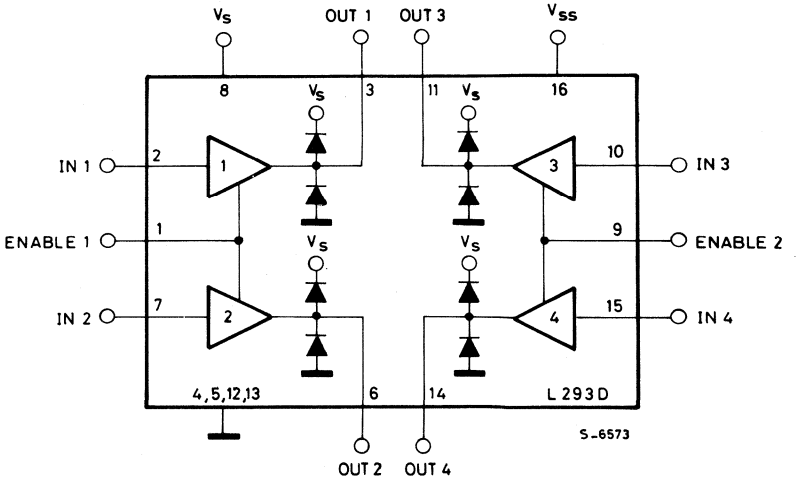
The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip 12+2+2

ORDERING NUMBER: L293D

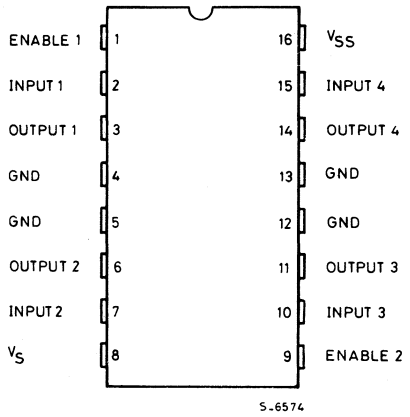
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	36	V
V_{SS}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{en}	Enable voltage	7	V
I_o	Peak output current (100μs non repetitive)	1.2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$= 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_s = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 8)		V_{ss}		36	V
V_{ss}	Logic supply voltage (pin 16)		4.5		36	V
I_s	Total quiescent supply current (pin 8)	V_i = L I_o = 0 V_{en} = H		2	6	mA
		V_i = H I_o = 0 V_{en} = H		16	24	
		V_{en} = L			4	
I_{ss}	Total quiescent logic supply current (pin 16)	V_i = L I_o = 0 V_{en} = H		44	60	mA
		V_i = H I_o = 0 V_{en} = H		16	22	
		V_{en} = L		16	24	
V_{IL}	Input low voltage (pin 2, 7, 10, 15)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 7, 10, 15)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{IL}	Low voltage input current (pin 2, 7, 10, 15)	V_{IL} = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 7, 10, 15)	$2.3V \leq V_{IH} \leq V_{ss} - 0.6V$		30	100	μA
V_{enL}	Enable low voltage (pin 1, 9)		-0.3		1.5	V
V_{enH}	Enable high voltage (pin 1, 9)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{enL}	Low voltage enable current current (pin 1, 9)	V_{enL} = 1.5V		-30	-100	μA
i_{enH}	High voltage enable current (pin 1, 9)	$2.3V \leq V_{enH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage (pins 3, 6, 11, 14)	I_o = - 0.6A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage (pins 3, 6, 11, 14)	I_o = + 0.6A		1.2	1.8	V
V_F	Clamp diode forward voltage	I_o = 600 mA		1.3		V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

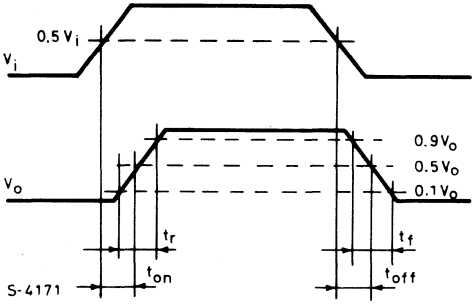
(*) See fig. 1

TRUTH TABLE (One channel)

INPUT	ENABLE (*)	OUTPUT
H	H	H
L	H	L
H	L	Z
L	L	Z

Z = High output impedance
(*) Relative to the considered channel

Fig. 1 - Switching Times



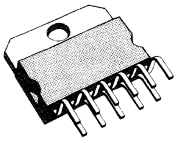
SWITCH-MODE SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUPTPUT CURRRENT CAPABILITY (UP TO 4A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

DESCRIPTION

The L294 is a monolithic switchmode solenoid driver designed for fast, high-current applications such as hammer and needle driving in printers and electronic typewriters. Power dissipation is reduced by efficient switchmode operation. An extra feature of the L294 is a latched diagnostic output which indicates when the output is short circuited.

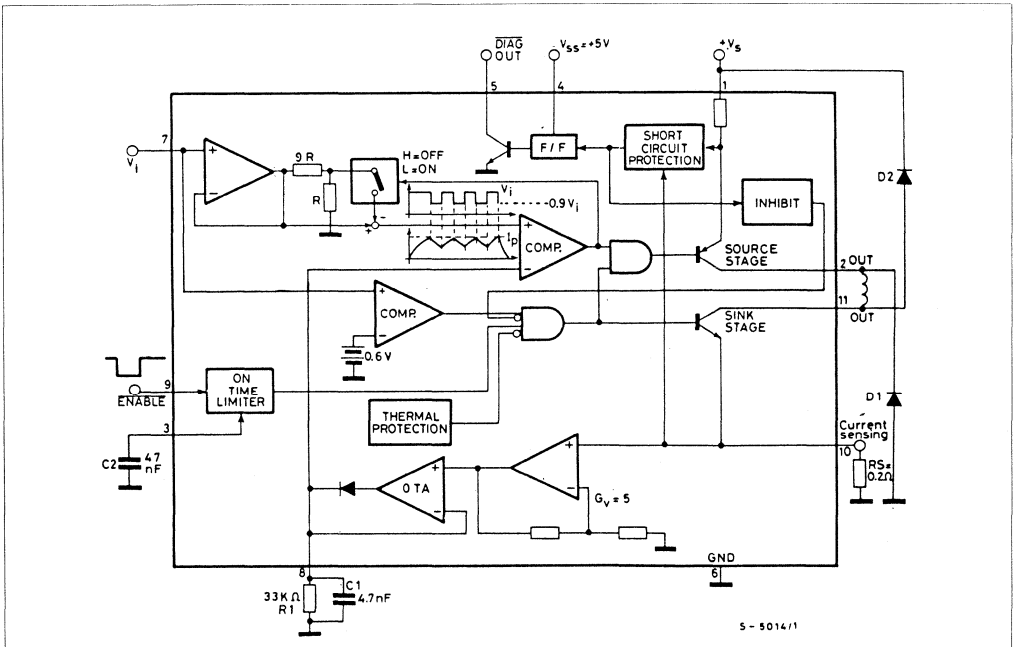
The L294 is supplied in a 11-lead Multiwatt ® plastic power package.



Multiwatt 11

ORDER CODE : L294

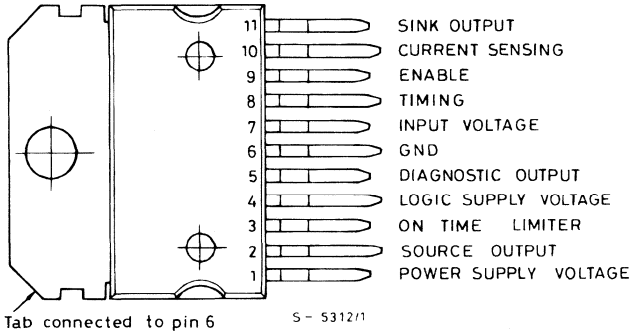
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage	50	V
V_{ss}	Logic Supply Voltage	7	V
V_{EN}	Enable Voltage	7	V
V_i	Input Voltage	7	V
I_p	Peak Output Current (repetitive)	4.5	A
P_{tot}	Total Power Dissipation (at T_{case} = 75°C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_S = 40V , V_{SS} = 5V , T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Power Supply Voltage (pin 1)	Operative Condition	12		46	V
I_d	Quiescent Drain Current (pin 1)	V_{ENABLE} = H		20	30	mA
		$V_i \geq 0.6V$; V_{ENABLE} = L		70		
V_{SS}	Logic Supply Voltage (pin 4)		4.5		7	V
I_{SS}	Quiescent Logic Supply Current	V_{DIAG} = L		5	8	mA
		DIAG Output at High Impedance		10	100	µA
V_i	Input Voltage (pin 7)	Operating Output	0.6			V
		Non-operative Output			0.45	
I_i	Input Current (pin 7)	$V_i \geq 0.6V$		– 1		µA
		$V_i \leq 0.45V$		– 3		
V_{ENABLE}	Enable Input Voltage (pin 9)	Low Level	– 0.3		0.8	V
		High Level	2.4			
I_{ENABLE}	Enable Input Current (pin 9)	V_{ENABLE} = L			– 100	µA
		V_{ENABLE} = H			100	
I_{load}/V_i	Transconductance	R_s = 0.2Ω V_i = 1V	0.95	1	1.05	A/V
		V_i = 4V	0.97	1	1.03	
$V_{sat\ H}$	Source Output Saturation Voltage	I_p = 4A		1.7		V
$V_{sat\ L}$	Sink Output Saturation Voltage	I_p = 4A		2		V
$V_{sat\ H}$+ $V_{sat\ L}$	Total Saturation Voltage	I_p = 4A			4.5	V
$I_{leakage}$	Output Leakage Current	R_s = 0.2Ω ; $V_i \leq 0.45V$		1		mA
K	On Time Limiter Constant (°)	V_{ENABLE} = L		120		
V_{DIAG}	Diagnostic Output Voltage (pin 5)	I_{DIAG} = 10 mA			0.4	V
I_{DIAG}	Diagnostic Leakage Current (pin 5)	V_{DIAG} = 40V			10	µA
$\frac{V_{pin\ 8}}{V_{pin\ 10}}$	OP AMP and OTA DC Voltage Gain (°°)	$V_{pin\ 10}$ = 100 to 800 mV		5		
V_{SENS}	Sensing Voltage (pin 10) (°°°)				0.9	V

(°) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(°°) See the block diagram.
(°°°) Allowed range of V_{SENS} without the intervention of the short circuit protection.

CIRCUIT OPERATION

The L294 works as a transconductance amplifier : it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see fig.1).

The following explanation refers to the Block Diagram, to fig.1 and to the typical application circuit of fig.2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible) : it is active low and enables the output stages "source" and "sink". At the end of t_{on}, the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_S, pin 1). During the t_{on} time, I_{load} is converter into a voltage signal by means of the external sensing resistance R_S connected to pin 10. This signal, amplified by the op amp and converted by the transconductance amplifier OTA, charges the external RC network at pin 8 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 7).

After t_r, the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D1.

Two cases are possible : the time constant of the recirculation phase is higher than R1.C1 ; the time constant is lower than R1.C1. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load}. In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1 C1 network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of R1.C1.

In other words, R1.C1 fixes the minimum value of t_1 ($t_1 \geq 1/10$ R1.C1. Note that C1 should be chosen in the range 2.7 to 10 nF for stability reasons of the OTA).

After t_1, the comparator switches again : the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again : t_2, t_4 and t_6 have the same characteristics as t_r, while t_3 and t_5 are similar to t_1. The peak current I_p depends on V_i as shown in the typical transfer function of fig.3.

It can be seen that for V_i lower than 450 mV the device is not operating.

For V_i greater than 600 mV, the L294 has a transconductance of 1A/V with $R_S = 0.2\Omega$. For V_i included between 450 and 600 mV, the operation is not guaranteed.

The order parts of the device have protection and diagnostic functions. At pin 3 is connected an external capacitor C2, charged at constant current when the Enable is low.

After a time interval equal to K · C2 (K is defined in the table of Electrical Characteristics and has the dimensions of ohms) the output stages are switched off independently by the Input signal.

This avoids the load being driven in conduction for an excessive period of time (overdriving protection). The action of this protection is shown in fig.1b. Note that the voltage ramp at pin 3 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 3 and to restore the normal conditions, pin 9 must return high.

This protection can be disabled by grounding pin 3.

The thermal protection included in the L294 has a hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

Finally, the device is protected against any type of short circuit at the outputs : to ground, to supply and across the load.

When the source stage current is higher than 5A and/or when the pin 10 voltage is higher then 1V (i.e. for a sink current greater than $1V/R_S$) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 5) ; the internal flip-flop F/F changes and forces the output transistor into saturation. The F/F must be supplied independently through V_{SS} (pin 4). The DIAG signal is reset and the output stages are still operative by switching off the supply voltage at pin 1 and then by switching the device on again. After that, two cases are possible : the reason for the "bad operation" is still present and the protection acts again ; the reason has been removed and the device starts to work properly.

Figure 1 : Output Current Waveforms.

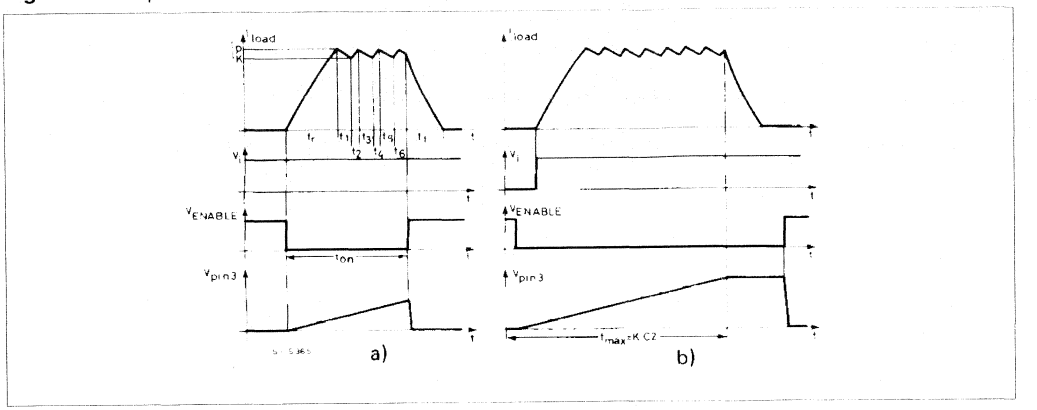
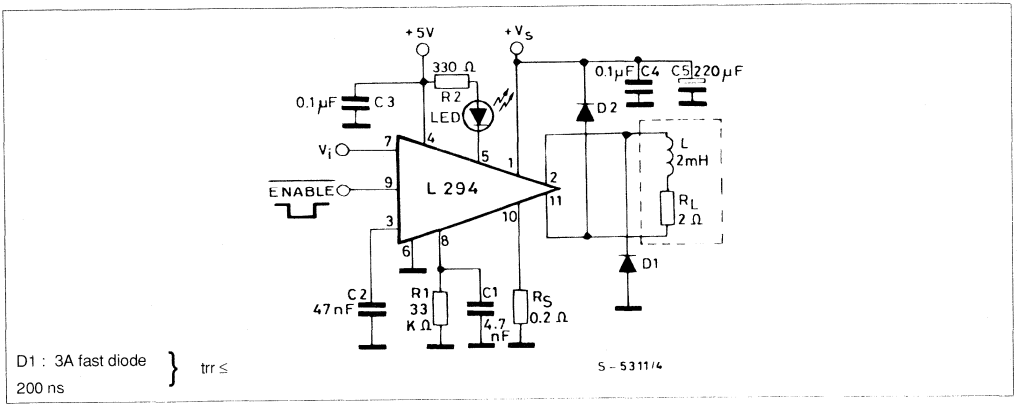


Figure 2 : Test and Typical Application Circuit.



D1 : 3A fast diode 200 ns } trr ≤

Figure 3 : Peak Output Current vs. Input Voltage.

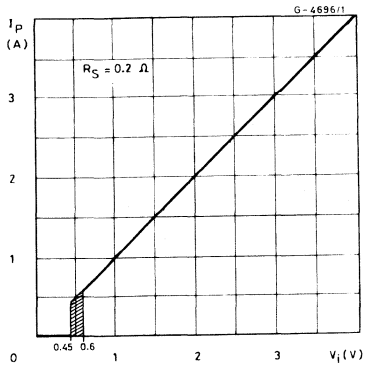


Figure 4 : Output Saturation Voltages vs. Peak Output Current.

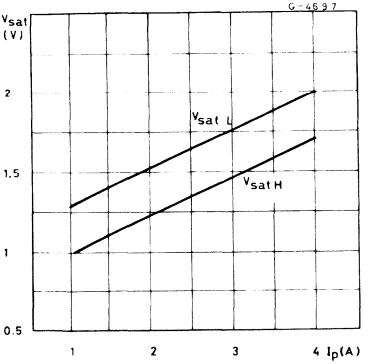


Figure 5 : Safe Operating Areas.

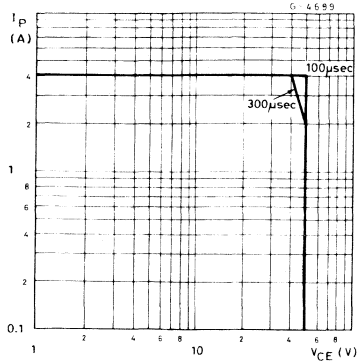
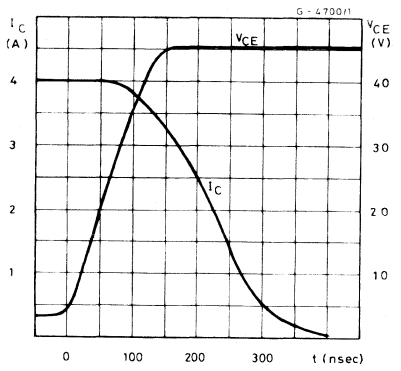


Figure 6 : Turn-off Phase.



CALCULATION OF THE SWITCHING TIMES

Referring to the block diagram and to the waveforms of fig.1, it is possible to calculate the switching times by means of the following relationships.

$$t_r = -\frac{L}{R_L} \ln\left(1 - \frac{R_L}{V1} \cdot I_p\right)$$

where : $V1 = V_S - V_{sat\,L} - V_{sat\,H} - V_{R\,sens}$

$$t_f = -\frac{L}{R_L} \ln\frac{V2}{V2 + R_L \cdot I_o}$$

Where : $V2 = V_S + V_{D1} + V_{D2}$

$I_K \leq I_o \leq I_p$

I_o is the value of the load current at the end of t_{on}.

$$t_1 = t_3 = t_5 = \ldots = \begin{cases} \text{a)} -\dfrac{L}{R_L} \ln\dfrac{0.9\, I_p \cdot R_L + V3}{I_p R_L + V3} \\ \text{b)} -R1\,C1 \ln 0.9 \cong \dfrac{1}{10} R1\,C1 \end{cases}$$

where $V3 = V_{sat\,L} + V_{R\,sens} + V_{D1}$

$$t_2 = t_4 = t_6 = \ldots = -\frac{L}{R_L} \ln\left(\frac{V1 - I_p R_L}{V1 - I_K R_L}\right)$$

Note that the time interval $t_1 = t_3 = t_5 = \ldots$ takes the longer value between case a) and case b). The switching frequency is always :

$$f_{switching} = \frac{1}{t_1 + t_2}$$

In the case a) the main regulation loop is always closed and it forces :

$$I_K = (0.9 \pm S)\, I_p$$

where : S = 3 % @ V_i = 1 V
S= 1.5 % @ V_i = 4 V

In the case b), the same loop is open in the recirculation phase and I_K, which is always lower than 0.9 I_p, is obtained by means of the following relationship.

$$I_K = I_p\, e^{-\frac{t_1 R_L}{L}} - \frac{V3}{R_L}\left(1 - e^{-\frac{t_1 R_L}{L}}\right)$$

With the typical application circuit, in the conditions V_S = 40V, I_p = 4A, the following switching times result :

t_r = 255 µs $\quad$ t_f = 174 µs @ $I_o = I_p$

t_1 = a) 70 µs
b) 16 µs $\quad$ t_2 = 29 µs $\quad$ f=10.2 KHz

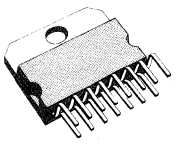
DUAL SWITCH-MODE SOLENOID DRIVER

PRELIMINARY DATA

- HIGH CURRENT CAPABILITY (up to 2.5A per channel)
- HIGH VOLTAGE OPERATION (up to 46V for power stage)
- HIGH EFFICIENCY SWITCHMODE OPERATION
- REGULATED OUTPUT CURRENT (adjustable)
- FEW EXTERNAL COMPONENTS
- SEPARATE LOGIC SUPPLY
- THERMAL PROTECTION

The L295 is a monolithic integrated circuit in a 15 - lead Multiwatt ® package ; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels at the inputs and can drive 2 solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and dual supplies (for interfacing with peripherals running at a higher voltage than the logic).

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.



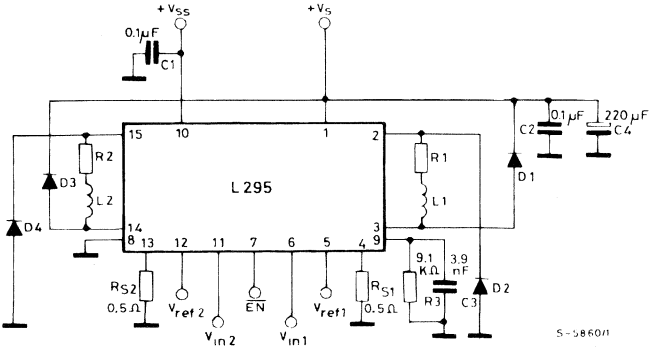
Multiwatt 15

ORDER CODE : L295

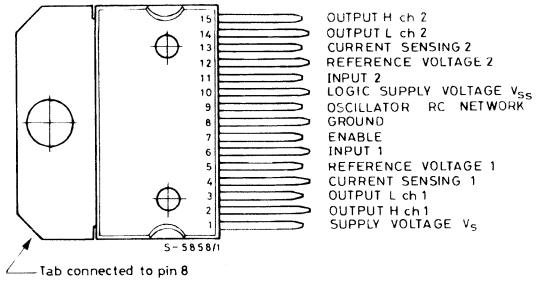
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	12	V
V_{EN}, V_i	Enable and input voltage	7	V
V_{ref}	Reference voltage	7	V
I_o	Peak output current (each channel)		
	– non repetitive (t = 100 µsec)	3	A
	– repetitive (80 % on – 20 % off ; T_{on} = 10 ms)	2.5	A
	– DC operation	2	A
P_{tot}	Total power dissipation (at T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

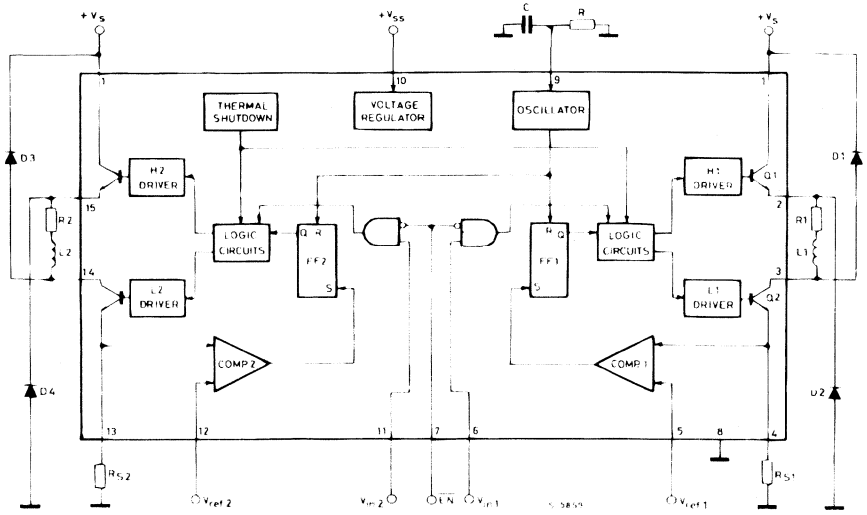
APPLICATION CIRCUIT



CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



THERMAL DATA

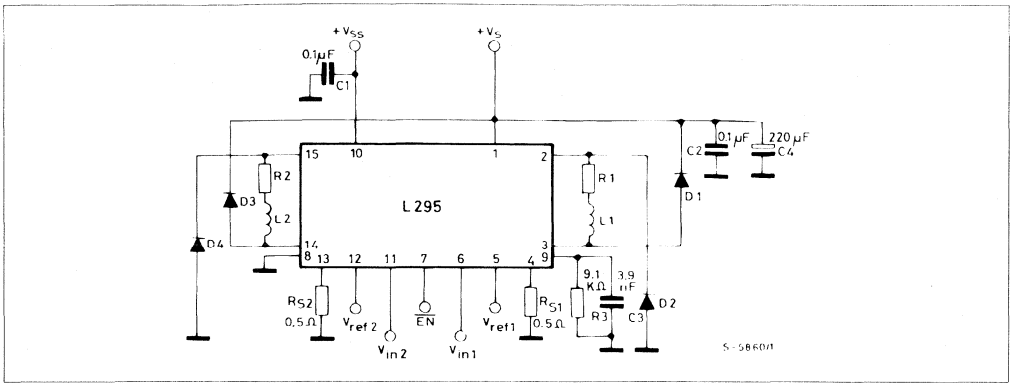
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	C/W

ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{SS} = 5V, V_S = 36V; T_j = 25°C; L = low; H = high; unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage			12		46	V
V_{SS}	Logic Supply Voltage			4.75		10	V
I_d	Quiescent drain current (from VSS)	V_S = 46 V; V_{i1} = V_{i2} = V_{EN} = L				4	mA
I_{ss}	Quiescent drain current (from VS)	V_{SS} = 10 V				46	mA
V_{i1}, V_{i2}	Input Voltage		Low	− 0.3		0.8	V
			High	2.2		7	
V_{EN}	Enable Input Voltage		Low	− 0.3		0.8	V
			High	2.2		7	
I_{i1}, I_{i2}	Input Current		V_{i1} = V_{i2} = L			− 100	µA
			V_{i1} = V_{i2} = H			10	
I_{EN}	Enable Input Current		V_{EN} = L			− 100	µA
			V_{EN} = H			10	
V_{ref1}, V_{ref2}	Input Reference Voltage			0.2		2	V
I_{ref1}, I_{ref2}m	Input Reference Voltage					− 5	µA
F_{osc}	Oscillation Frenquency	C = 3.9 nF ;	R = 9.1 KΩ		25		KHz
$\frac{I_p}{V_{ref}}$	Transconductance (each ch.)	V_{ref} = 1 V	R_S = 0.5Ω	1.9	2	2.1	A/V
V_{drop}	Total output voltage drop (each channel) (*)	I_O = 2 A			2.8	3.6	V
V_{sens1} V_{sens2}	External sensing resistors voltage drop					2	V

(*) V_{drop} = $V_{CEsat\ Q1}$ + $V_{CEsat\ Q2}$.

APPLICATION CIRCUIT



D2, D4 = 2A High speed diodes
D1, D3 = 1A High speed diodes) trr ≤ 200 ns

R1 = R2 = 2Ω
L1 = L2 = 5 mH

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are :

$\overline{EN}$ chip enable (digital input,active low) , enables both channels when in the low state.

V_{in1}, V_{in2} channel inputs (digital inputs,active high), enable each channel independently. A channel is actived when both $\overline{EN}$ and the appropriate channel input are active.

V_{ref1}, V_{ref2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{ref}.

Since the two channels are identical, only channel one will be described.

The following description applies also the channel two, replacing FF2 for FF1, V_{ref2} for V_{ref1} etc.

When the channel is activated by a low level on the EN input and a high level on the channel input, V_{in2}, the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law :

$$I = \frac{V}{R1}\left(1 - e^{\frac{-R1\,t}{L1}}\right)$$

where : R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load ($V_s - V_{drop} - V_{sense}$).

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{ref1}. This peak current, I_{p1}, is given by :

$$I_{p1} = \frac{V_{ref1}}{R_{S1}}$$

At this point the comparator output, Comp1, sets the RS flip–flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law :

$$I = \left(\frac{V_A}{R1} + I_{p1}\right) e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where $V_A = V_{CEsat\,Q2} + V_{sense\,1} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in fig. 1.

At the time t_2 the channel 1 is disabled, by taking the inputs V_{in1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law :

$$I = \left(\frac{V_B}{R1} + I_{T2} \right) e^{\frac{-R1\,t}{L1}} - \frac{V_B}{R1}$$

where $V_B = V_S + V_{D1} + V_{D2}$

I_{T2} = current value at the time t_2.

Fig. 2 in shows the current waveform obtained with an RC network connected between pin 9 and ground. From to t_1 the current increases as in fig. 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the outout transistor, Q1. The current increases until the drop on the sensing resistor R_{s1} is equal to V_{ref1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in fig. 4 and must be chosen in the range 10 to 30 KHz.

It is possible with external hardware to change the reference voltage V_{ref} in order to obtain a high peak current I_p and a lower holding current I_h (see fig.3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150 °C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20 °C.

The analog input pins (V_{ref1}, V_{ref2}) can be left open or connected to V_{ss} ; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_S :

$$I_p = \frac{2.5}{R_S}$$

SIGNAL WAVEFORMS

Figure 1 : Load current waveform with pin 9 connected to GND.

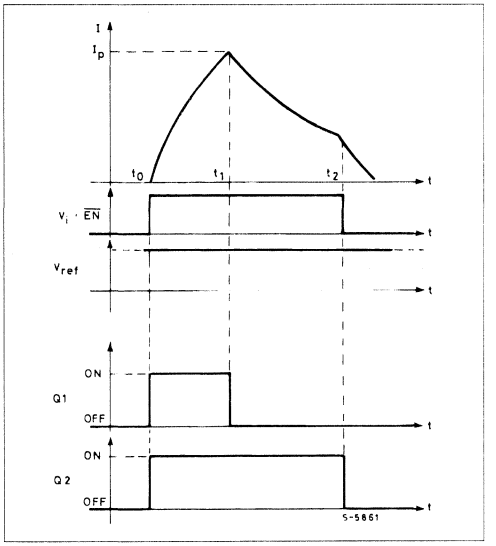
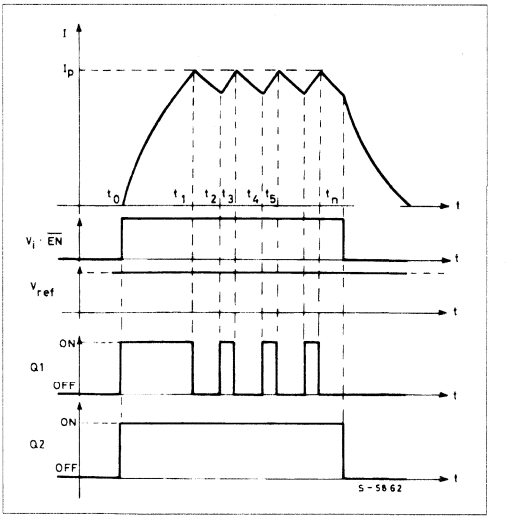


Figure 2 : Load current waveform with external R–C network connected between pin 9 and ground.



SIGNAL WAVEFORMS (continued)

Figure 3 : With V_{ref} changed by hardware.

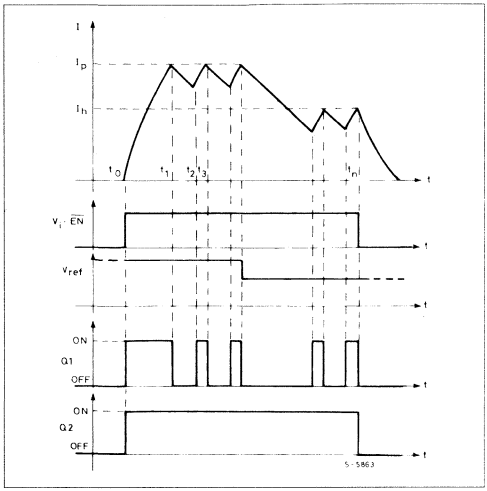
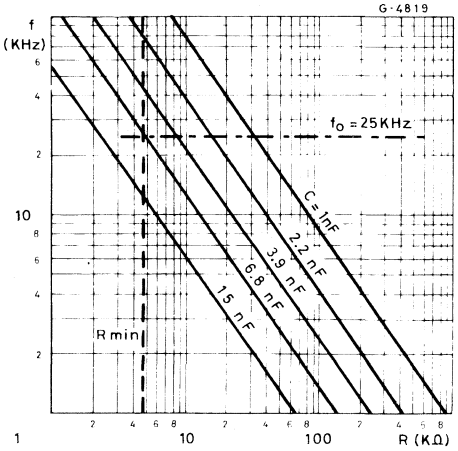


Figure 4 : Switching frequency vs. values of R and C.



HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

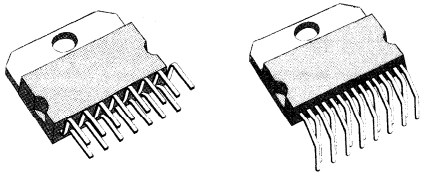
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

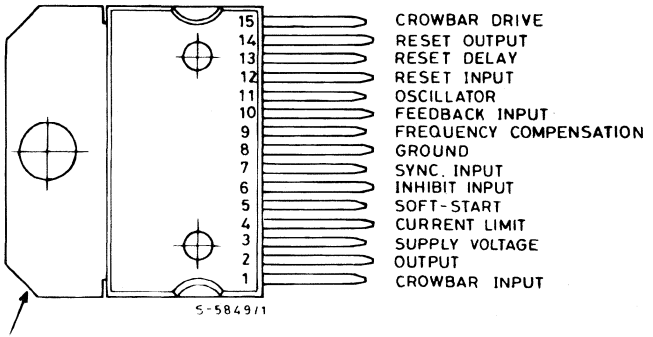
Multiwatt®
(15-lead)



ORDER CODES :

L296	L296HT
L296P	L296PHT

PIN CONNECTION (top view)



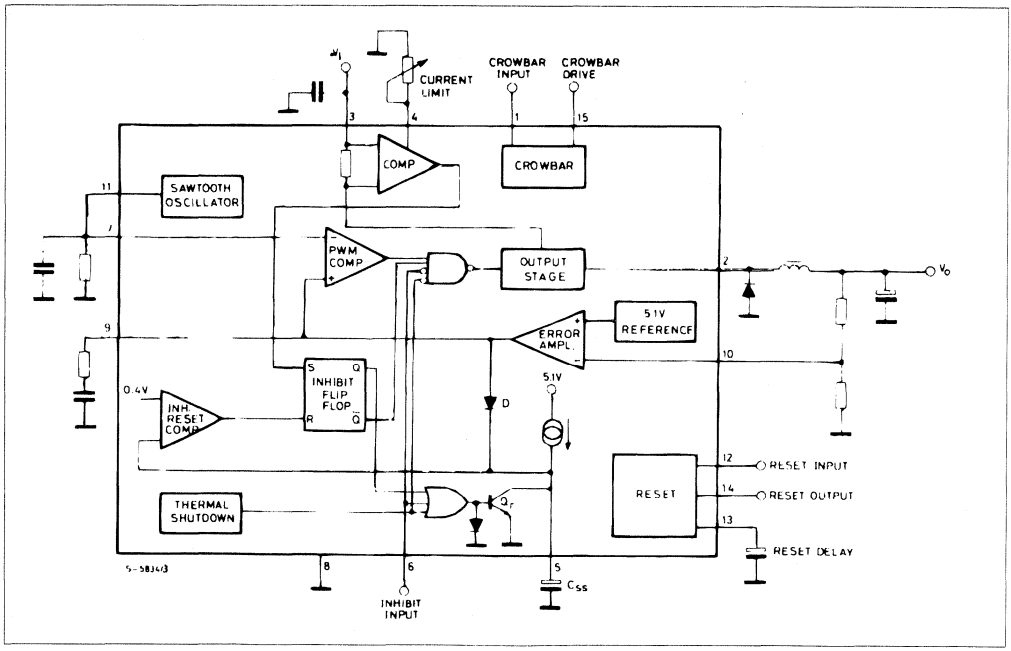
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	– 1 – 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1 V to 40 V and delivering 4 A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

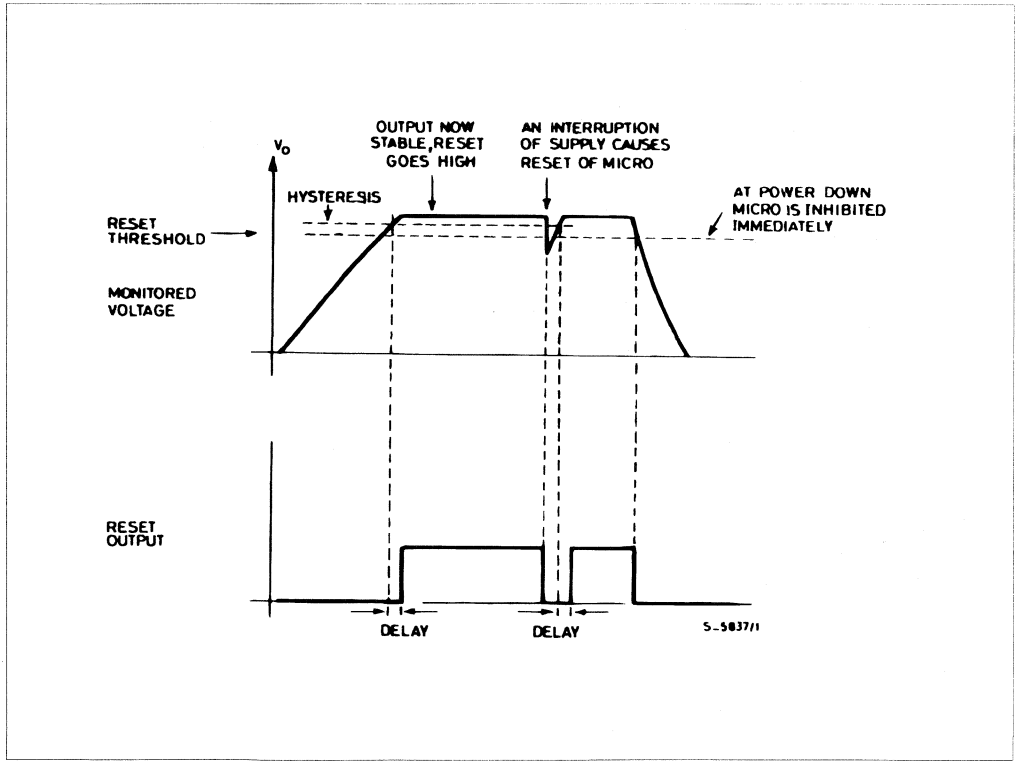
The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20 %. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.



CIRCUIT OPERATION (continued)

Figure 2 : Soft Start Waveforms.

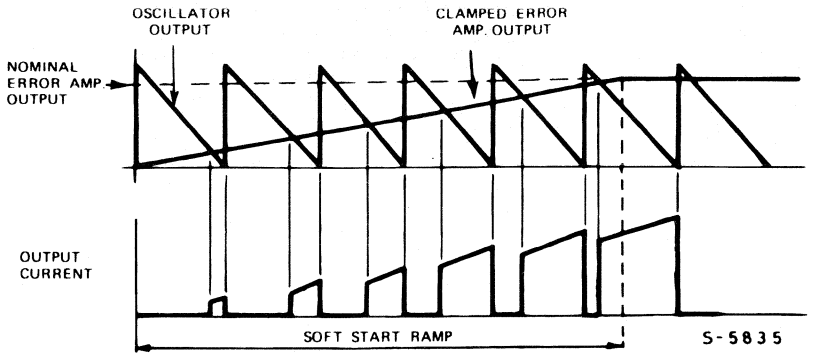
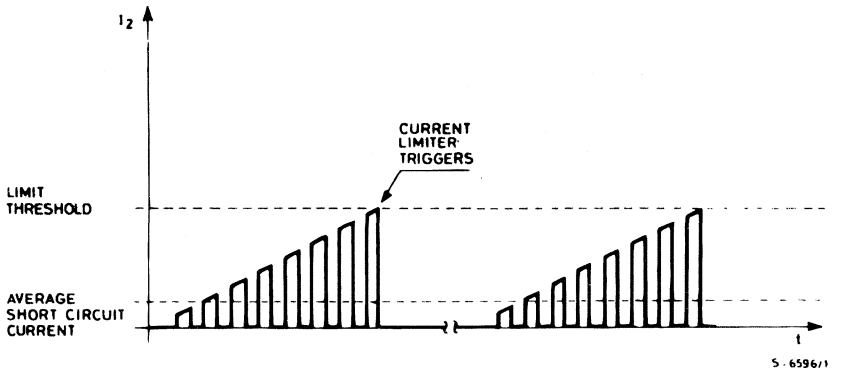


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 35 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)							
V_o	Output Voltage Range	V_i = 46 V I_o = 1 A	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36 V $I_o \leq$ 3 A	9		46	V	4
V_i	Input Voltage Range	Note (1) $V_o = V_{REF}$ to 36 V I_o = 4 A			46	V	4
ΔV_o	Line Regulation	V_i =10 V to 40 V, $V_o = V_{ref}$, I_o = 2 A		15	50	mV	4
ΔV_o	Load Regulation	I_o = 2 A to 4 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 4 A		15	45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 46 V I_o = 2 A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4 A		2	3.2	V	4
		I_o = 2 A		1.3	2.1	V	4
I_{2L}	Current Limiting Threshold (pin 2)	L296 Pin 4 Open V_i = 9 V to 40 V $V_o = V_{ref}$ to 36 V	4.5		7.5	A	4
		L296P Pin 4 Open	5		7	A	4
		V_i = 9 V to 40 V $V_o = V_{ref}$ R_{lim} = 22 KΩ	2.5		4.5	A	4
I_{SH}	Input Average Current	V_i = 46 V; Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$		75		%	4
		V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms} f_{ripple} = 100 Hz $V_o = V_{ref}$ I_o = 2 A	50	56		dB	4
f	Switching Frequency		85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 46 V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; I_o = 1 A	200			KHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	V_i = 46 V V_7 = 0 V V_6 = 0 V		66	85	mA	6a
		S1 : B S2 : B V_6 = 3V		30	40	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 46 V, V_6 = 3 V, S1 : B, S2 : A, V_7 = 0 V			2	mA	6a

Note (1) : Using min. 7 A schottky diode.
(2) : Guaranteed by design, not 100 % tested in production.

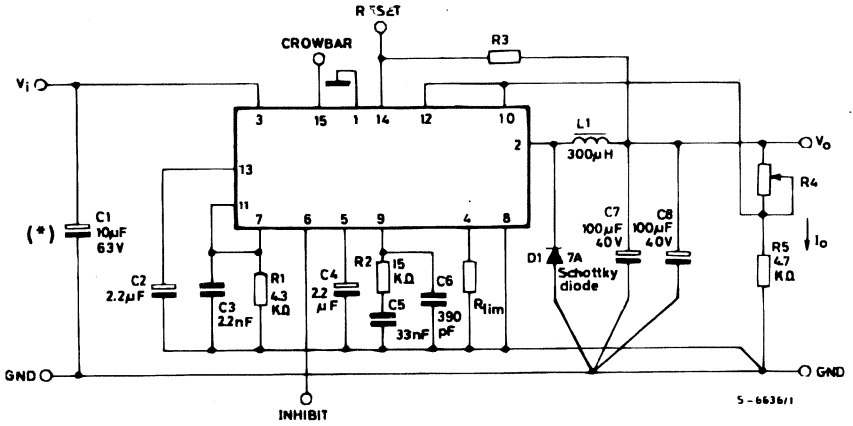
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SOFT START								
$I_{5\,so}$	Source Current	$V_6 = 0$ V, $V_5 = 3$ V		80	130	150	µA	6b
$I_{5\,si}$	Sink Current	$V_6 = 3$ V, $V_5 = 3$ V		50	70	120	µA	6b
INHIBIT								
V_{6L}	Low Input Voltage	$V_i = 9$ V to 46 V	S1 : B S2 : B	− 0.3		0.8	V	6a
V_{6H}	High Input Voltage	$V_7 = 0$ V		2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	$V_i = 9$ V to 46 V	$V_6 = 0.8$ V			10	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	$V_7 = 0$ V S1 : B S2 : B	$V_6 = 2$ V			3	µA	6a
ERROR AMPLIFIER								
V_{9H}	High Level Output Voltage	$V_{10} = 4.7$ V, $I_9 = 100$ µA,	S1 : A, S2 : A	3.5			V	6c
V_{9L}	Low Level Output Voltage	$V_{10} = 5.3$ V, $I_9 = 100$ µA,	S1 : A, S2 : E			0.5	V	6c
$I_{9\,si}$	Sink Output Current	$V_{10} = 5.3$ V,	S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	$V_{10} = 4.7$ V,	S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	$V_{10} = 5.2$ V,	S1 : B		2	10	µA	6c
		$V_{10} = 6.4$ V,	S1 : B, L296P		2	10	µA	6c
G_v	DC Open Loop Gain	$V_9 = 1$ V to 3 V,	S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR								
$-I_7$	Input Bias Current of PWM Comparator	$V_7 = 0.5$ V to 3.5 V				5	µA	6a
$-I_{11}$	Oscillator Source Current	$V_{11} = 2$ V,	S1 : A S2 : B	5				mA
RESET								
$V_{12\,R}$	Rising Threshold Voltage	$V_i = 9$ V to 46 V,	S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling Threshold Voltage			4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay Threshold Voltage	$V_{12} = 5.3$ V,	S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay Threshold Voltage Hysteresis				100		mV	6d
$V_{14\,S}$	Output Saturation Voltage	$I_{14} = 16$ mA; $V_{12} = 4.7$ V;	S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	$V_{12} = 0$ V to V_{ref},	S1 : B, S2 : B		1	3	µA	6d
$-I_{13\,so}$	Delay Source Current	$V_{13} = 3$ V S1 : A S2 : B	$V_{12} = 5.3$ V	70	110	140	µA	6d
$I_{13\,si}$	Delay Sink Current		$V_{12} = 4.7$ V	10			mA	6d
I_{14}	Output Leakage Current	$V_i = 46$ V, $V_{12} = 5.3$ V,	S1 : B, S2 : A			100	µA	6d

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
CROWBAR								
V_1	Input Threshold Voltage	S1 : B		5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9 V to 46 V, I_{15} = 5 mA	V_i = 5.4 V S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6 V,	S1 : B			10	µA	6b
$-I_{15}$	Output Source Current	V_i = 9 V to 46 V, V_{15} = 2 V	V_1 = 6.5 V S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations. Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale).

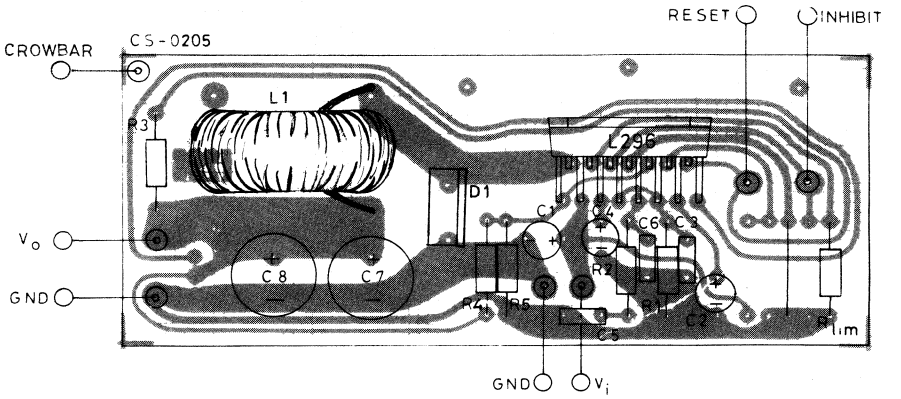


Figure 6 : DC Test Circuits.

Figure 6a.

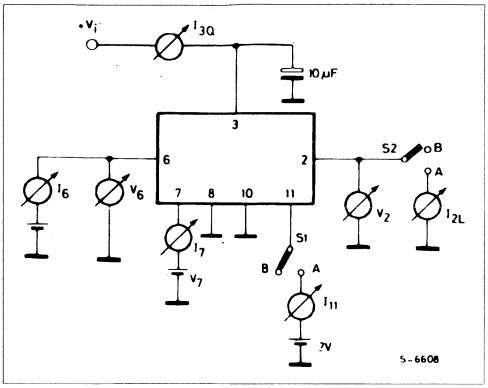


Figure 6b.

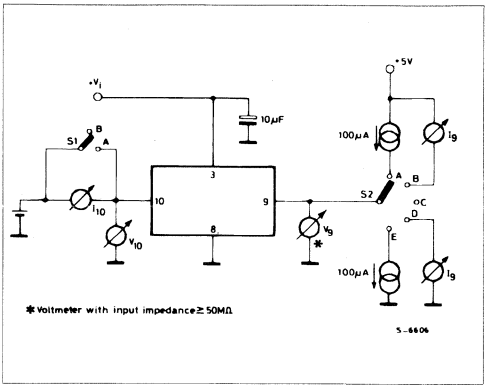


Figure 6c.

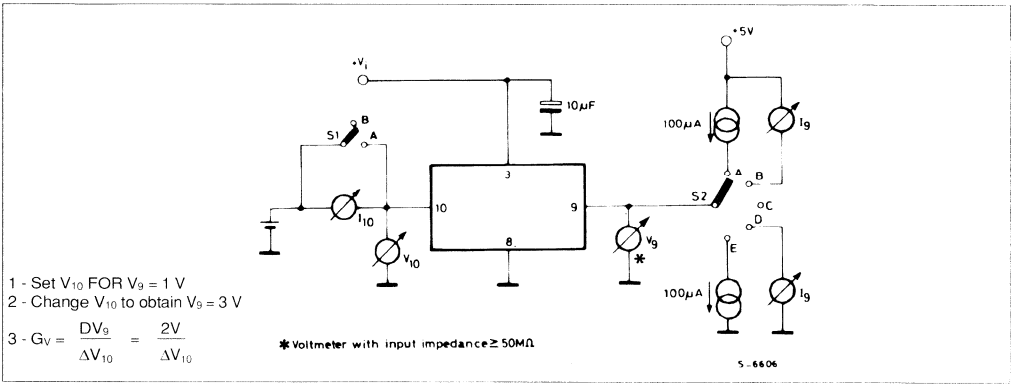


Figure 6d.

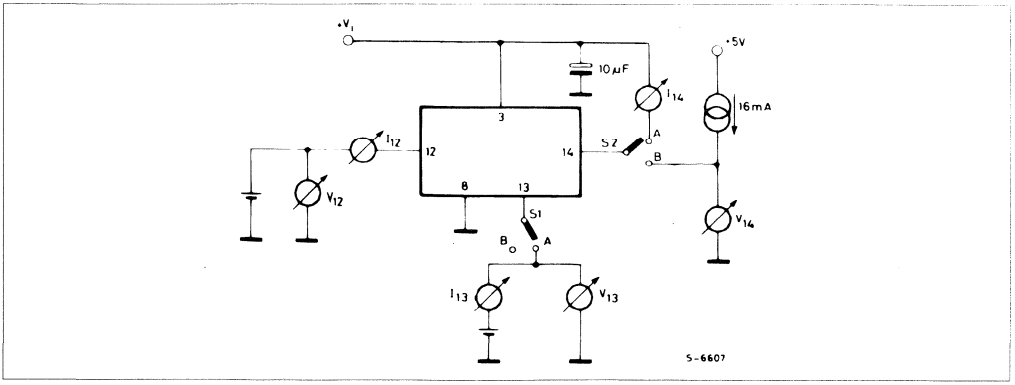


Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

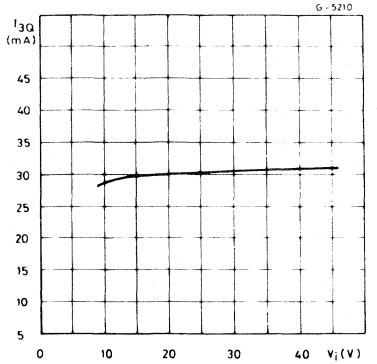


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

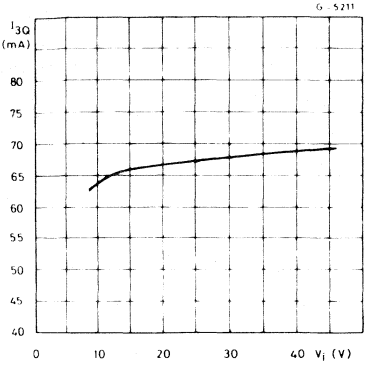


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

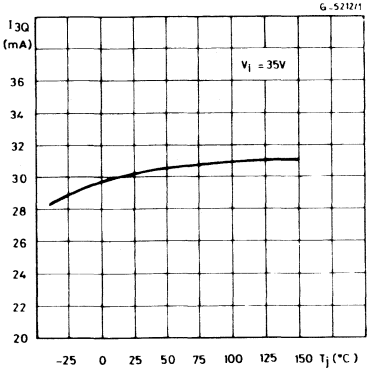


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

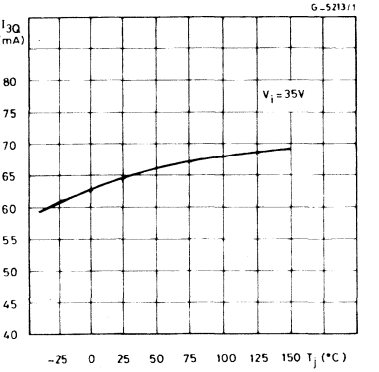


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

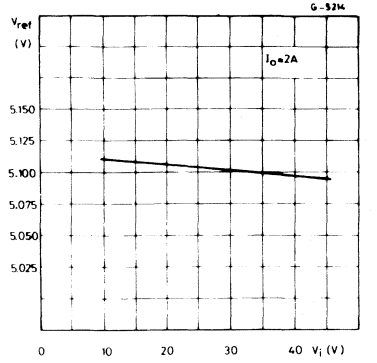


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

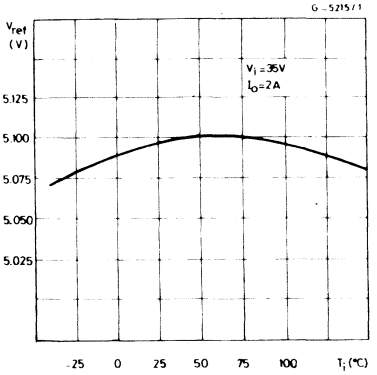


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

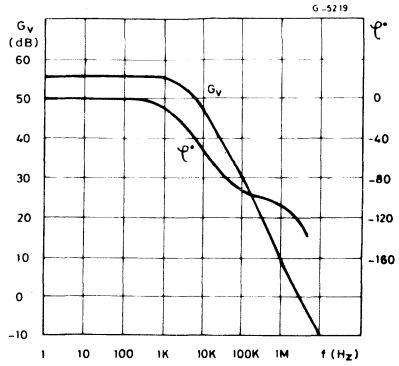


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

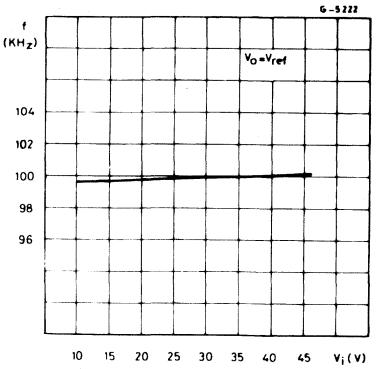


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

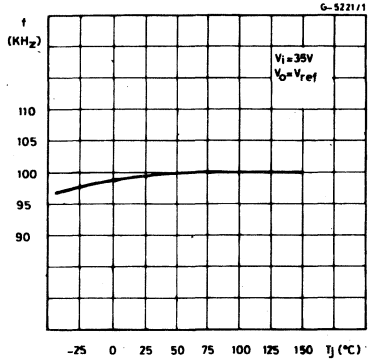


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

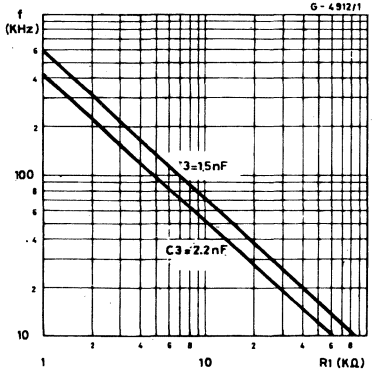


Figure 17 : Line Transient Response (see fig. 4).

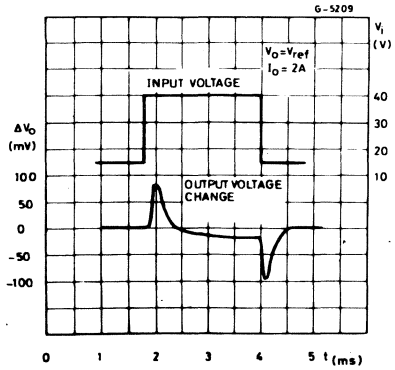


Figure 18 : Load Transient Response (see fig. 4).

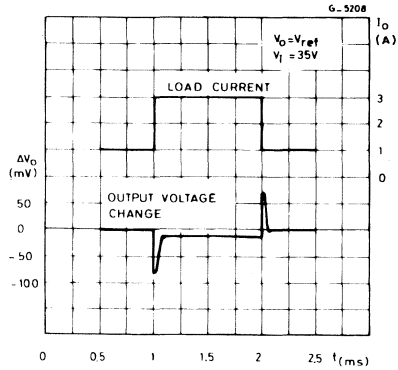


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

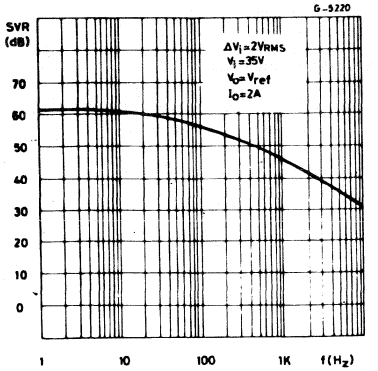


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

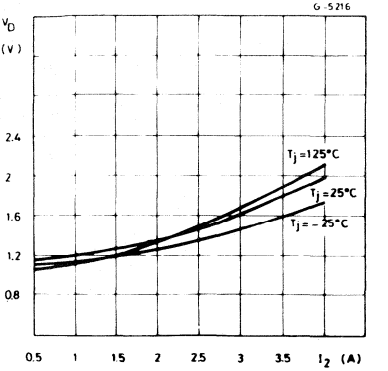


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

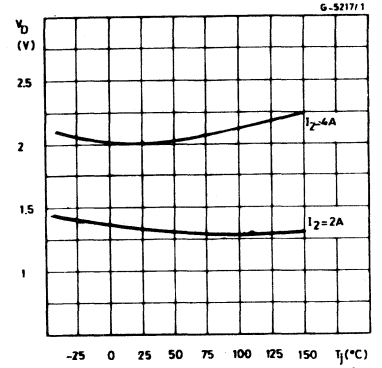


Figure 22 : Power Dissipation Derating Curve.

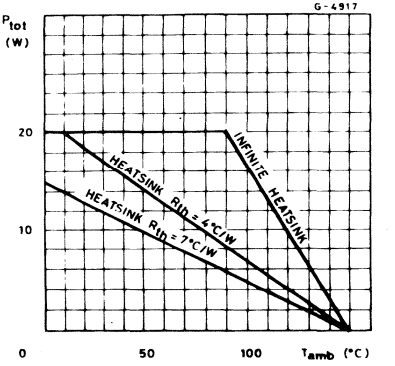


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

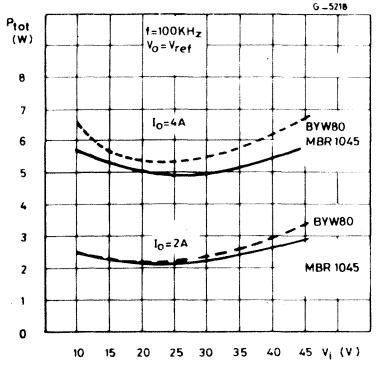


Figure 24 : Power Dissipation (device only) vs. Input voltage.

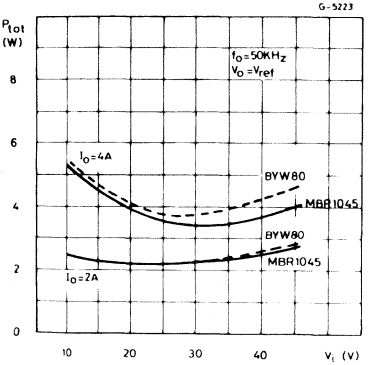


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

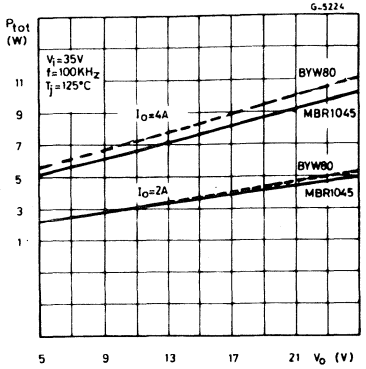


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

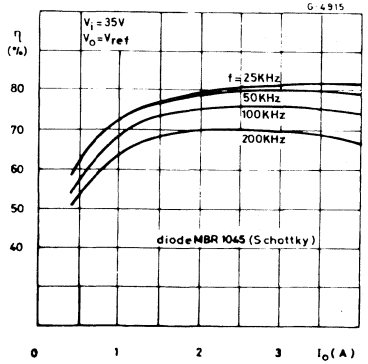


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

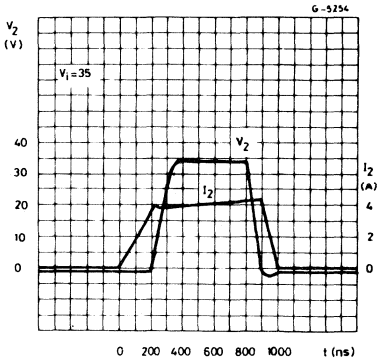


Figure 28 : Efficiency vs. Output Current.

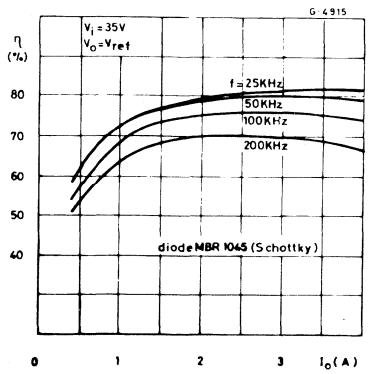


Figure 29 : Efficiency vs. Output Voltage.

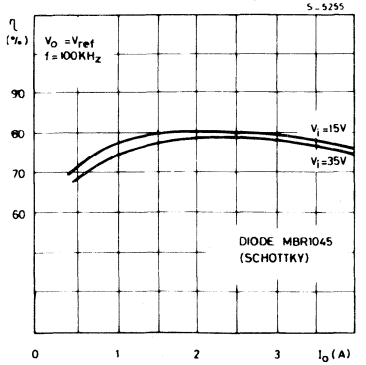


Figure 30 : Efficiency vs. Output Voltage.

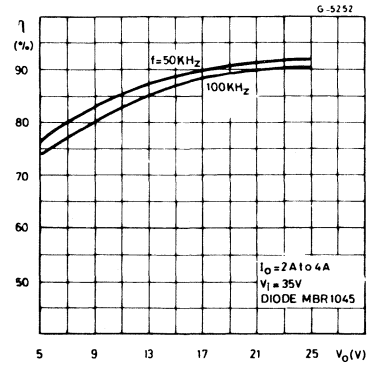


Figure 31 : Current Limiting Threshold vs. $R_{pin\ 4}$ (L296P only).

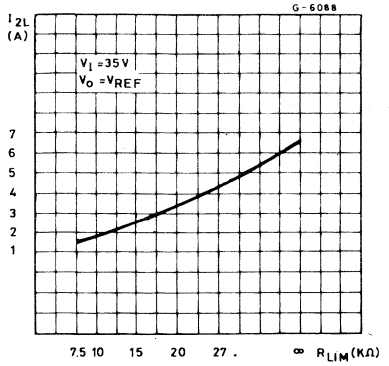


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

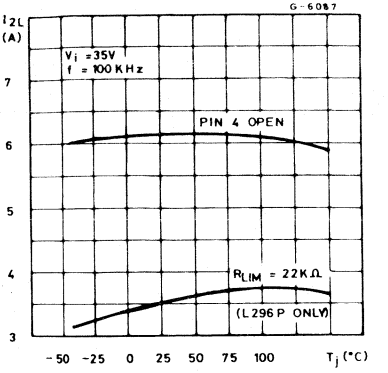
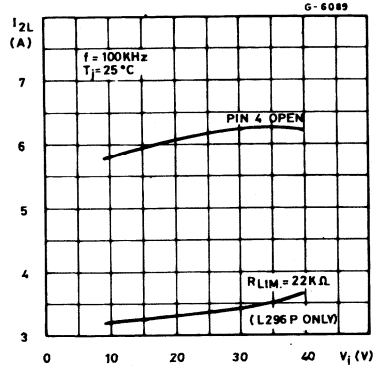
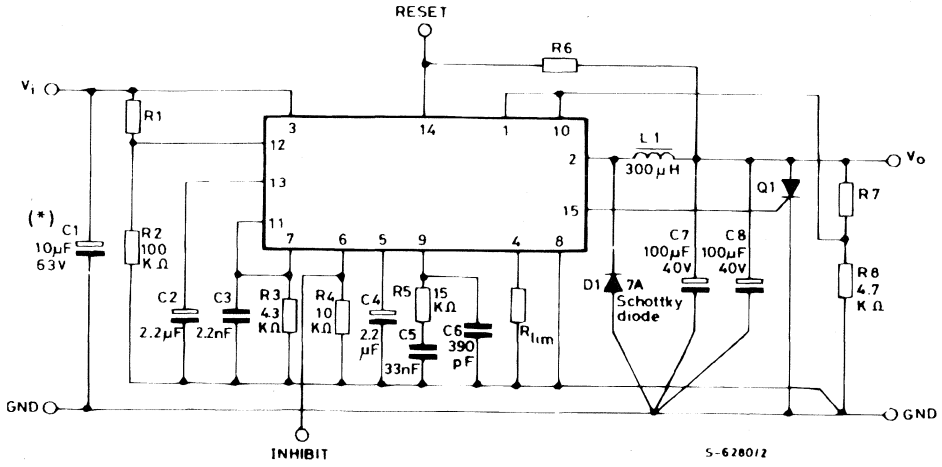


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



(*) Minimum value (10 μF) to avoid oscillations : ripple consideration leads to typical value of 1000 μF or higher L1 : 58930 - MPP COGEMA 946044 : GUP 20 COGEMA 946045

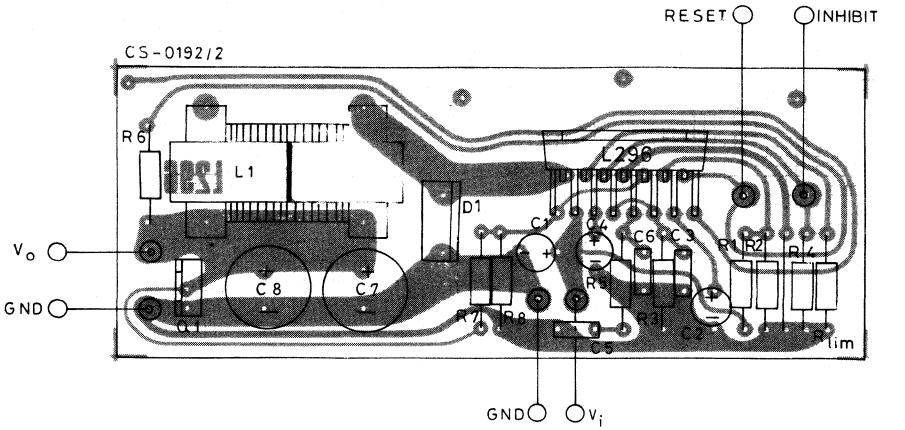
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 μH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages

V_0	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale).



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage Min.	Allowed Rage Max.	Notes
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	220 kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down Resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10 kΩ		
R6		Collector Load For Reset Output	$\frac{V_o}{0.05\ A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R_{iim}	–	Sets Current Limit Level	7.5 kΩ		If R_{iim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2 µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3 nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100 µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

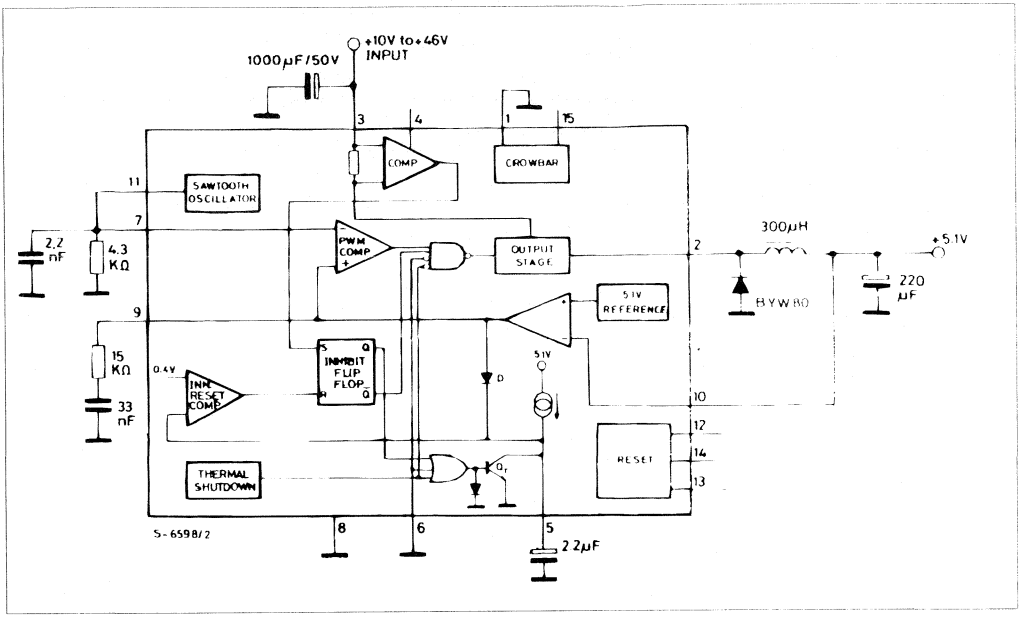


Figure 37 : 12 V/10 A Power Supply.

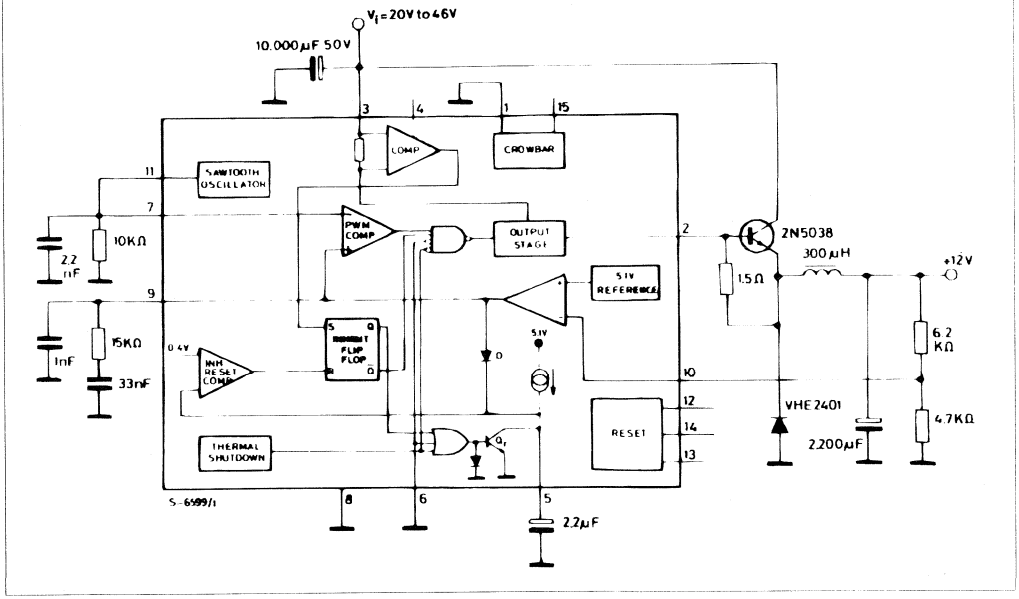
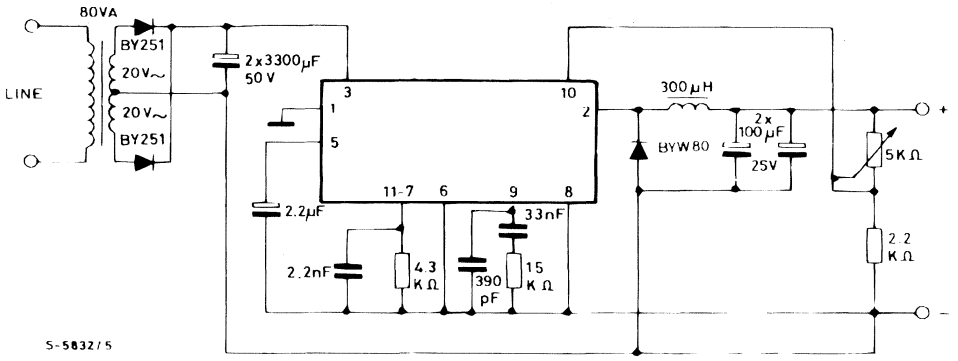
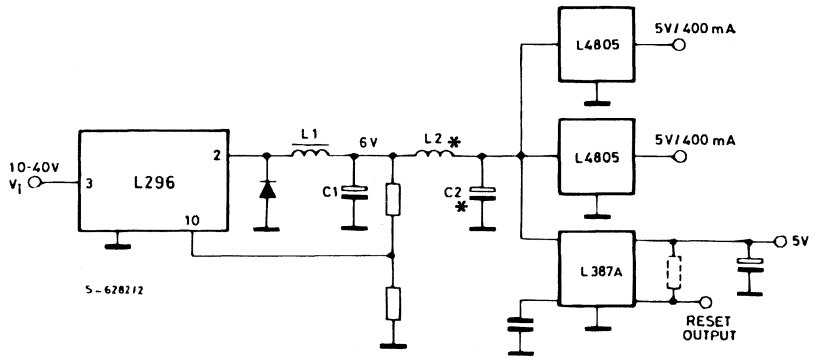


Figure 38 : Programmable Power Supply.



V_o = 5.1 to 15 V
I_o = 4 A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V_o = 5.1 V)
line regulation (220 V ± 15 % and to I_o = 3 A) = 15 mV (V_o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

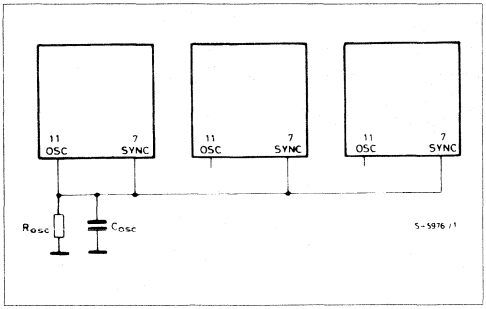


Figure 41 : Voltage Sensing for Remote Load.

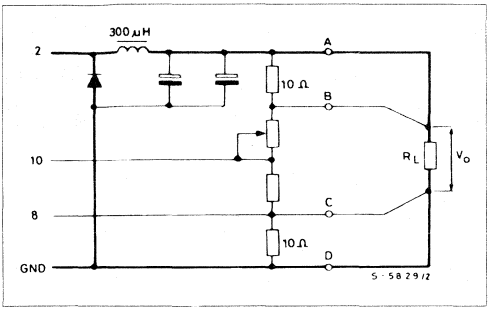


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

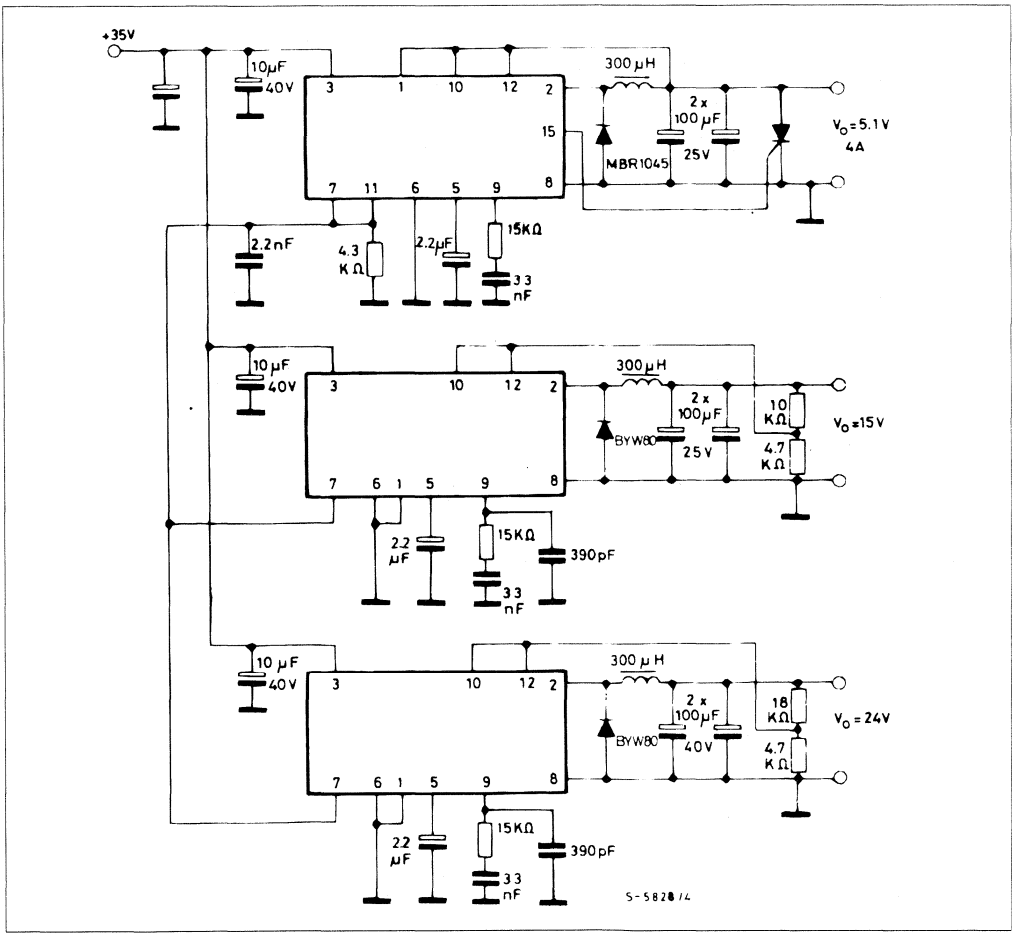
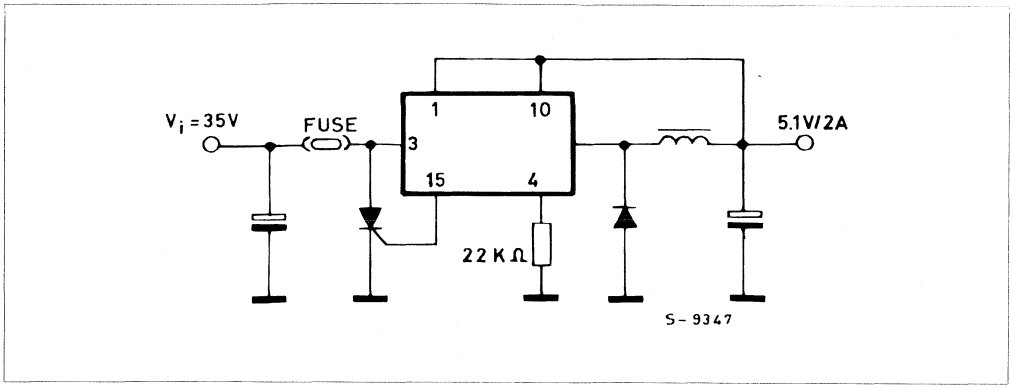


Figure 43 : 5.1 V/2 A Power Supply using External Limiting Current Resistor and Crowbar Protection on the Supply Voltage (L296P only).



SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

The approximate discharge times obtained with this circuit are :

C_{SS}	t_{DIS}
2.2 µF	200 µs
4.7 µF	300 µs
10 µF	600 µs

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 44.

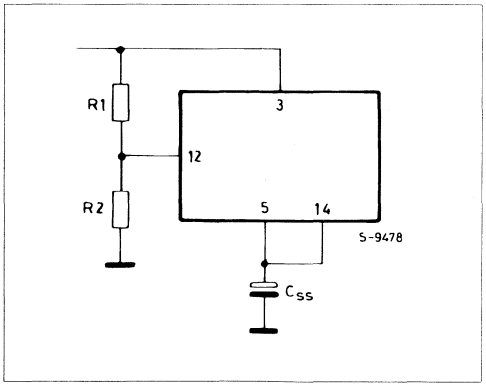
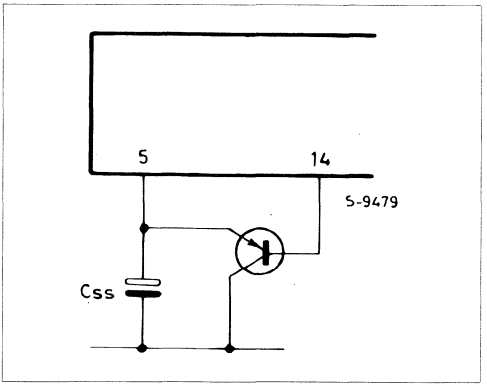


Figure 45.



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

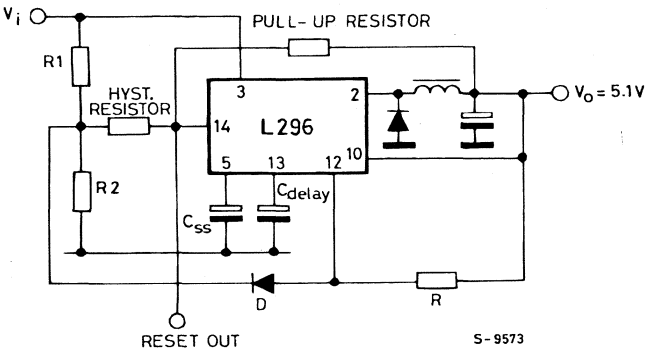
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geq V_{REF}$ - 100 mV and the voltage across R2 is higher than 4.5 V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100 Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100 KΩ and the pull-up resistor of 1 to 2.2 KΩ.

Figure 46.

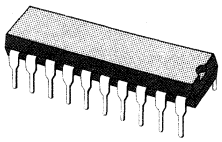


L297
L297A

STEPPER MOTOR CONTROLLERS

- NORMAL/WAWE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULATION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT
- STEP-PULSE DOUBLER (L297A only)

The L297 Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wawe drive modes and on-chip PWM chopper circuits permit switch-mode control of the current in the windings. A feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in a 20-pin plastic package, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons. The L297A also includes a clock pulse doubler.



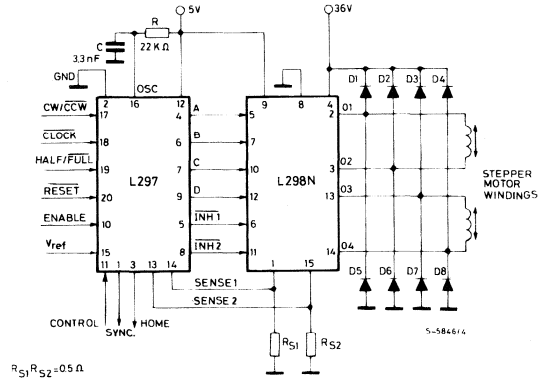
DIP-20 Plastic
(0.25)

ORDER CODES : L297 – L297A

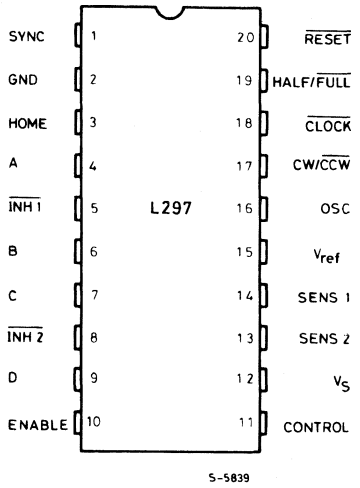
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	– 40 to + 150	°C

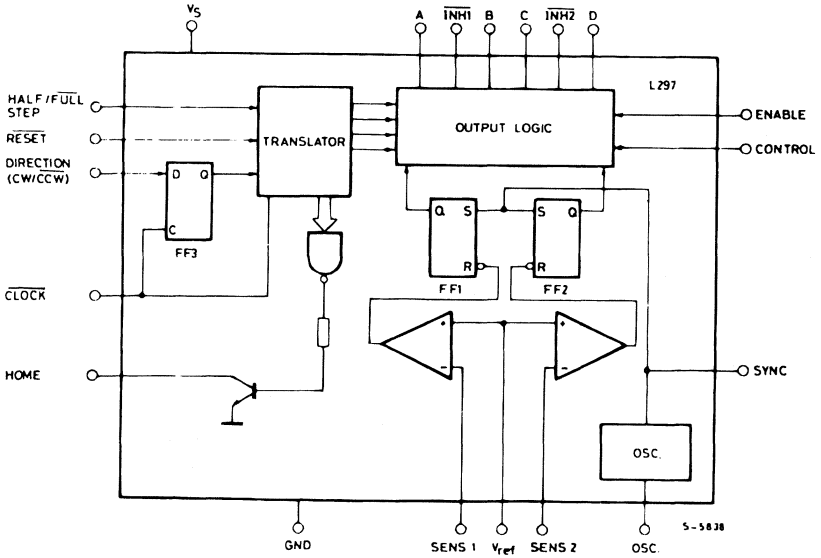
TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT



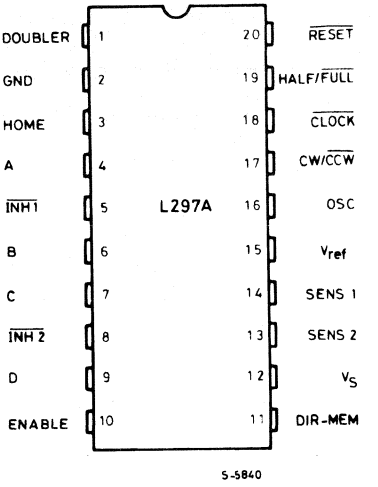
PIN CONNECTION (L297)



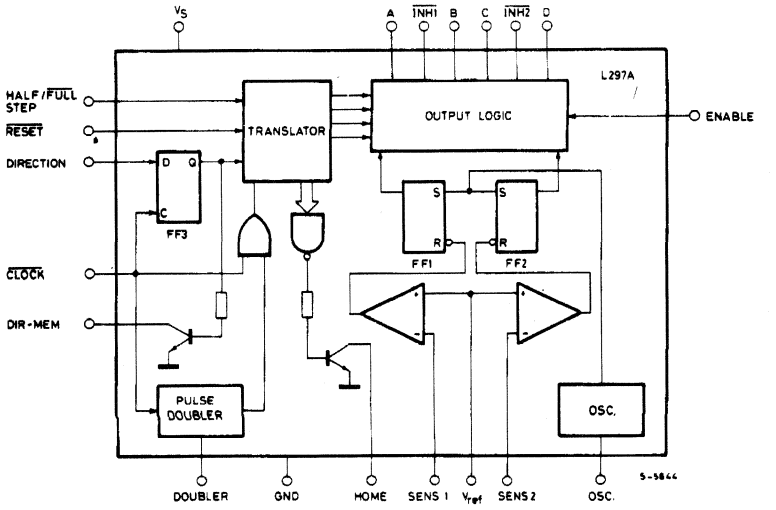
BLOCK DIAGRAM (L297)



PIN CONNECTION (L297A)



BLOCK DIAGRAM (L297A)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

PIN FUNCTIONS – L297

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{INH1}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	$\overline{INH2}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{INH1}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{INH1}$, $\overline{INH2}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{INH1}$ and $\overline{INH2}$; when high chopper acts on phase lines ABCD.
12	V_s	5V supply input.
13	$SENS_2$	Input for load current sense voltage from power stages of phases C and D.
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.

PIN FUNCTIONS – L297 (continued)

N°	NAME	FUNCTION
19	HALF/$\overline{\text{FULL}}$	Half/full step select input. When high selects half step operation, when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designate state 1).
20	$\overline{\text{RESET}}$	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

PIN FUNCTIONS – L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	NAME	FUNCTIONS
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip flop. Open collector output.

CIRCUIT OPERATION

The L297(A) is intended for use with a dual bridge driver, quad darlington array or discrete power devices in step motor driving applications. It receives step clock, direction and mode signals from the systems controller (usually a microcomputer chip) and generates control signals for the power stage.

The principal functions are a translator, which generates the motor phase sequences, and a dual PW/M chopper circuit which regulates the current in the motor windings. The translator generates three different sequences, selected by the HALF/$\overline{\text{FULL}}$ input. These are normal (two phases energised), wave drive (one phase energised) and half-step (alternately one phase energised/two phases energised). Two inhibit signals are also generated by the L297 in half step and wave drive modes. These signals, which connect directly to the L298's enable inputs, are intended to speed current decay when a winding is de-energised. When the L297 is used to drive a unipolar motor the chopper acts on these lines.

An input called CONTROL determines whether the chopper will act on the phase lines ABCD or the inhibit lines $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$. When the phase lines are chopped the non-active phase line of each pair (AB or CD) is activated (rather than interrupting the line then active). In L297 + L298 configurations this technique reduces dissipation in the load current sense resistors.

A common on-chip oscillator drives the dual chopper. It supplies pulses at the chopper rate which set the two flip-flops FF1 and FF2. When the current in a winding reaches the programmed peak value the voltage across the sense resistor (connected to one of the sense inputs $SENS_1$ or $SENS_2$) equals V_{ref} and the corresponding comparator resets its flip flop, interrupting the drive current until the next oscillator pulse arrives. The peak current for both windings is programmed by a voltage divider on the V_{ref} input.

Ground noise problems in multiple configurations can be avoided by synchronising the chopper oscillators. This is done by connecting all the SYNC pins together, mounting the oscillator RC network on one device only and grounding the OSC pin on all other devices.

The L297A includes a pulse doubler on the step clock line which is intended to simplify the implementation of multiple stepping. A ghost pulse is generated automatically after each input pulse, delayed by the time $0.75\ R_d\ C_d$.

The RC network should be dimensioned to place the ghost pulse roughly halfway between clock pulses. If pin 1 (DOUBLER) is grounded the doubler function is disabled.

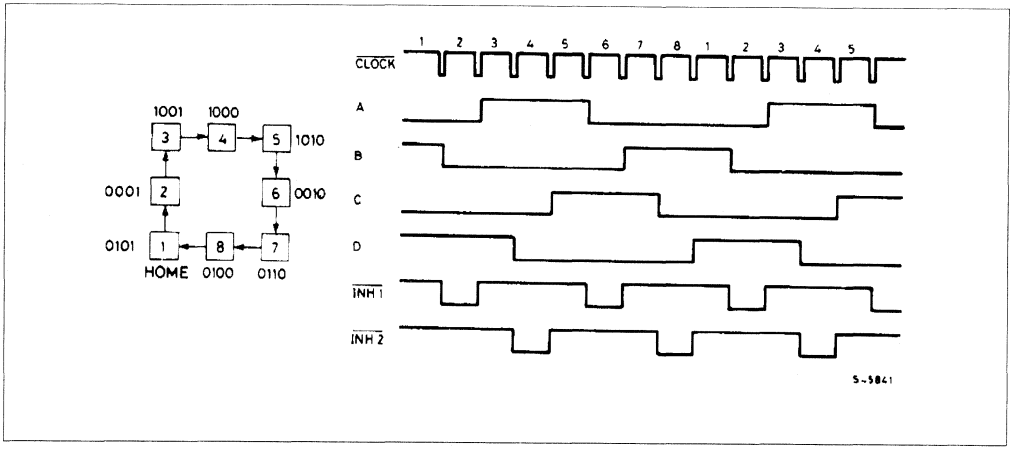
MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transistion of CLOCK.

Clockwise rotation is indicated ; for anticlockwise rotation the sequences are simply reversed. RESET restores the translator to state 1, where ABCD = 0101.

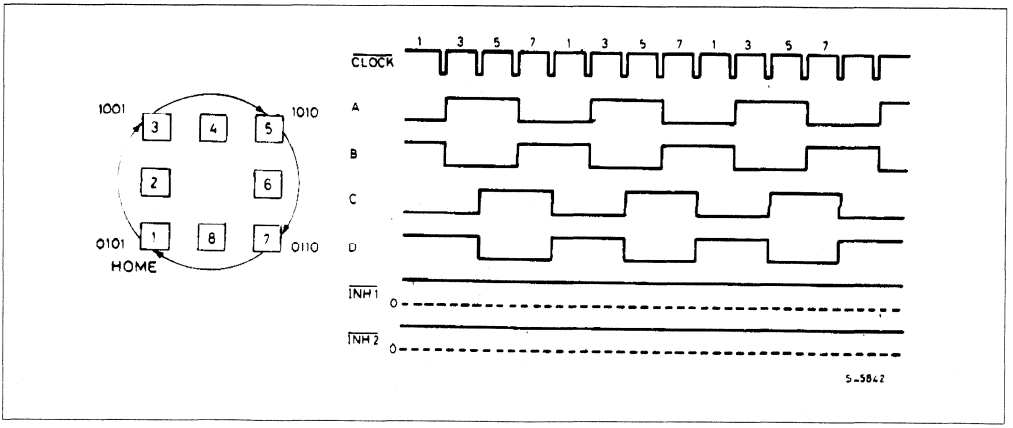
HALF STEP MODE

Half step mode is selected by a high level on the HALF/$\overline{\text{FULL}}$ input.



NORMAL DRIVE MODE

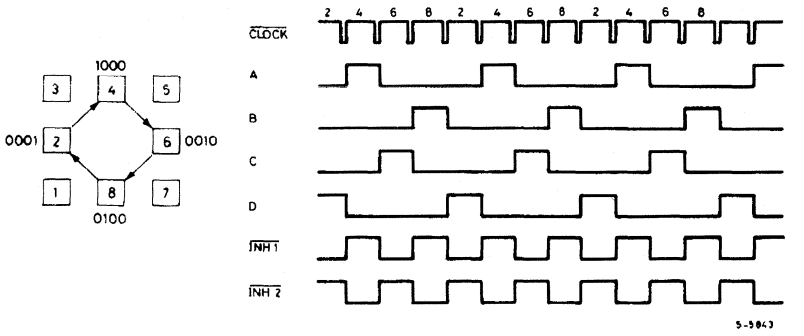
Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the HALF/$\overline{\text{FULL}}$ input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ outputs remain high throughout.



MOTOR DRIVING PHASE SEQUENCES (continued)

WAVE DRIVE MODE

Wave drive mode (also called "one-phase-on" drive) is selected by a low level on the HALF/$\overline{\text{FULL}}$ input when the translator is at an even numbered state (2, 4, 6 or 8).



ELECTRICAL CHARACTERISTICS (Refer to the block diagram T_{amb} = 25°C, V_S = 5V unless otherwise specified)

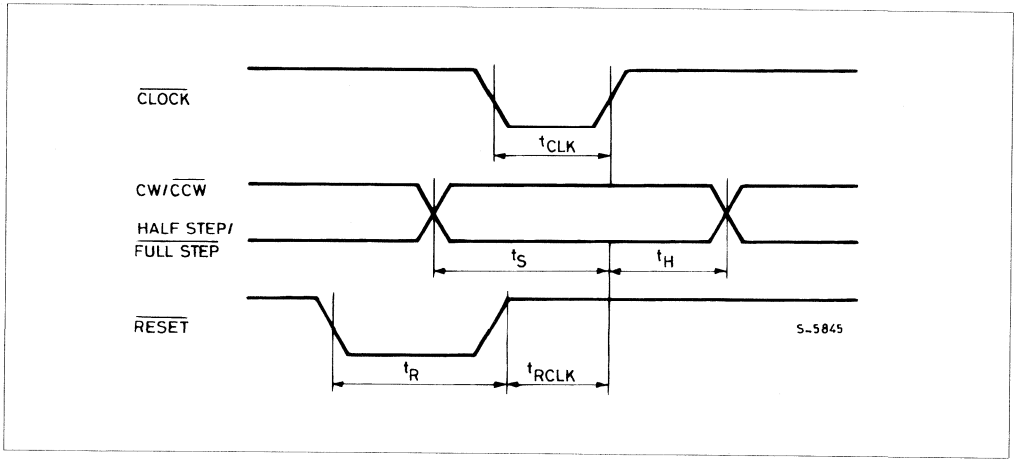
Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 12)			4.75		7	V
I_S	Quiescent supply current (pin 12)	Outputs floating			50	80	mA
V_i	Input voltage (pin 11, 17, 18, 19, 20)		Low			0.8	V
			High	2		V_S	V
I_i	Input current (pin 11, 17, 18, 19, 20)		V_i = L			–100	µA
			V_i = H			10	µA
V_{en}	Enable input voltage (pin 10)		Low			1.5	V
			High	2		V_S	V
I_{en}	Enable input current (pin 10)		V_{en} = L			–100	µA
			V_{en} = H			10	µA
V_o	Phase output voltage (pins 4, 6, 7, 9)	I_o = 10mA	V_{OL}			0.4	V
		I_o = 5mA	V_{OH}	3.9			V
V_{inh}	Inhibit output voltage (pins 5, 8)	I_o = 10mA	$V_{inh\ L}$			0.4	V
		I_o = 5mA	$V_{inh\ H}$	3.9			V
V_{SYNC}	Sync Output Voltage	I_o = 5mA	$V_{SYNC\ H}$	3.3			V
		I_o = 5mA	$V_{SYNC\ V}$			0.8	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{leak}	Leakage current (pin 3, 11*)	V_{CE} = 7 V			1	µA
V_{sat}	Saturation voltage (pins 3, 11*)	I = 5 mA			0.4	V
V_{off}	Comparators offset voltage (pins 13, 14, 15)	V_{ref} = 1 V			5	mV
I_b	Comparator bias current (pins 13, 14, 15)		– 100		10	µA
V_{ref}	Input reference voltage (pin 15)		0		3	V
t_{CLK}	Clock time		0.5			µs
t_S	Set up time		1			µs
t_H	Hold time		4			µs
t_R	Reset time		1			µs
t_{RCLK}	Reset to clock delay		1			µs

* L297A only

Figure 1.



APPLICATION INFORMATION

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

This circuit drives bipolar stepper motors with winding currents up to 2A. The diodes are fast 2A types.

Figure 2.

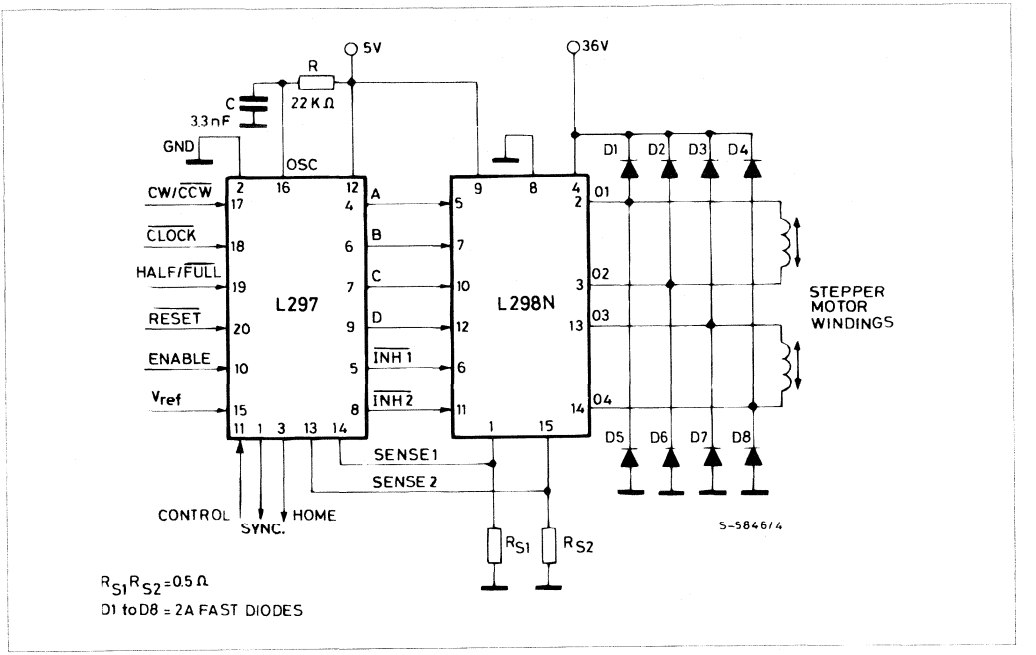


Figure 3 : Synchronising L297s

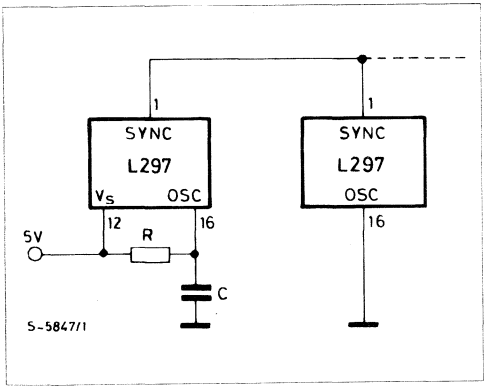
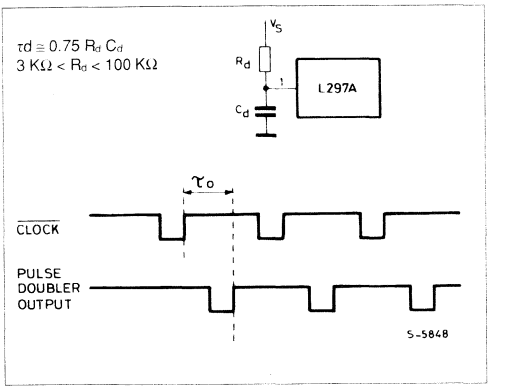


Figure 4 : Pulse doubler (L297A)



DUAL FULL-BRIDGE DRIVER

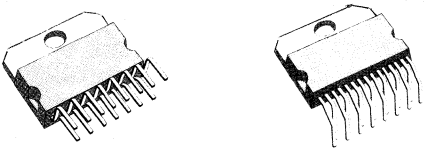
PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)

DESCRIPTION

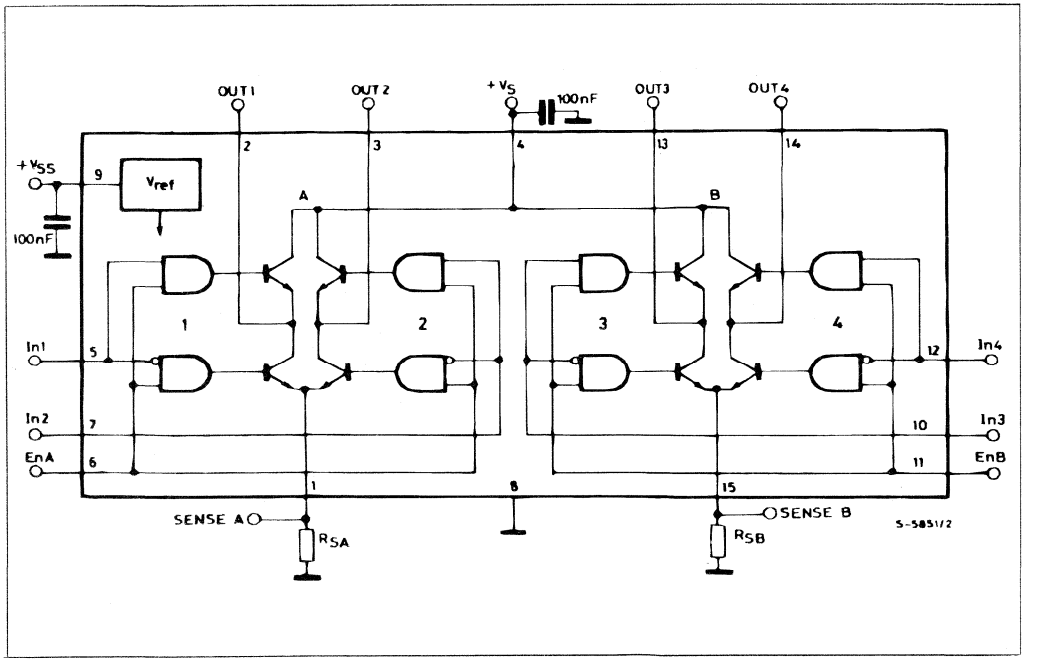
The L298N is an integrated monolithic circuit in a 15-lead Multiwatt® package. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

Multiwatt
(15-lead)



ORDER CODES : L298N
L298HN

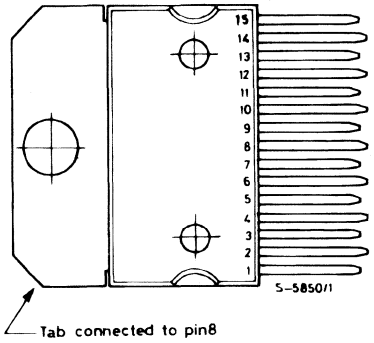
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I, V_{en}	Input and Enable Voltage	– 0.3 to 7	V
I_O	Peak Output Current (each channel) - Non Repetitive (t = 100 µs) - Repetitive (80 % on – 20 % off ; t_{on} = 10 ms) - DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	– 1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



CURRENT SENSING B
OUTPUT 4
OUTPUT 3
INPUT 4
ENABLE B
INPUT 3
LOGIC SUPPLY VOLTAGE V_{SS}
GROUND
INPUT 2
ENABLE A
INPUT 1
SUPPLY VOLTAGE V_S
OUTPUT 2
OUTPUT 1
CURRENT SENSING A

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

PIN FUNCTIONS (refer to the block diagram)

N°	Name	Function
1 ; 15	Sense A ; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2 ; 3	Out 1 ; Out 2	Outputs of the Bridge A ; the current that flows through the load connected between these two pins is monitored at pin 1.
4	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100 nF capacitor must be connected between this pin and ground.
5 ; 7	Input 1 ; Input 2	TTL Compatible Inputs of the Bridge A.
6 ; 11	Enable A ; Enable B	TTL Compatible Enable Input : the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	GND	Ground.
9	V_{SS}	Supply Voltage for the Logic Bloks. A 100 nF capacitor must be connected between this pin and ground.
10 ; 12	Input 3 ; Input 4	TTL Compatible Inputs of the Bridge B.
13 ; 14	Out 3 ; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.

ELECTRICAL CHARACTERISTICS (V_S = 42 V ; V_{SS} = 5 V, T_j = 25 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} + 2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H I_L = 0	V_i = L		13	22	mA
			V_i = H		50	70	
		V_{en} = L	V_i = x			4	
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H I_L = 0	V_i = L		24	36	mA
			V_i = H		7	12	
		V_{en} = L	V_i = x			6	
V_{iL}	Input Low Voltage (pins 5,7,10,12)			− 0.3		1.5	V
V_{iH}	Input High Voltage (pins 5,7,10,12)			2.3		V_{SS}	
I_{iL}	Low Voltage Input Current (pins 5,7,10,12)	V_i = L				− 10	µA
I_{iH}	High Voltage Input Current (pins 5,7,10,12)	V_i = H ≤ V_{SS} − 0.6 V			30	100	
V_{en} = L	Enable Low Voltage (pins 6,11)			− 0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6,11)			2.3		V_{SS}	
I_{en} = L	Low Voltage Enable Current (pins 6,11)	V_{en} = L				− 10	µA
I_{en} = H	High Voltage Enable Current (pins 6,11)	V_{en} = H ≤ V_{SS} − 0.6 V			30	100	
$V_{CE\ sat\ (H)}$	Source Saturation Voltage	I_L = 1 A			1.35	1.7	V
		I_L = 2 A			2	2.7	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE\ sat\ (L)}$	Sink Saturation Voltage	I_L = 1 A (5)		1.2	1.6	V
		I_L = 2 A (5)		1.7	2.3	
$V_{CE\ sat}$	Total Drop	I_L = 1 A (5)			3.2	V
		I_L = 2 A (5)			4.9	
V_{sens}	Sensing Voltage (pins 1, 15)		−1 (1)		2	V
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2) ; (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2) ; (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3) ; (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3) ; (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.2		µs
f_c (V_i)	Commutation Frequency	I_L = 2 A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2) ; (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2) ; (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3) ; (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (3) ; (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.1		µs
f_c (V_{en})	Commutation Frequency	I_L = 2 A		1		KHz

1) Sensing voltage can be −1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ − 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.
5) PIN 1 and PIN 15 connected to GND.

Figure 1 : Typical Saturation Voltage vs. Output Current.

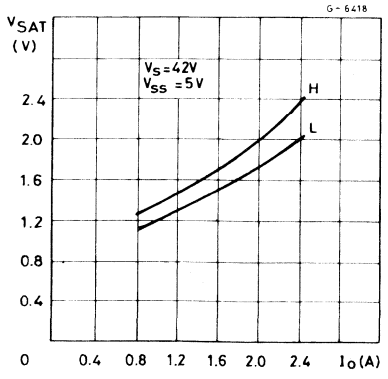
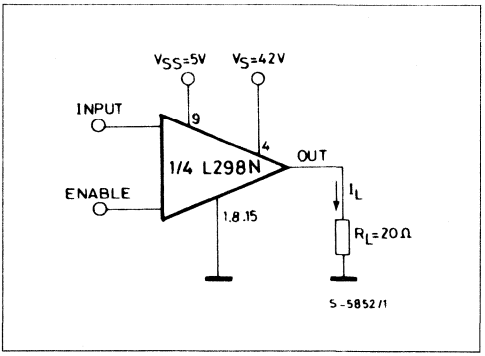


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

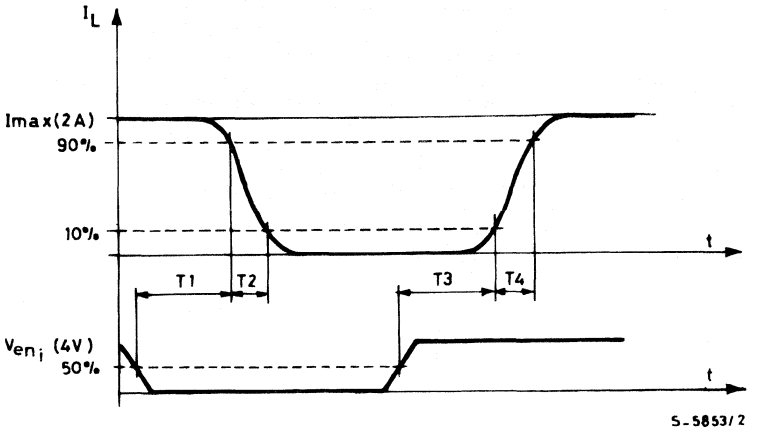
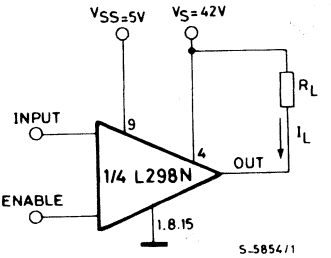


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

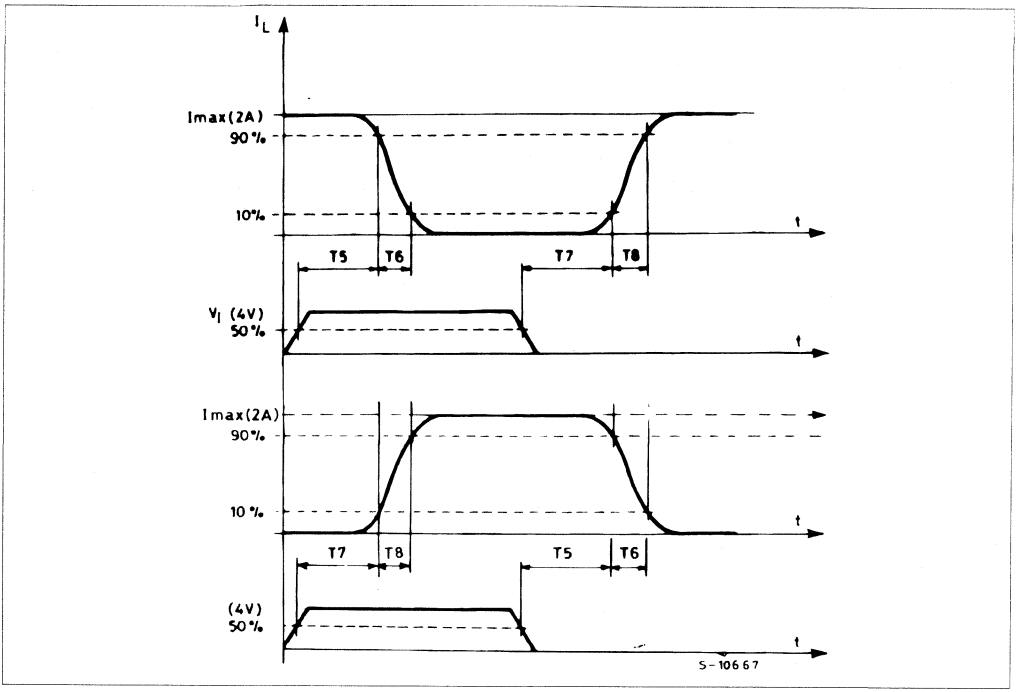
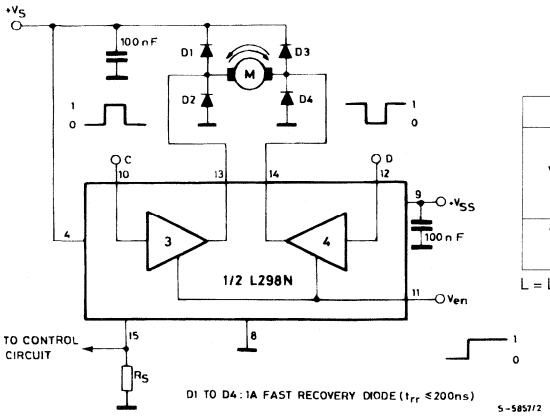


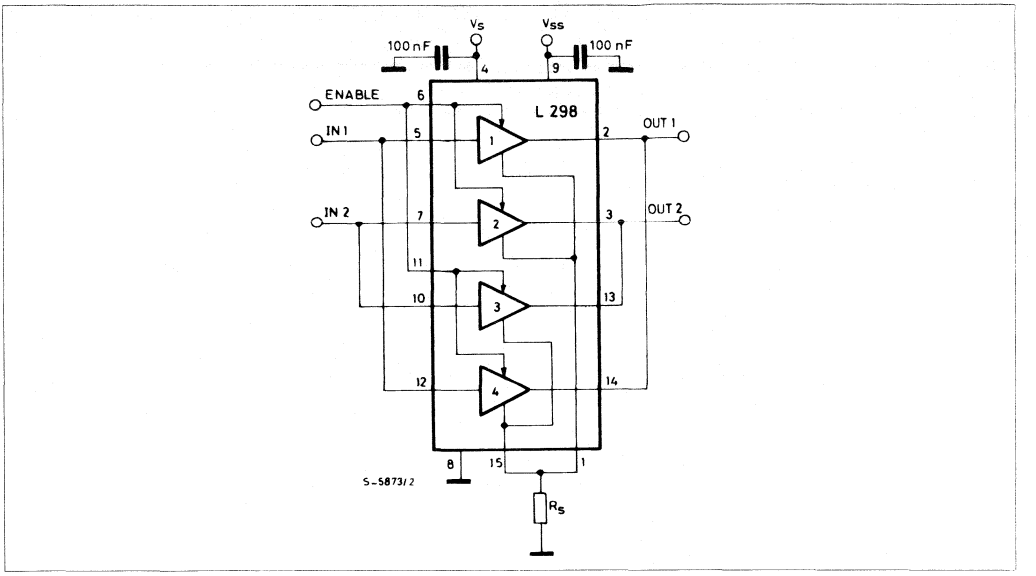
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Turn Right
	C = L ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = C	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298N integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to pin 8 (GND). When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298N.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements (trr $\leq$ 200 nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the

IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

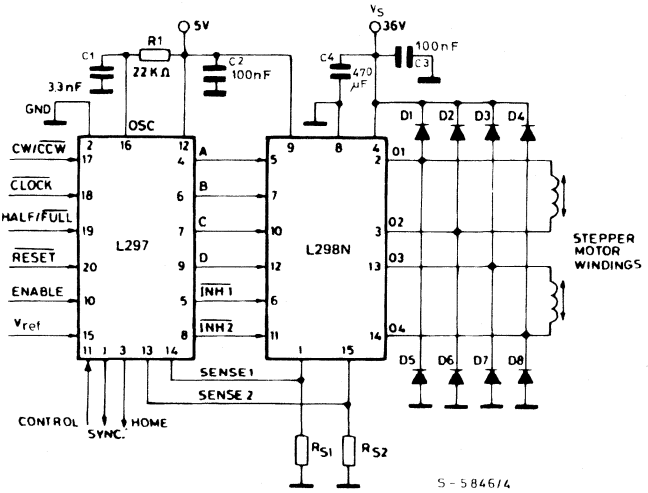
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298N are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\ \Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A ; trr ≤ 200 ns

Figure 9: Suggested Printer Circuit Board Layout for the Circuit of fig. 8 (1 : 1 scale)

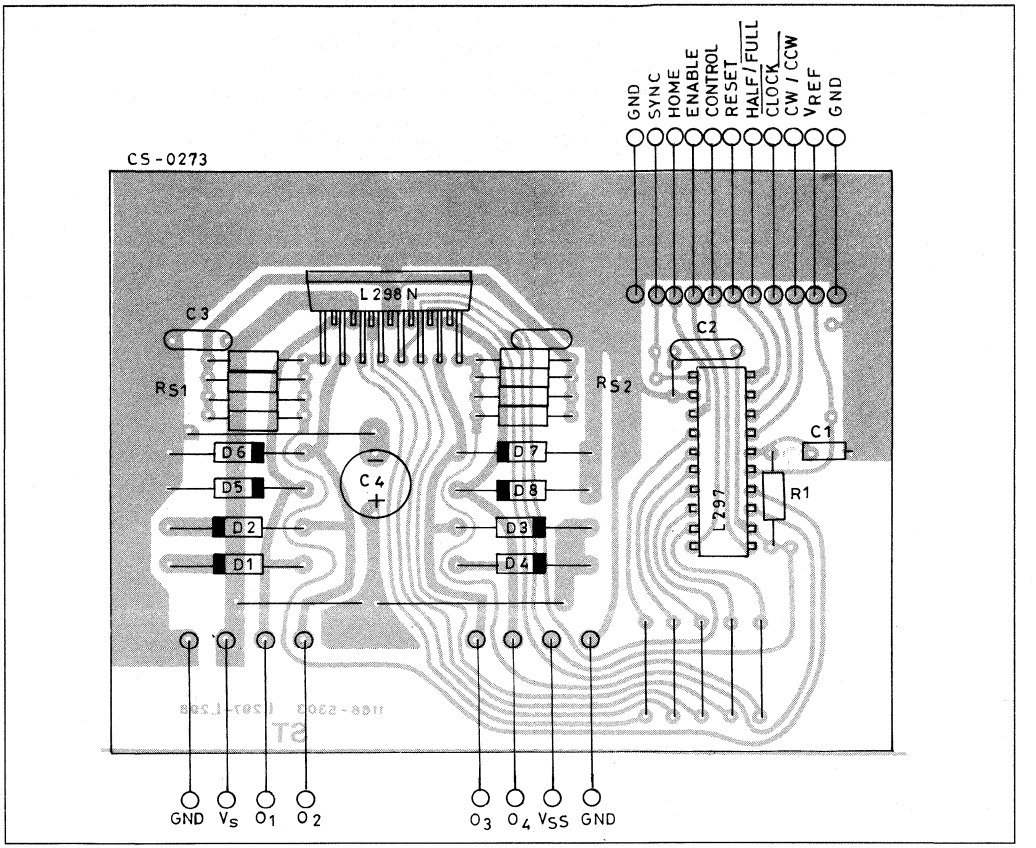
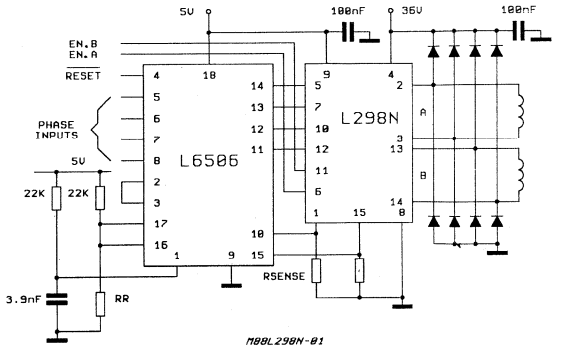


Figure 10: Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.



R_R and R_{sense} depend from the load current

SGS-THOMSON MICROELECTRONICS

L601-L603
L602-L604

DARLINGTON ARRAYS

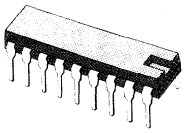
- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400 mA PER DRIVER (500 mA PEAK)
- OUTPUT VOLTAGE 90 V ($V_{CE\ (sus)}$ = 70 V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The four versions interface to all common logic families :

L601	General purpose
L602	14 - 25 V PMOS
L603	5 V TTL, CMOS
L604	6 - 15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



DIP-18
(Plastic)

ORDER CODES : L601C L603C
L602C L604C

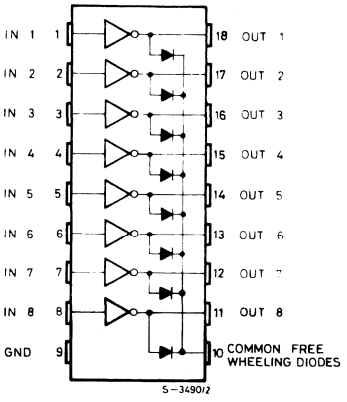
DESCRIPTION

The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can with stand peak currents of 500 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

ABSOLUTE MAXIMUM RATINGS

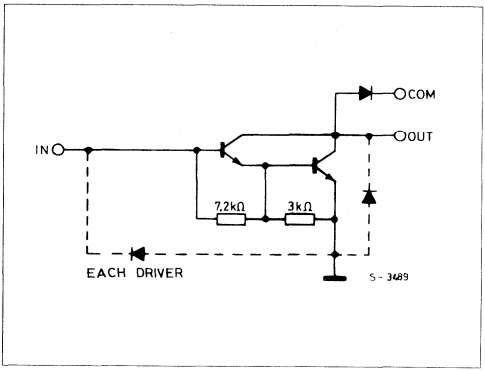
Symbol	Parameter	Value	Unit
V_{CEX}	Collector Emitter Voltage (input open)	90	V
I_C	Collector Current	0.4	A
I_C	Collector Peak Current	0.5	A
V_i	Input Voltage (for L602, L603 and L604)	30	V
I_i	Input Current (for L601 only)	25	mA
P_{tot}	Total Power Dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating Junction Temperature	– 25 to 150	°C

PIN CONNECTIONS (top view)

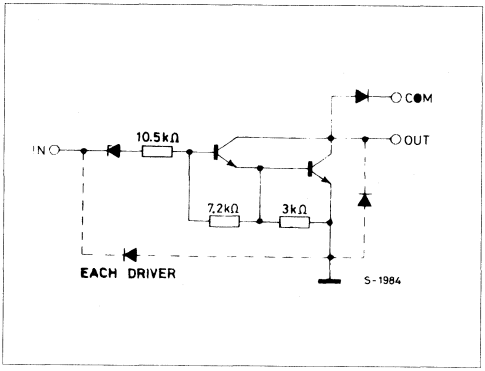


SCHEMATIC DIAGRAMS

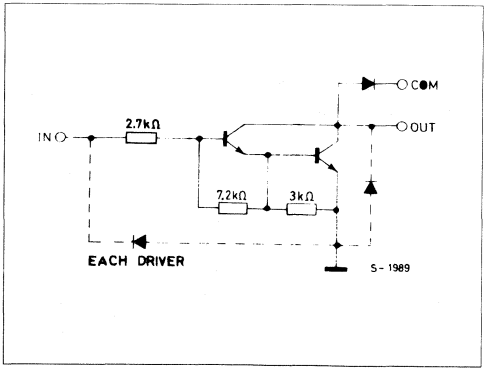
L601



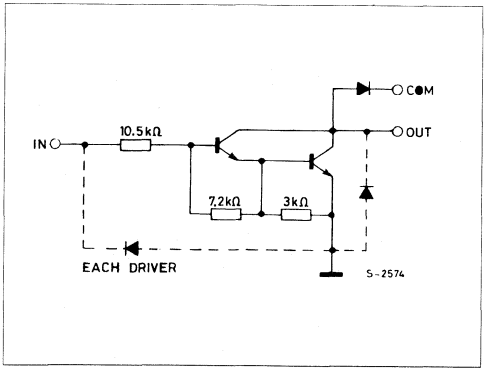
L602



L603



L604



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

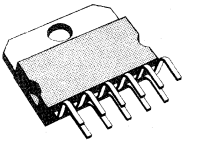
Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current	V_{CE} = 90 V				10	µA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage	I_C = 300 mA I_C = 200 mA I_C = 100 mA	I_B = 500 µA I_B = 350 µA I_B = 250 µA			2 1.7 1.2	V V V
h_{FE}	DC Forward Current Gain (L601 only)	V_{CE} = 3 V	I_C = 300 mA	1000			–
V_i	Minimum Input Voltage (ON condition)	V_{CE} = 3 V for L602 for L603 for L604	I_C = 300 mA			 11.5 2.5 5	 V V V
V_i	Maximum Input Voltage (OFF condition)	V_{CE} = 90 V for L601 for L602 for L603 for L604	I_C = 25 µA	 0.55 7 0.75 1			 V V V V
I_R	Clamp Diode Reverse Current	V_R = 90 V				50	µA
V_F	Clamp Diode Forward Voltage	I_F = 300 mA			2	2.4	V
t_{on}	Turn-on Delay	0.5 V_i to 0.5 V_o			0.4		µs
t_{off}	Turn-off Delay	0.5 V_i to 0.5 V_o			0.4		µs

SGS-THOMSON
MICROELECTRONICS

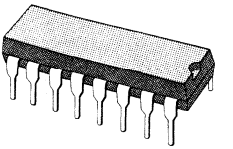
L702

2A QUAD DARLINGTON SWITCH

- SUSTAINING VOLTAGE : 70 V
- 2 A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.



Multiwatt-11



Powerdip 8 + 8

ORDER CODES : L702B - Powerdip
L702N - Multiwatt

DESCRIPTION

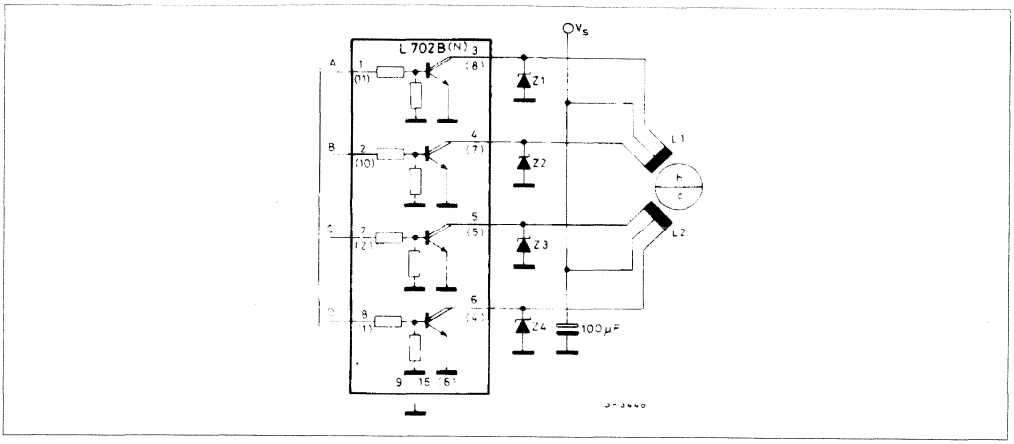
The L702 is a monolithic integrated circuit for high current and high voltage switching applications. It comprises four darlington transistors with common emitter and open collector suitable for current sinking applications mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs ; it can provide direct interface between low level logic and a variety of high current applications.

ABSOLUTE MAXIMUM RATINGS

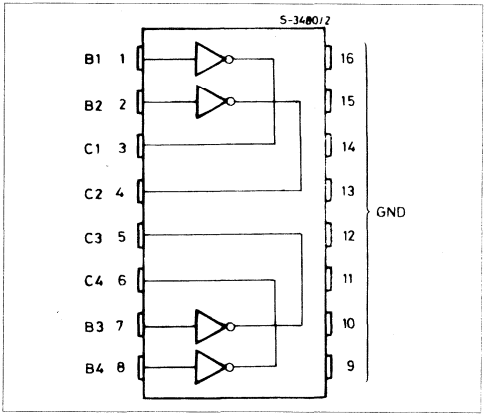
Symbol	Parameter		Value	Unit
V_{CEX}	Collector-emitter Voltage (input open)		90	V
V_i	Input Voltage		30	V
I_C	Collector Current		3	A
P_{tot}	Total Power Dissipation at T_{pin} 9 to 16 ≤ 90 °C	Powerdip	4	W
	Total Power Dissipation at T_{amb} ≤ 70 °C	Powerdip	1.1	W
	Total Power Dissipation at T_{case} ≤ 90 °C	Multiwatt	20	W
T_{stg}	Storage Temperature		– 55 to 150	°C
T_j	Operating Junction Temperature		– 25 to 150	°C

STEPPING MOTOR BUFFER

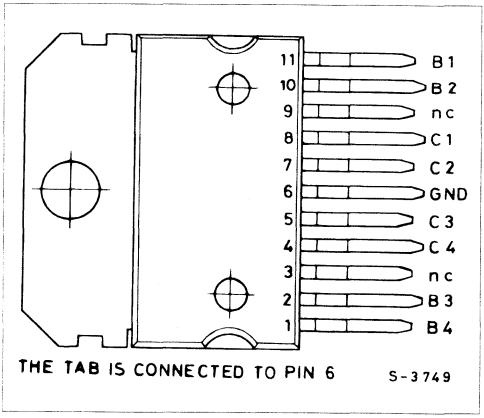


CONNECTION DIAGRAMS (top view)

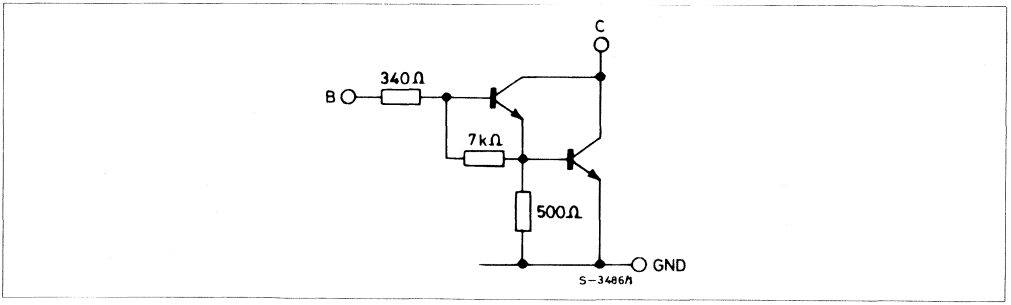
Powerdip



Multiwatt



SCHEMATIC DIAGRAM (each Darlington)



SGS-THOMSON MICROELECTRONICS

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	} Powerdip	Max	70	°C/W
$R_{th\ j\text{-}pins\ 9/16}$	Thermal Resistance Junction Pins 9 to 16		Max	14	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Multiwatt	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current		V_{CE} = 90 V			10	50	µA
$V_{CE(sust)}$	Collector Emitter (°) Sustaining Voltage		I_C = 100 mA		70			V
$V_{CE(sat)}$	Collector Emitter Saturation Voltage		I_C = 1.25 A I_i = 2 mA			1.3	1.9	V
h_{FE}	DC Forward Current Gain		I_C = 1 A V_{CE} = 3 V		1 000	4 000		
I_i	Input Current		V_i = 3.75 V V_i = 2.4 V Open Collector			7 3	11 6	mA mA
V_i	Input Voltage	Off Condition	V_{CE} = 70 V	$I_C \leq$ 0.1 mA			0.4	V
		On Condition	V_{CE} = 3 V	$I_C \geq$ 1 A	2.4			V
T_{on}	Turn On Time		V_s = 12 V R_L = 10 Ω			0.3		µs
T_{off}	Turn Off Time					1		µs

Figure 1 : Switching Time.

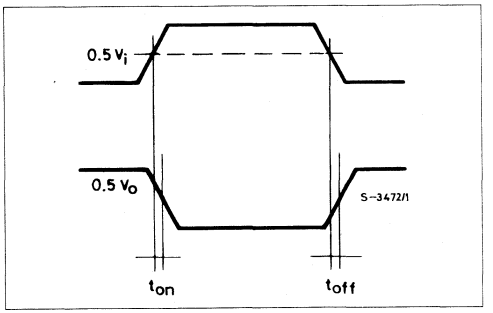


Figure 2 : t_{on} and t_{off} Test Circuit.

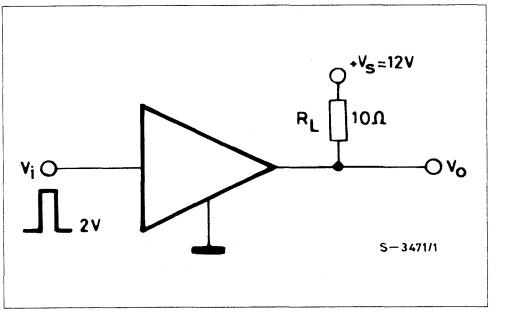


Figure 3 : Peak Collector Current vs. Duty Cycle and Number of Outputs (L702B only).

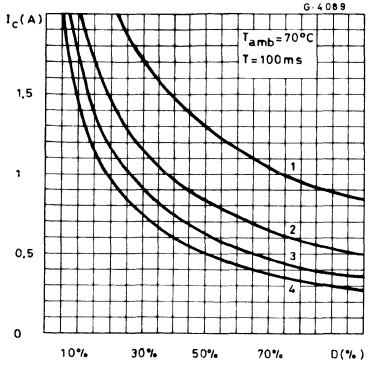


Figure 4 : Collector Emitter Saturation Voltage vs. Collector Current.

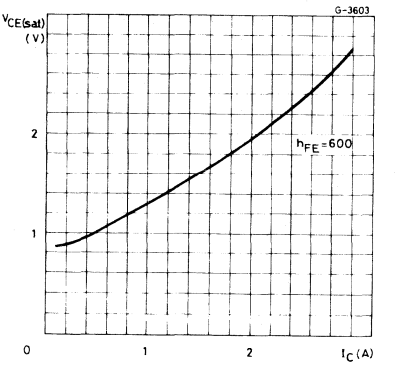


Figure 5 : Collector Current vs. Input Voltage.

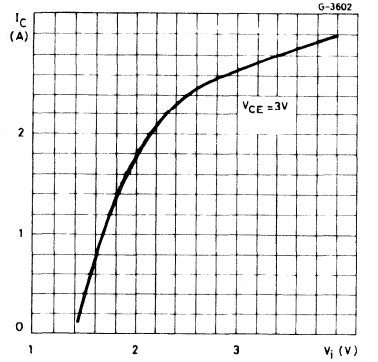


Figure 6 : Input Current vs. Input Voltage.

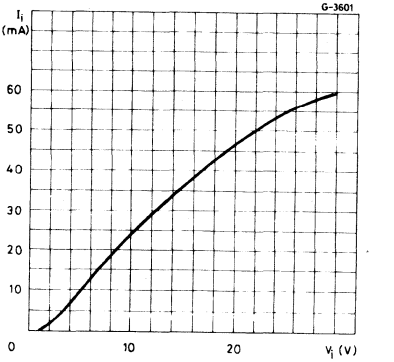


Figure 7 : Safe Operating Areas (L702B).

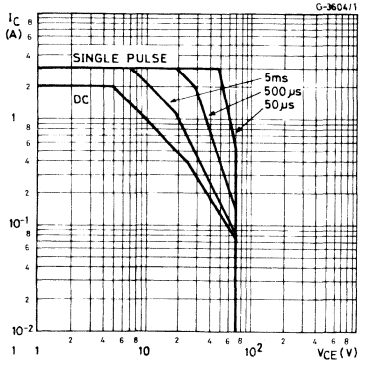
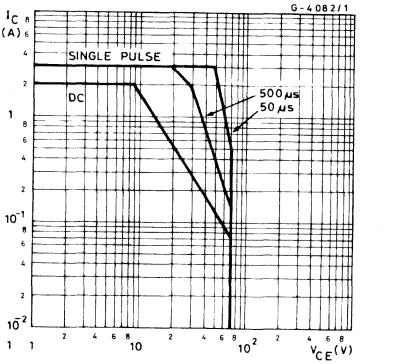


Figure 8 : Safe Operating Areas (L702N).



SGS-THOMSON MICROELECTRONICS

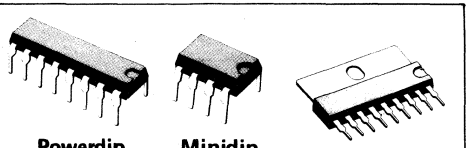
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

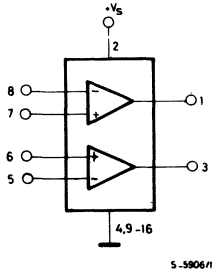
ORDERING NUMBERS:

L2720 L2722 L2724

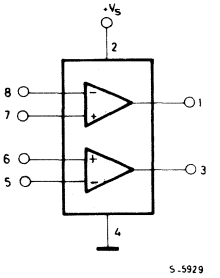
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L2720)**, T_{amb} = 50°C **(L2722)** T_{case} = 75°C **(L2720)** T_{case} = 50°C **(L2724)**	1 5 10	W W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

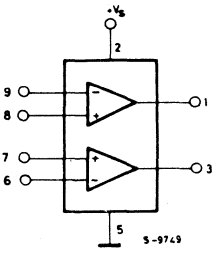
BLOCK DIAGRAMS



L2720

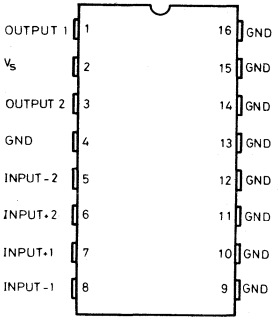


L2722

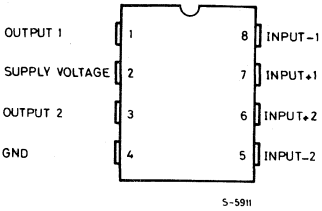


L2724

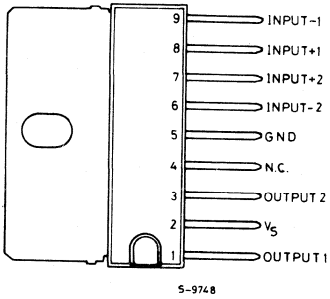
CONNECTION DIAGRAMS
(Top view)



L2720

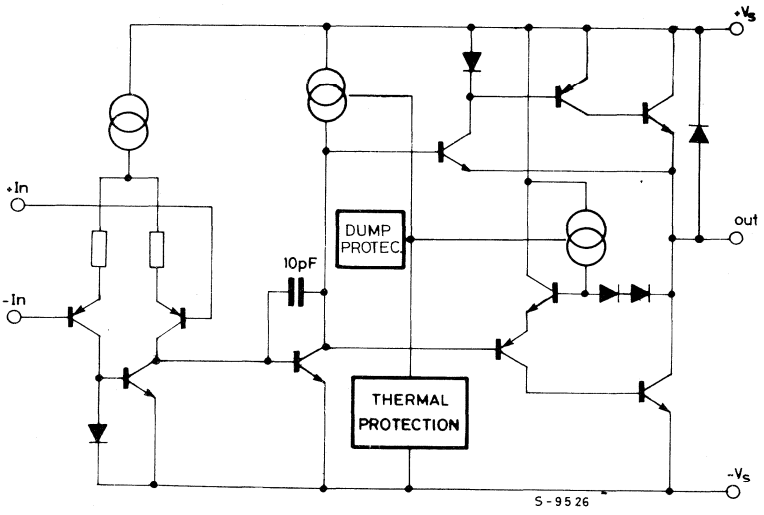


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

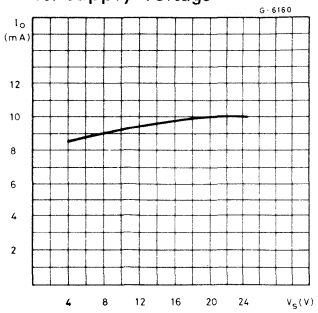


Fig. 2 - Open loop gain vs. frequency

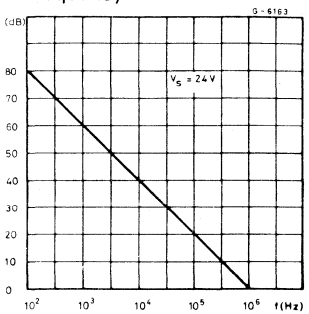


Fig. 3 - Common mode rejection vs. frequency

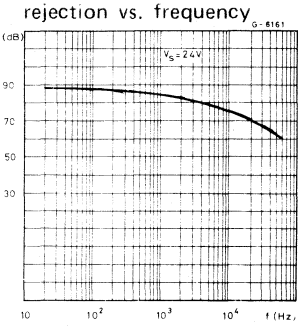


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

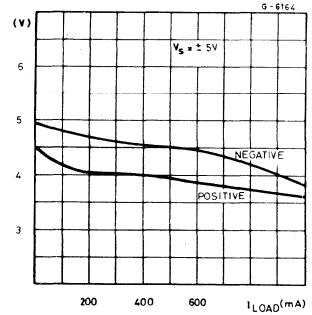


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

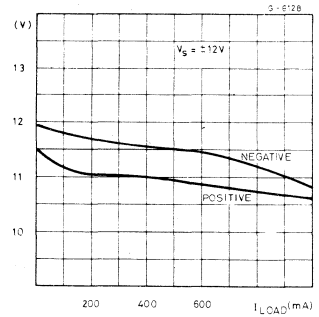


Fig. 6 - Supply voltage rejection vs. frequency

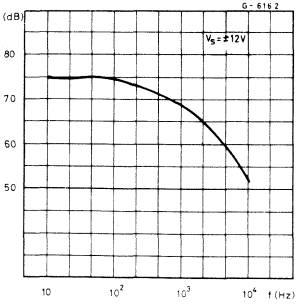
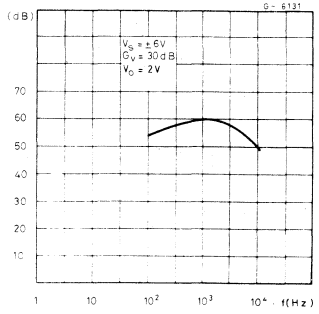


Fig. 7 - Channel separation vs. frequency

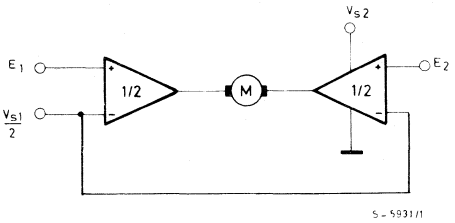


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

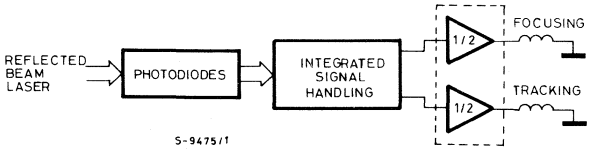


Fig. 10 - Capstan motor control in video recorders

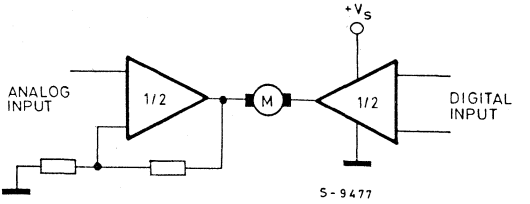
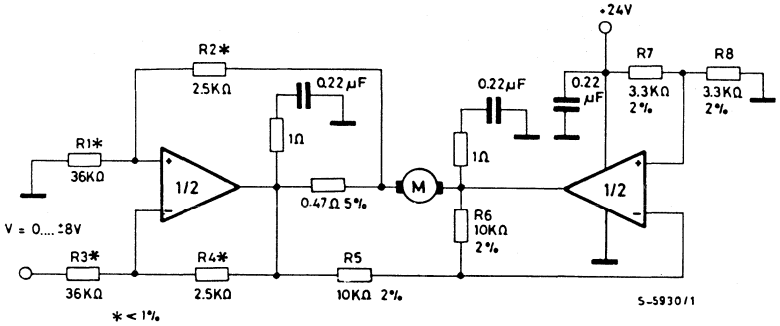


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_i - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

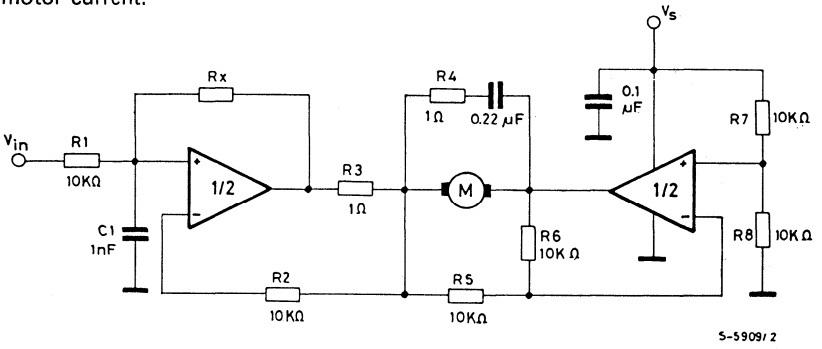
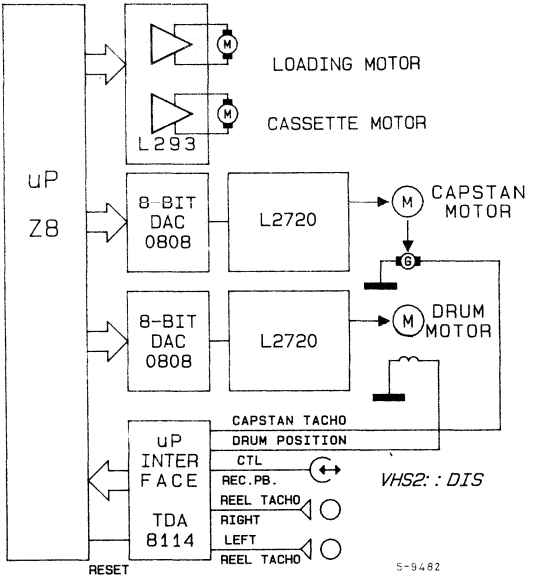


Fig. 13 - VHS-VCR Motor control circuit



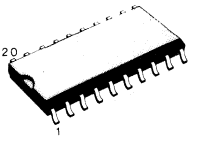
LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



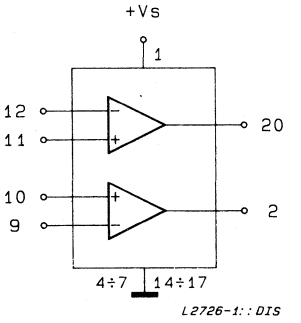
SO-20
(12 + 4 + 4)

ORDER NUMBER: L2726

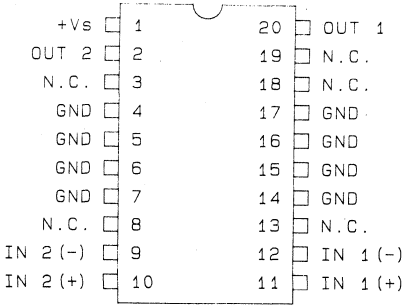
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 85°C T_{case} = 75°C	1 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

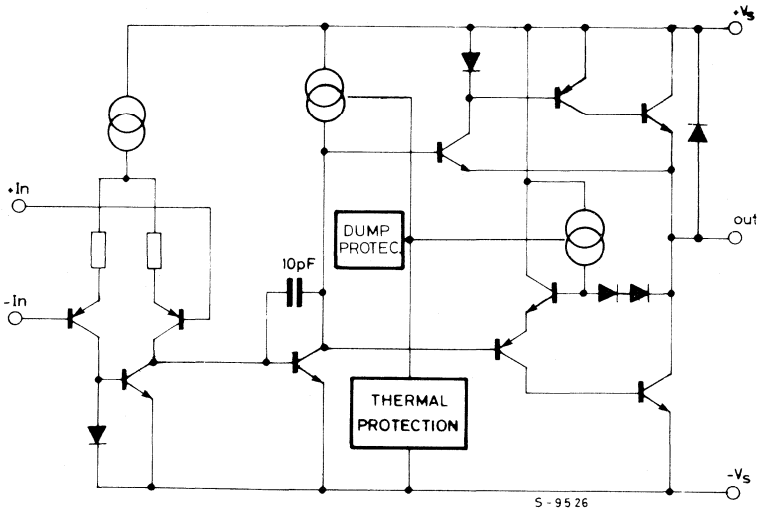


CONNECTION DIAGRAM
(Top view)



L2726-2: : DIS

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	15.0	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (*)	max	65	°C/W

(*) With 4 sq. cm copper area heatsink

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

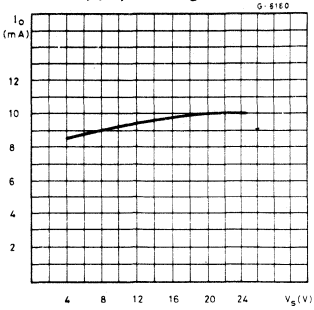


Fig. 2 - Open loop gain vs. frequency

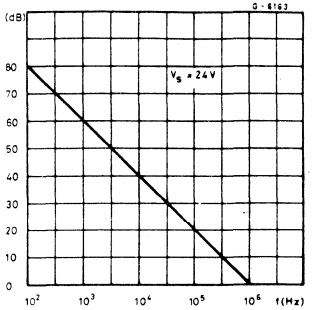


Fig. 3 - Common mode rejection vs. frequency

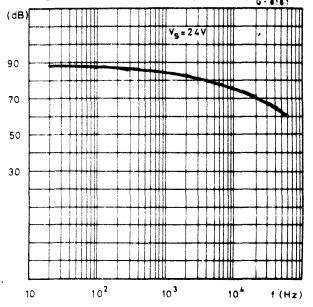


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

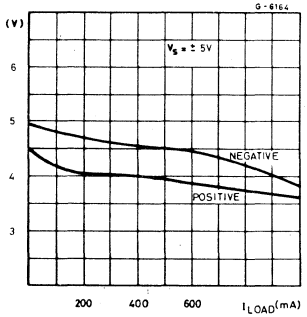


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

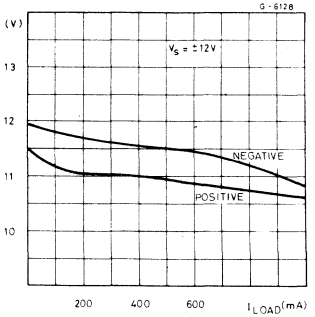


Fig. 6 - Supply voltage rejection vs. frequency

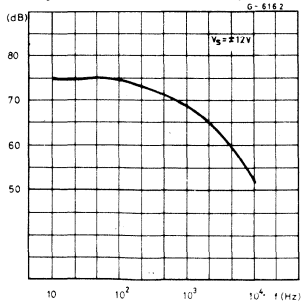
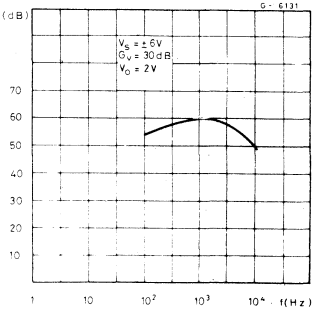


Fig. 7 - Channel separation vs. frequency



SGS-THOMSON MICROELECTRONICS

L2750

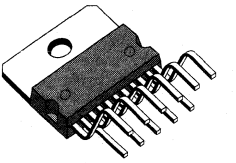
DUAL LOW DROP HIGH POWER OPERATIONAL AMPLIFIER

ADVANCE DATA

- HIGH OUTPUT CURRENT
- VERY LOW SATURATION VOLTAGE
- LOW VOLTAGE OPERATION
- LOW INPUT OFFSET VOLTAGE
- GND COMPATIBLE INPUTS
- ST-BY FUNCTION (LOW CONSUMPTION)
- HIGH APPLICATION FLEXIBILITY

PROTECTIONS:

- VERY INDUCTIVE LOADS
- OVERRATING CHIP TEMPERATURE
- LOAD DUMP VOLTAGE
- FORTUITOUS OPEN GROUND
- ESD



Multiwatt-11

ORDERING NUMBER: L2750

DESCRIPTION

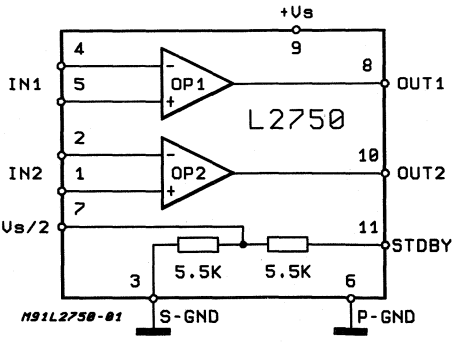
The L2750 is a new technology class AB dual power operational amplifier assembled in Multiwatt 11 package.

Thanks to the fully complementary PNP/NPN output configuration the L2750 can deliver a rail-to-rail output voltage swing even at the highest current.

Additional feature is the very low current Stand-By function.

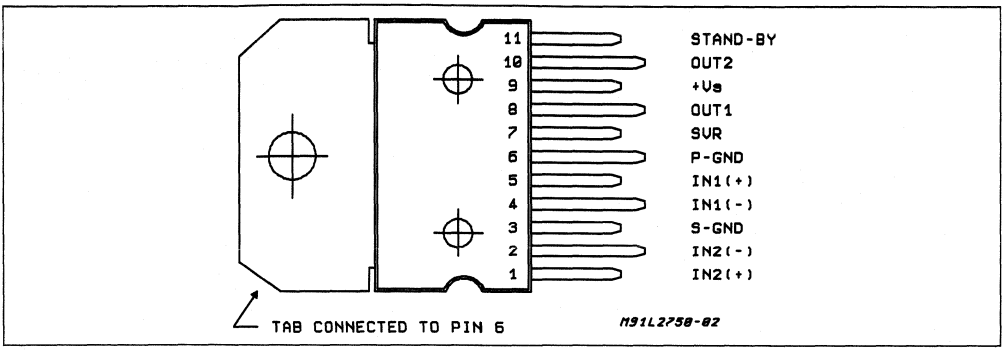
The high application flexibility of the L2750 makes the device suitable for either motor driving/control and audio applications purposes.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{S\ op}$	Operating Supply Voltage	18	V
$V_{S\ max}$	Supply Voltage	28	V
V_{PEAK}	Peak Supply Voltage (t = 50ms)	40	V
V_i	Input Voltage	$V_{S\ op}$	V
V_i	Differential Input Voltage	$V_{S\ op}$	V
I_O	Output Peak Current (non rep. t = 100µs)	5	A
I_O	Output Peak Current (rep. f > 10Hz)	4	A
P_{tot}	Power Dissipation T_{CASE} – 85°C	36	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the operational amplifier with G_V = 24dB; V_S = 14.4V; T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		18	V
I_d	Total Quiescent Drain Current			30	50	mA
V_{OS}	Input Offset Voltage				5	mV
I_{SB}	ST-BY Current Consumption				50	µA
I_S	Input Bias Current				0.5	µA
I_{OS}	Input Offset Current				50	nA
V_{DROP}	Output Voltage Drop (High)	I_O = 0.5A I_O = 3A		0.25 1.1	0.5 2.5	V V
	Output Voltage Drop (Low)	I_O = 0.5A I_O = 3A		0.25 1	0.5 2	V V
SR	Slew Rate			4		V/µs
B	Gain Bandwidth Prod			10		MHz
G_V	Open Loop Voltage Gain	f = 1KHz		85		dB
R_{IN}	Input Resistance			150		MΩ
E_{IN}	Input Noise Voltage	R_s = 0 to 10KΩ f = 22Hz to 22KHz		3		µV
CMRR	Common Mode Rejection Ratio		75	90		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	R_s = 0 f = 100Hz	75	90		dB
C_T	Crosstalk	f = 1KHz to 10KHz		80		dB

APPLICATION SUGGESTION

The high flexibility makes the L2750 suitable for a wide range of applications.

Motor Controller

The device can be utilized as a motor controller. Fig.1 represents a bidirectional DC motor control suitable for logic driving. In these kinds of application it is possible to take advantage of the high current capability of the L2750 for driving several types of low impedance motors in a broad range of applications. Moreover the low drop allows high start up currents even at lowest supply voltage.

Audio Applications

Another typical utilization of the L2750 concerns the audio field, as follows:

1) DRIVER FOR BOOSTER : The remarkably low distortion and noise makes the device proper to be used as high quality driver for main amplifiers (i.e. car radio boosters). An example is shown by Fig. 5, where the gain is set to 24 dB (see also the relevant characteristics).

2) CAR RADIO BOOSTER WITH DIFFERENTIAL INPUT : Fig. 10 shows an example of car radio booster, with a gain of 30 dB, that is specially recommended for active loudspeakers. Among its main feature is the differential input and subsequent high noise suppression. The typical output power delivered into a 4Ω load is 24W (V_S = 14.4V; d =10%), as shown by the characteristics enclosed.

Figure 1

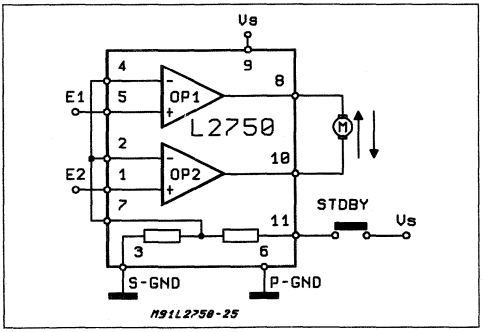


Figure 2: Low Drop Voltage vs. Output Current

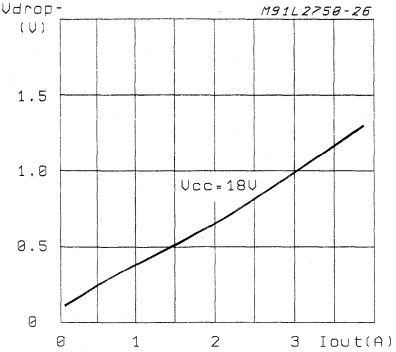


Figure 3: High Drop Voltage vs. Output Current

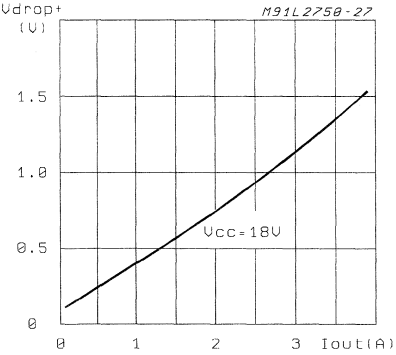


Figure 4: Open Loop Gain vs. Phase Response

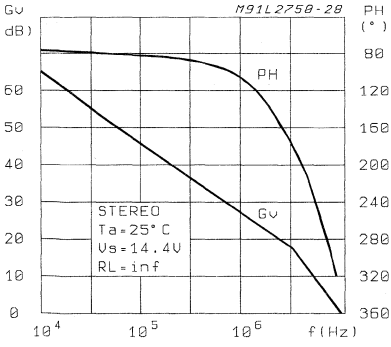


Figure 5: Stereo Audio Amplifier Application Circuit

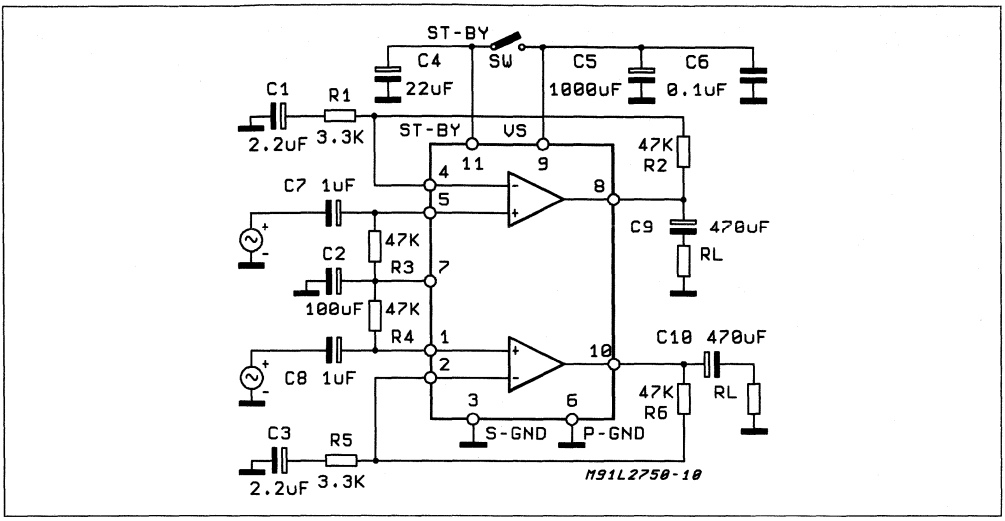
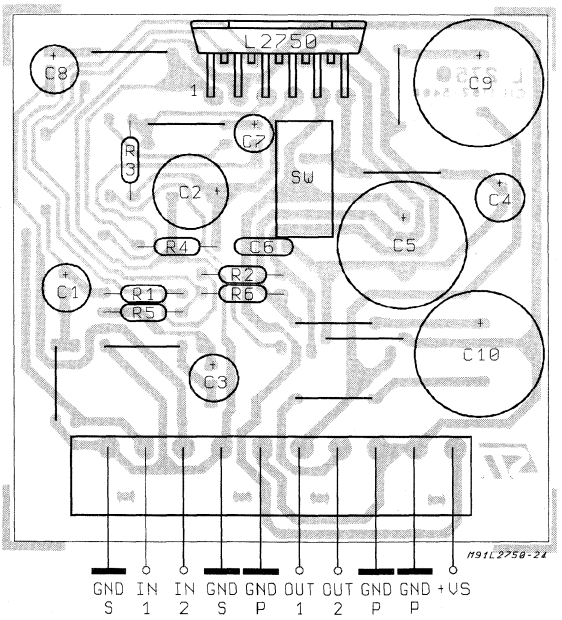


Figure 6: P.C. Board and Components Layout of the Circuit of Figure 5 (1:1 scale)



AUDIO STEREO APPLICATION CIRCUIT OF FIGURE 5

Figure 7: Quiescent Drain Current vs. Supply Voltage

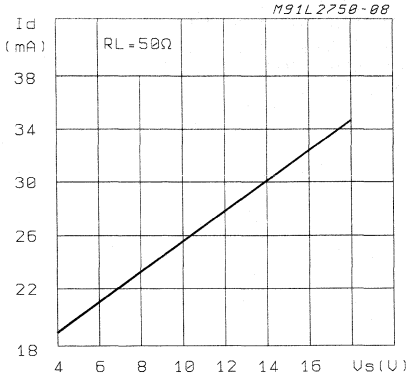


Figure 8: Distortion vs. Output Voltage

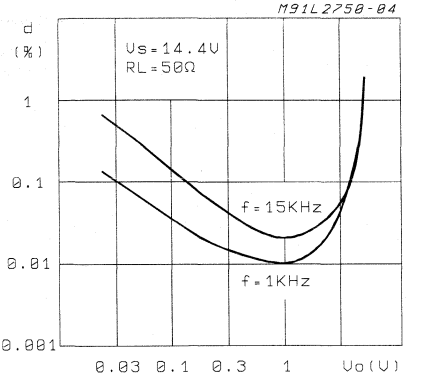


Figure 9: Distortion vs. Frequency

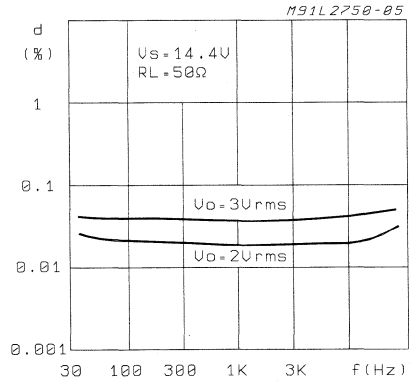


Figure 10: Cross-Talk vs Frequency

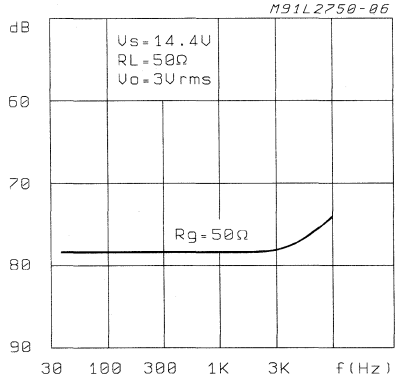


Figure 11: Supply Voltage Rejection vs. Frequency

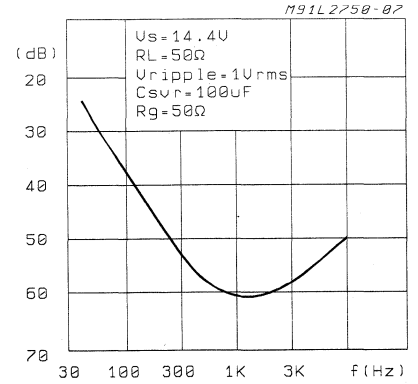


Figure 12: E_N Input vs. R_g

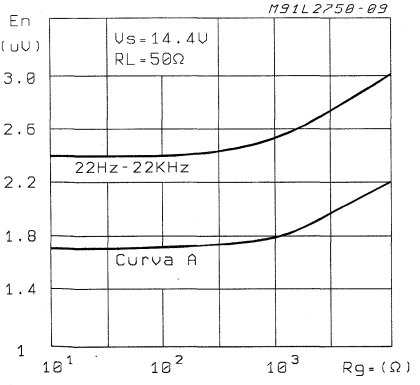


Figure 13: Bridge Power Amplifier with Balanced Input Application Circuit

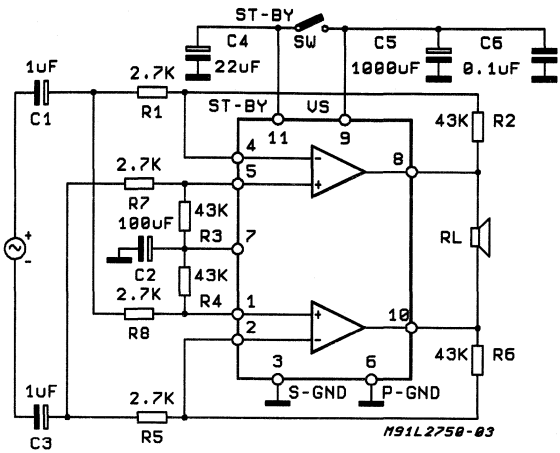
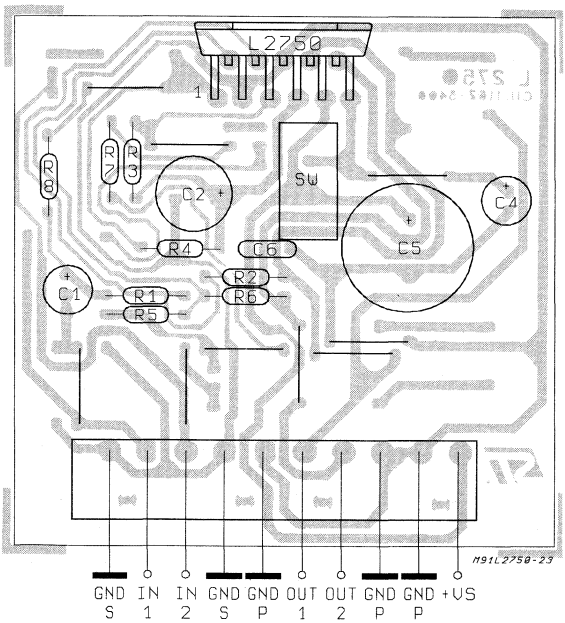


Figure 14: P.C. Board and Component Layout of the Circuit of Figure 13 (1:1 scale)



BRIDGE AUDIO APPLICATION CIRCUIT OF FIGURE 13

Figure 15: Quiescent Drain Current vs. Supply Voltage

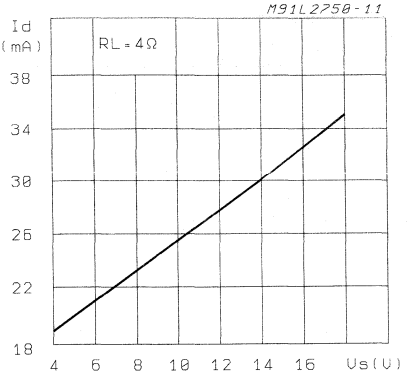


Figure 16: Noise vs. Rs

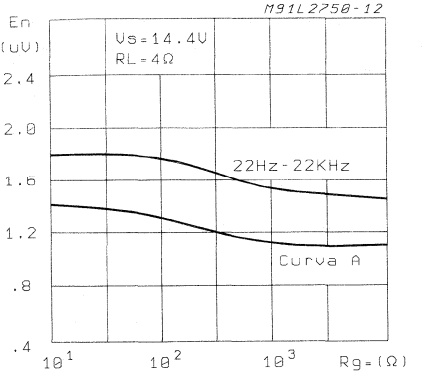


Figure 17: Output Power vs. Supply Voltage

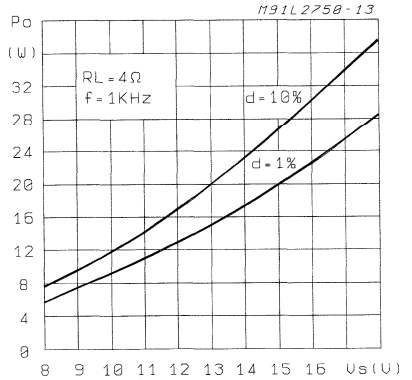


Figure 18: Output Power vs Supply Voltage

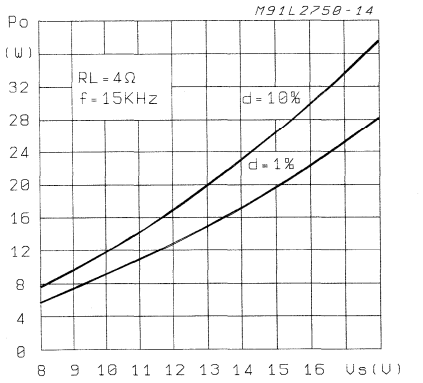


Figure 19: Distortion vs. Output Power

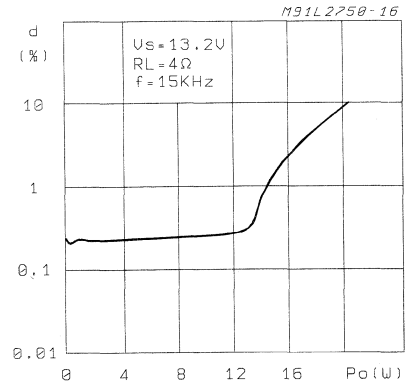


Figure 20: Distortion vs. Output Power

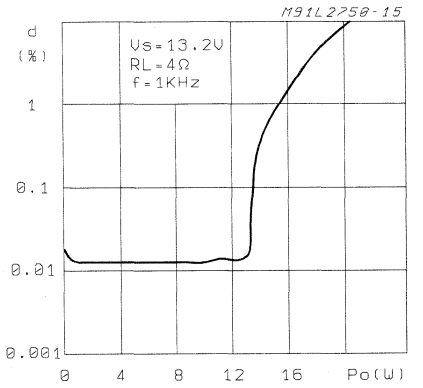


Figure 21: Distortion vs. Output Power

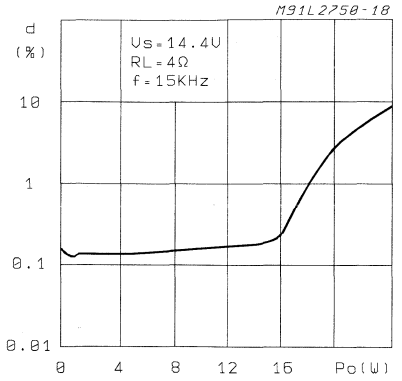


Figure 22: Distortion vs. Output Power

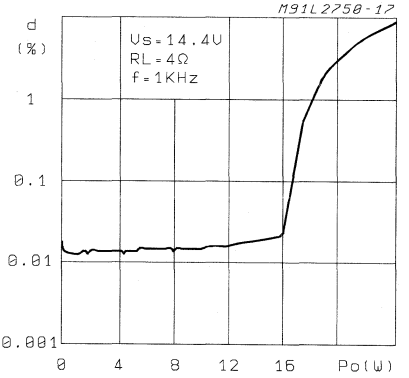


Figure 23: Distortion vs. Frequency

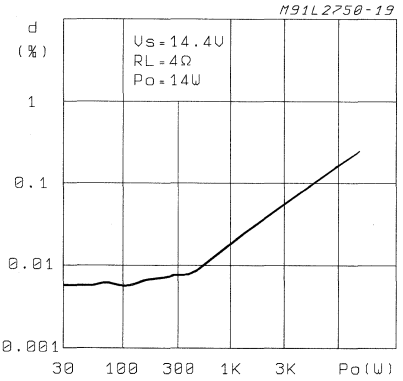


Figure 24: Supply Voltage Rejection vs. Frequency

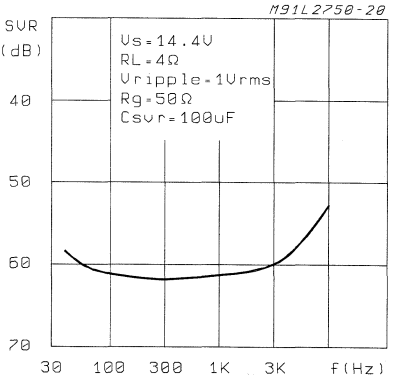


Figure 25: Total Power Dissipation and Efficiency vs. Output Power

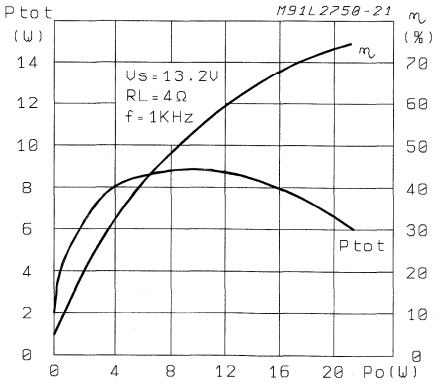
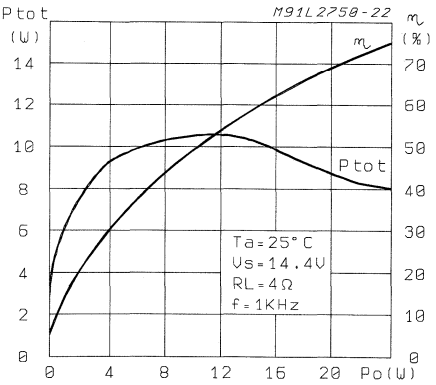


Figure 26: Total Power Dissipation and Efficiency vs. Output Power



2.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

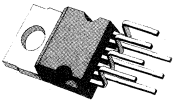
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external componénts.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



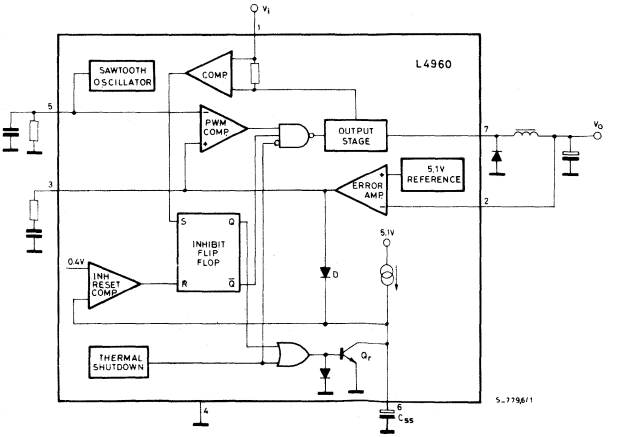
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

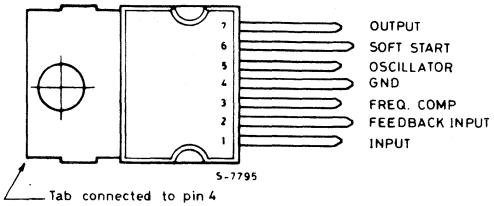
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_i = 46V$ $I_o = 1A$	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 2.5A$	9		46	V
ΔV_o	Line regulation	$V_i = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_i = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 2A$		1.4	3	V
I_{om}	Maximum operating load current	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	3		4.5	A
I_{SH}	Input average current	$V_i = 46V$; output short-circuit		30	60	mA
η	Efficiency	$f = 100KHz$ $V_o = V_{ref}$		75		%
		$I_o = 2A$ $V_o = 12V$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	$V_i = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 2A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

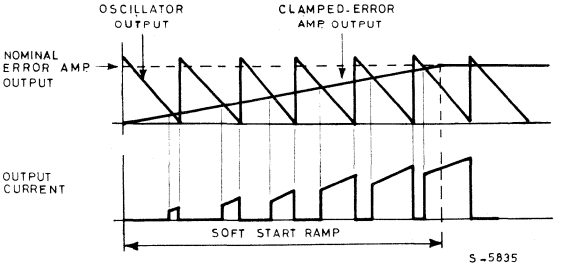


Fig. 2 - Current limiter waveforms

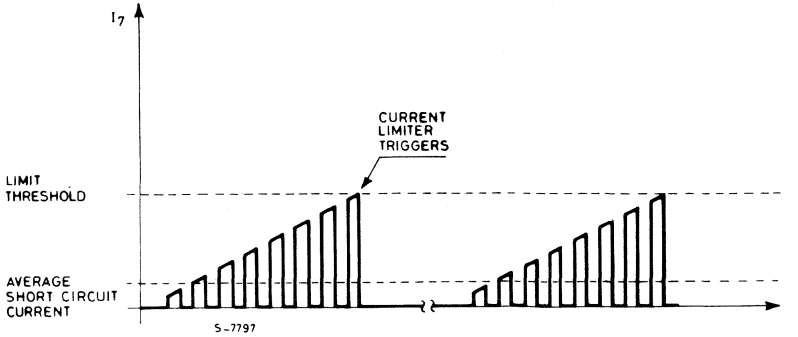
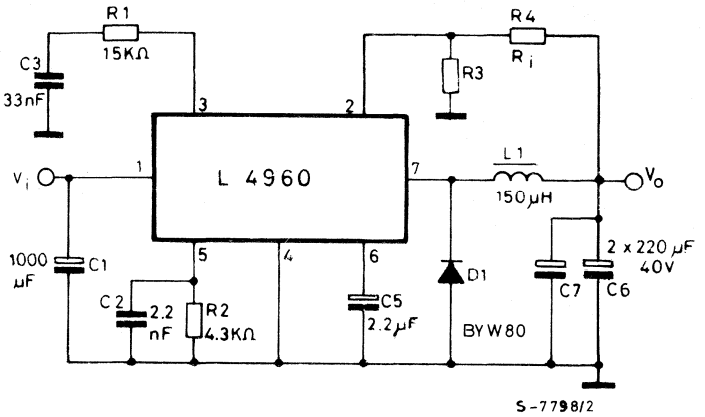


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150µH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

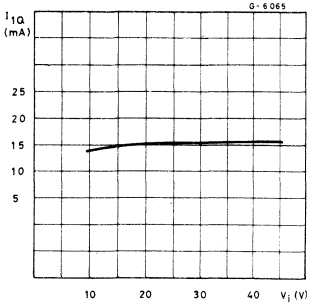


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

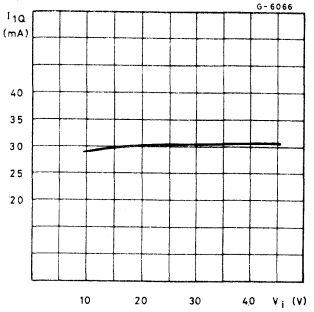


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

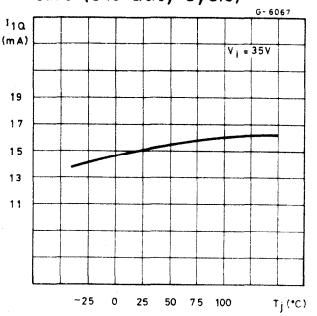


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

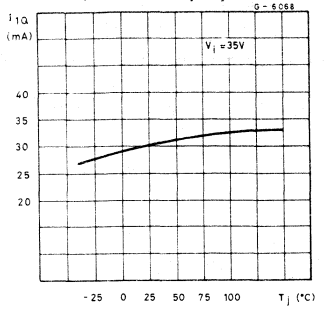


Fig. 8 - Reference voltage (pin 2) vs. V_i

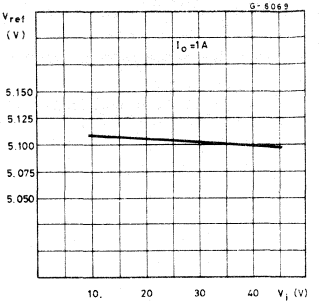


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

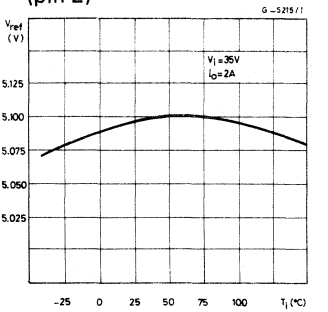


Fig. 10 - Open loop frequency and phase responde of error amplifier

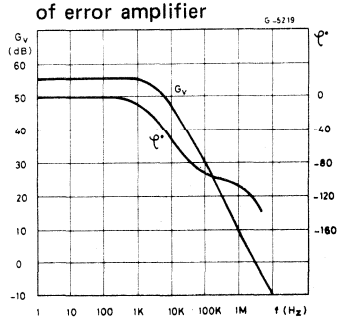


Fig. 11 - Switching frequency vs. input voltage

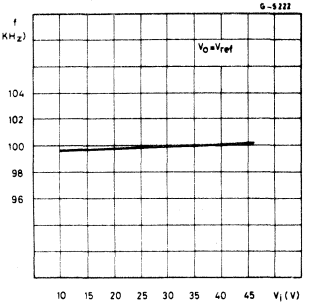


Fig. 12 - Switching frequency vs. junction temperature

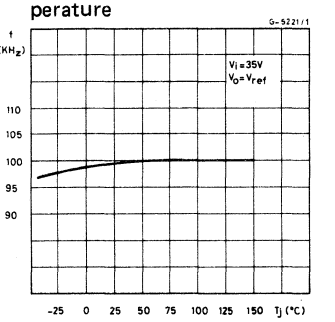


Fig. 13 - Switching frequency vs. R2 (see test circuit)

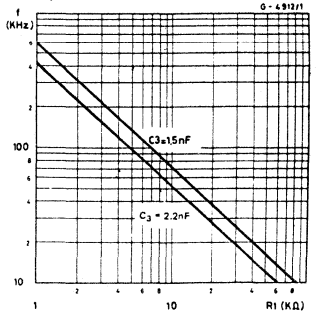


Fig. 14 - Line transient response

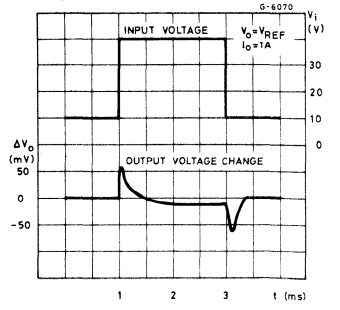


Fig. 15 - Load transient response

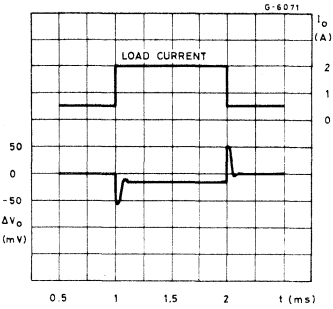


Fig. 16 - Supply voltage ripple rejection vs. frequency

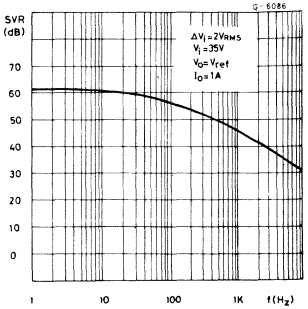


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

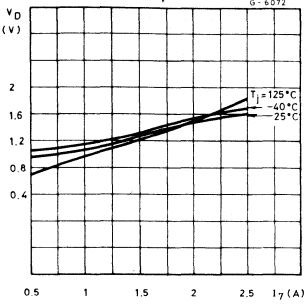


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

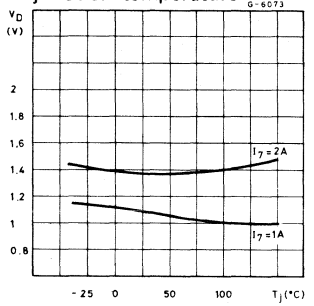


Fig. 19 - Power dissipation derating curve

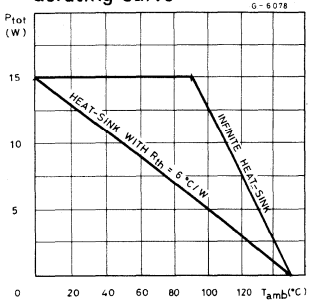


Fig. 20 - Efficiency vs. output current

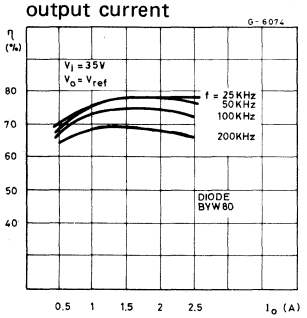


Fig. 21 - Efficiency vs. output current

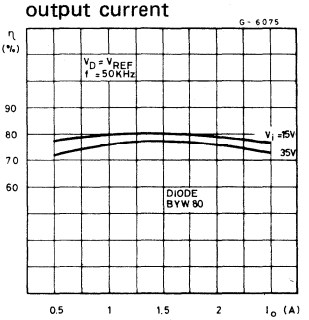


Fig. 22 - Efficiency vs. output current

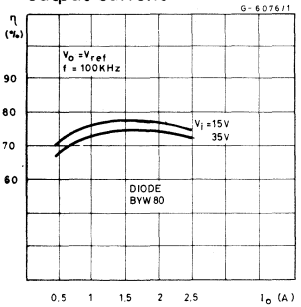
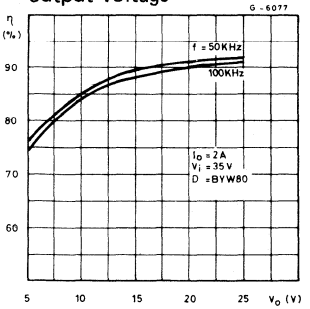
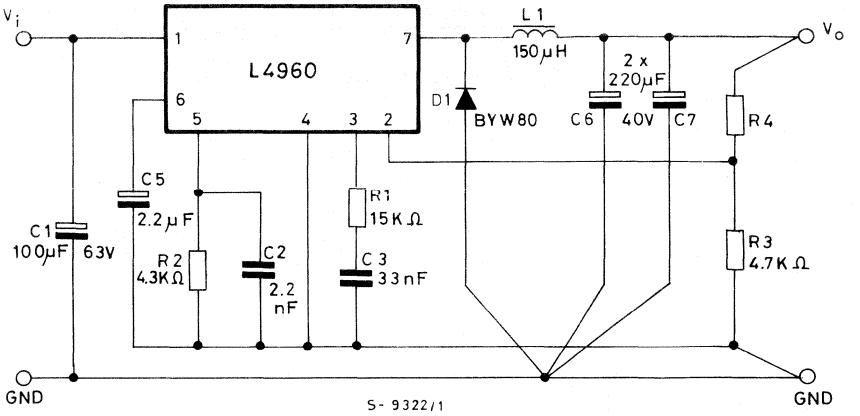


Fig. 23 - Efficiency vs. output voltage



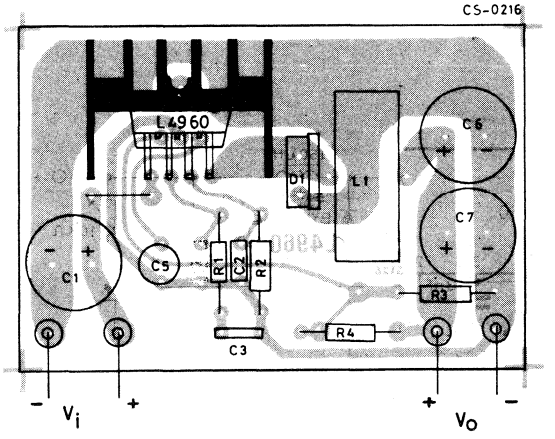
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

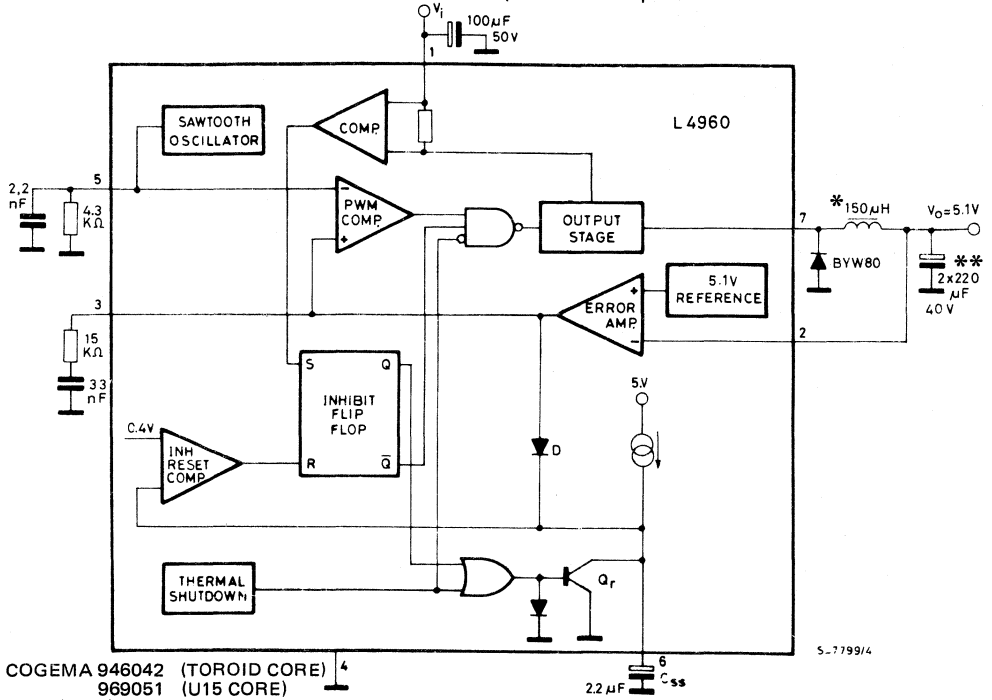
Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

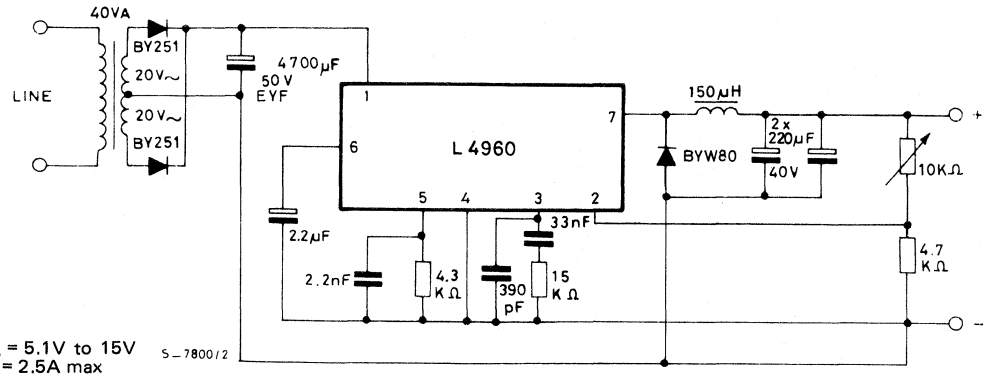
Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946042 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

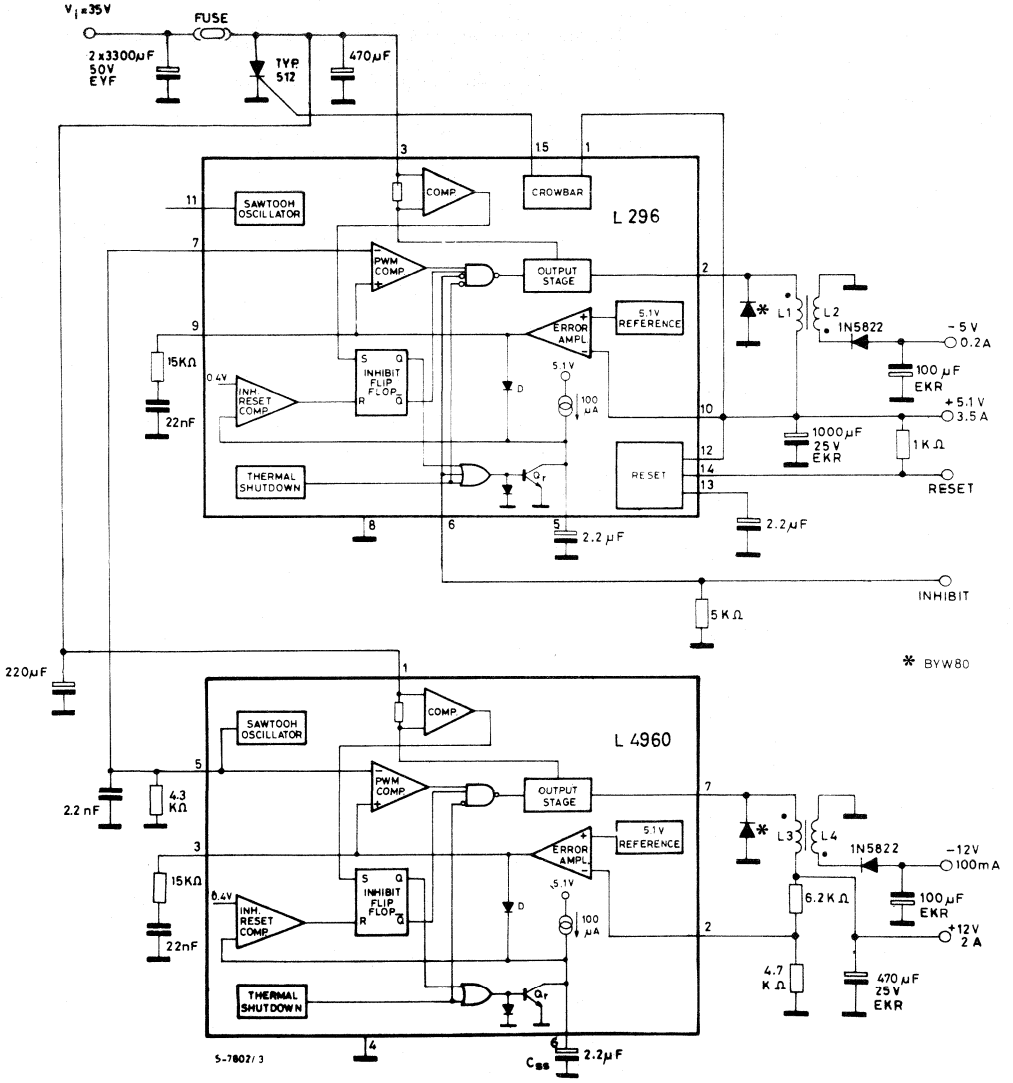
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

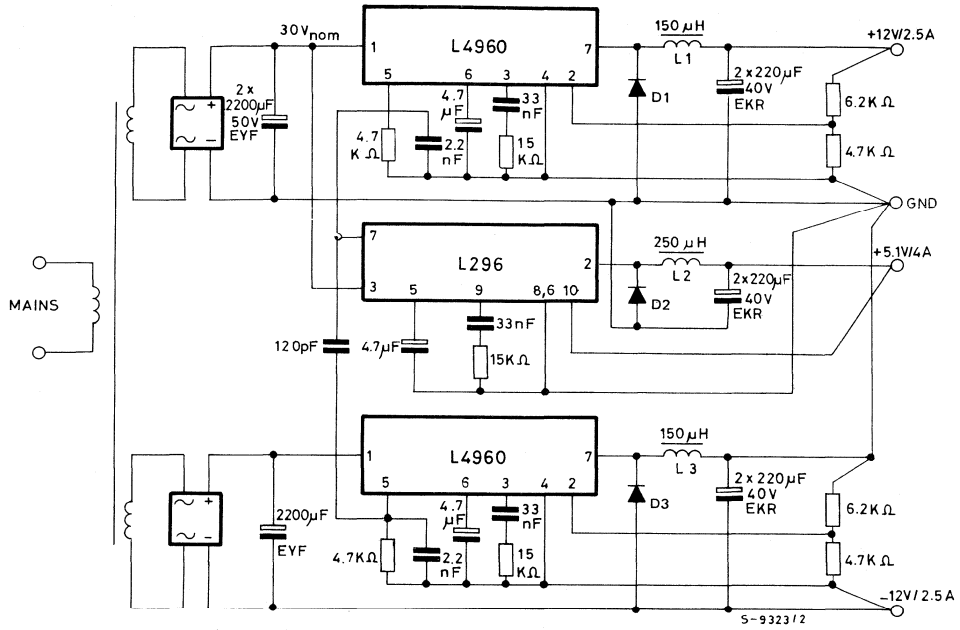
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



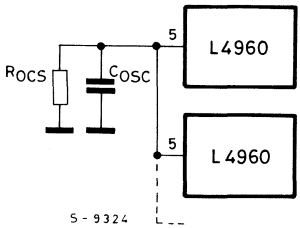
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



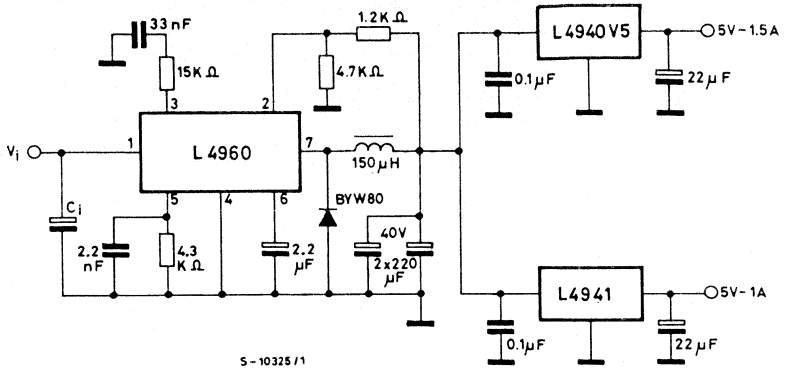
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

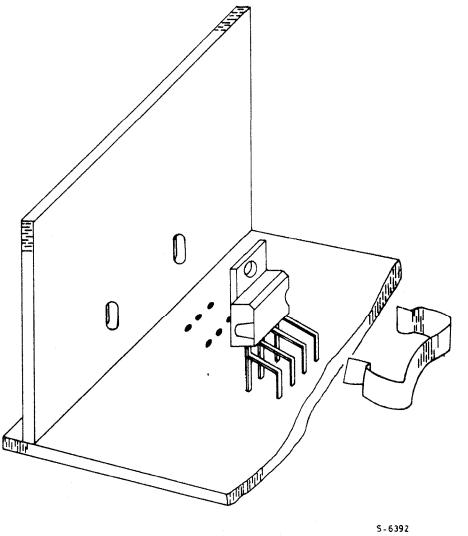
Fig. 31 - Regulator for distributed supplies



MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



1.5A POWER SWITHING REGULATOR

PRELIMINARY DATA

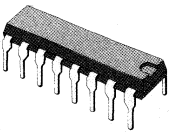
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

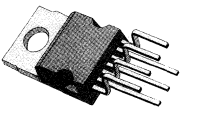
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

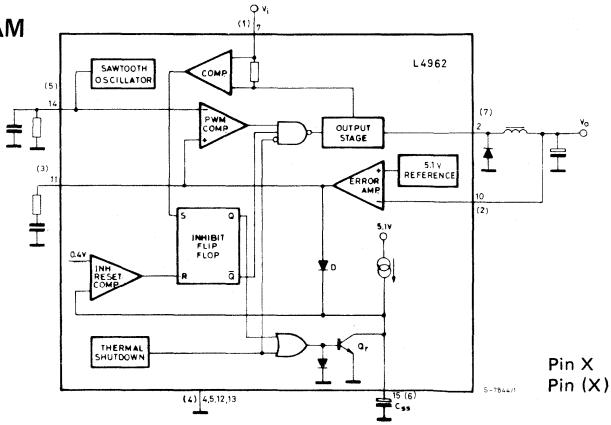
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

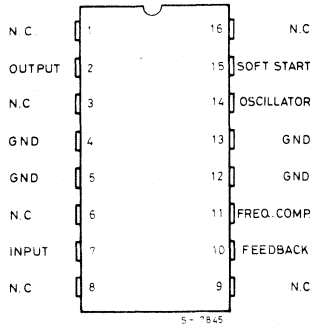
V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

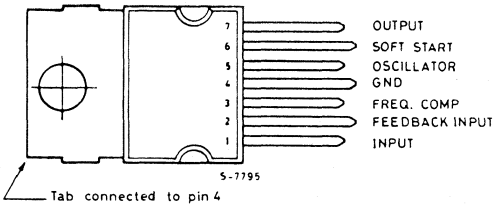
BLOCK DIAGRAM



CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	—
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	—	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	V_i = 46V I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	V_o = V_{ref} to 36V I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V V_o = V_{ref} I_o = 1A		15	50	mV
ΔV_o	Load regulation	V_o = V_{ref} I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A		0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A		1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V V_o = V_{ref} to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V V_o = V_{ref} to 36V	2		3.3	A
I_{SH}	Input average current	V_i = 46V; output short-circuit		15	30	mA
η	Efficiency	f = 100KHz V_o = V_{ref}		70		%
		I_o = 1A V_o = 12V		80		%
SVR	Supply voltage ripple rejection	ΔV_i = $2V_{rms}$ f_{ripple} = 100Hz V_o = V_{ref} I_o = 1A	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C		1		%
f_{max}	Maximum operating switching frequency	V_o = V_{ref} I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

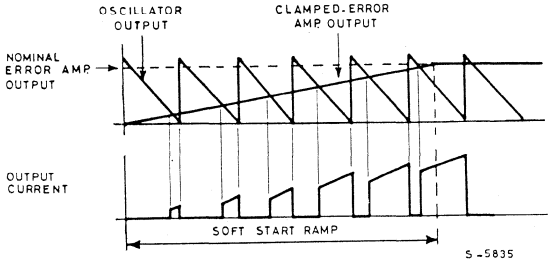


Fig. 2 - Current limiter waveforms

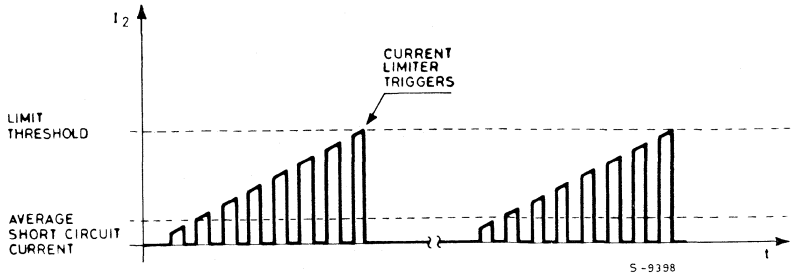
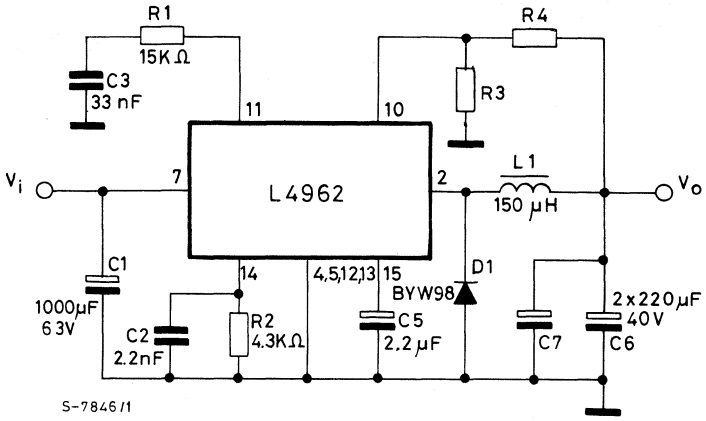


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

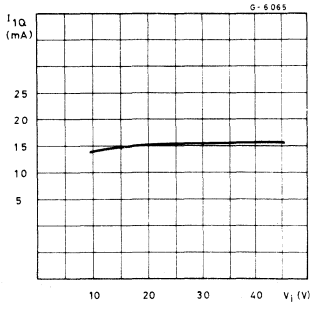


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

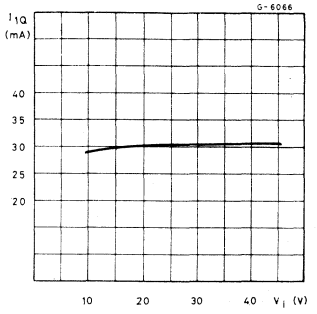


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

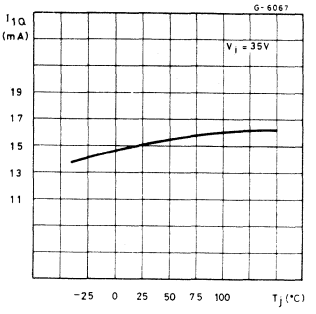


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

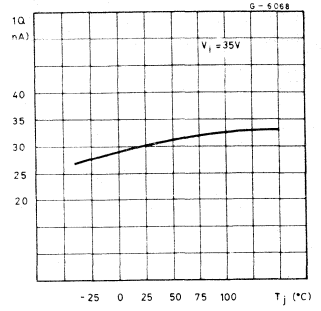


Fig. 8 - Reference voltage (pin 10) vs. V_i rdip) vs. V_i

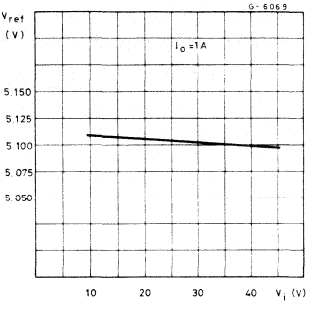


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

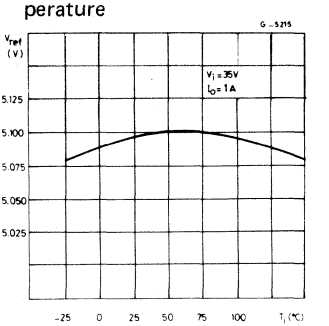


Fig. 10 - Open loop frequency and phase response of error amplifier

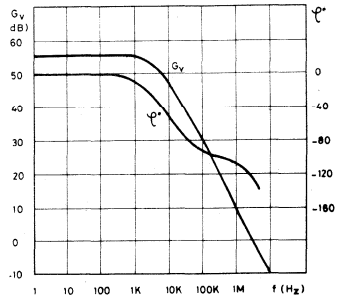


Fig. 11 - Switching frequency vs. input voltage

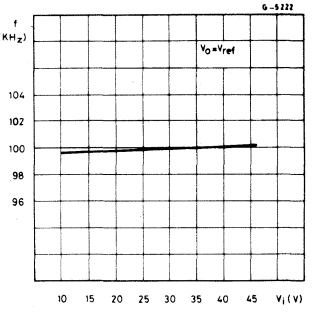


Fig. 12 - Switching frequency vs. junction temperature

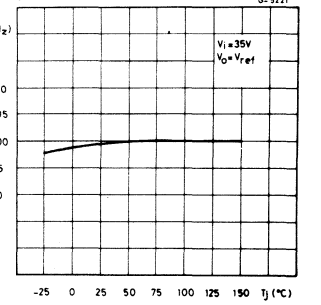


Fig. 13 - Switching frequency vs. R2 (see test circuit)

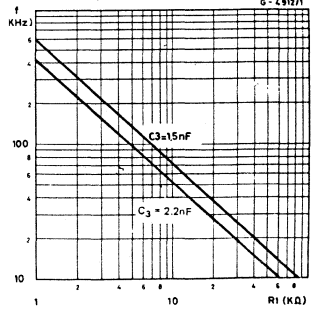


Fig. 14 - Line transient response

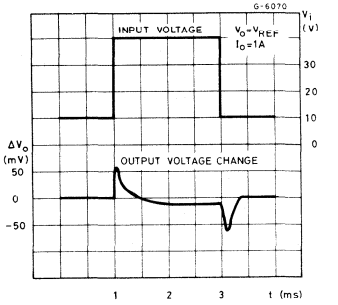


Fig. 15 - Load transient response

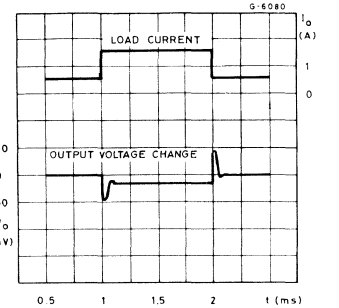


Fig. 16 - Supply voltage ripple rejection vs. frequency

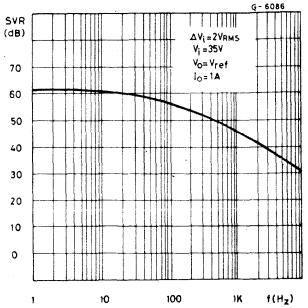


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

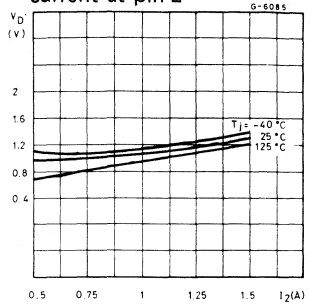


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

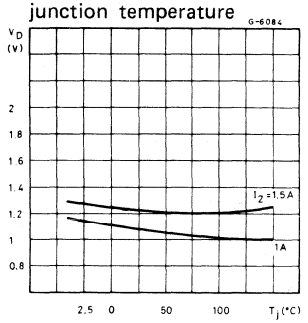


Fig. 19 - Efficiency vs. output current

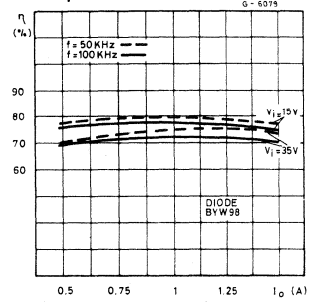


Fig. 20 - Efficiency vs. output current

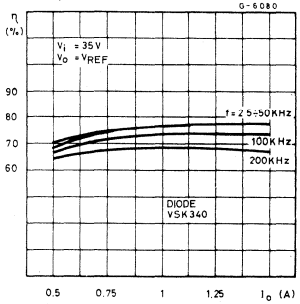


Fig. 21 - Efficiency vs. output current

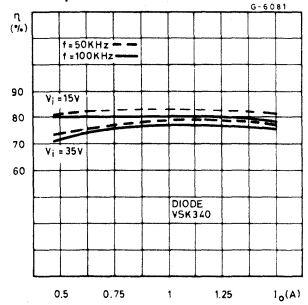


Fig. 22 - Efficiency vs. output voltage

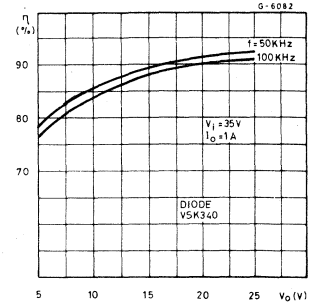


Fig. 23 - Efficiency vs. output voltage

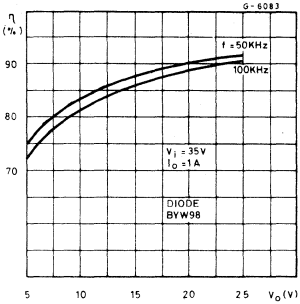
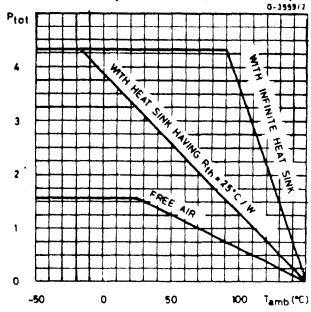
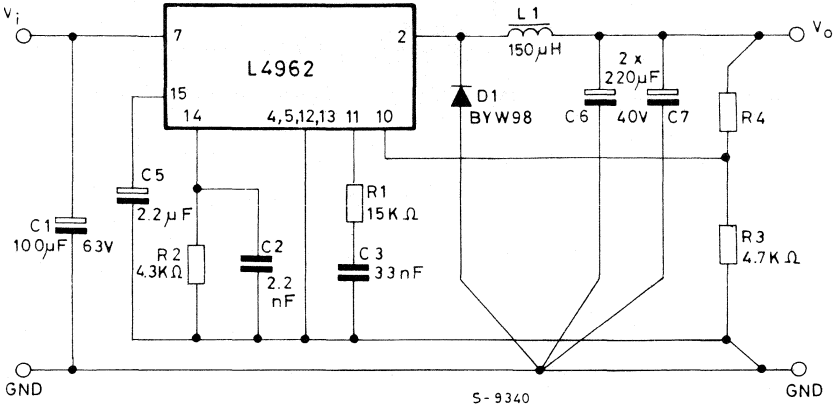


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



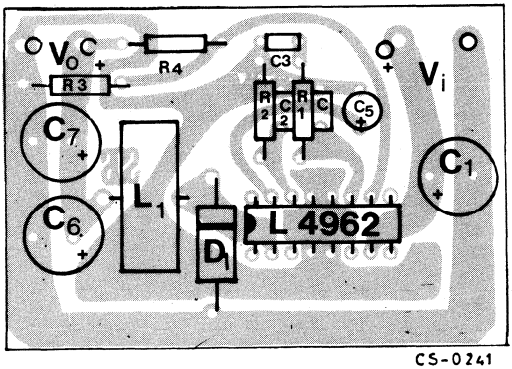
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

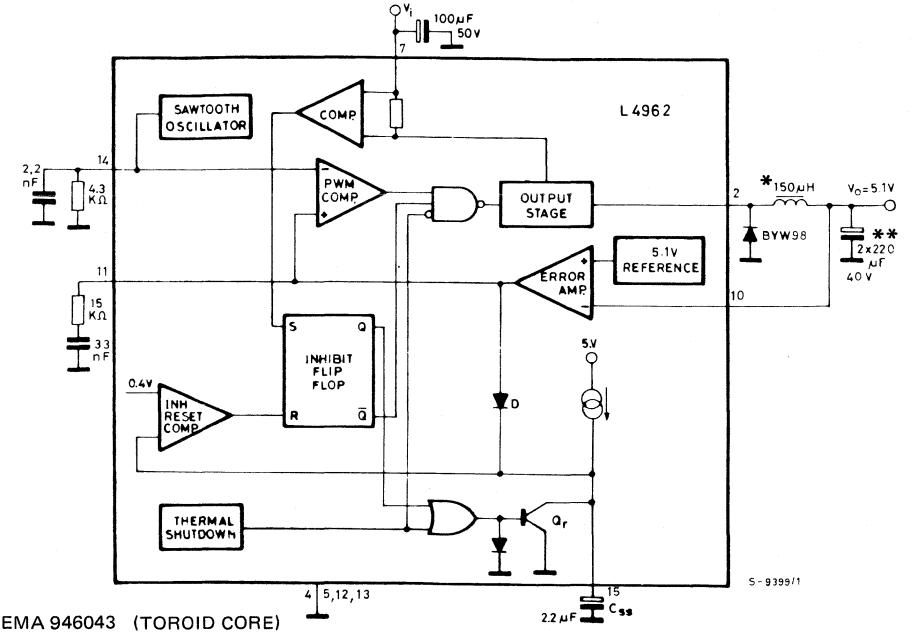
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

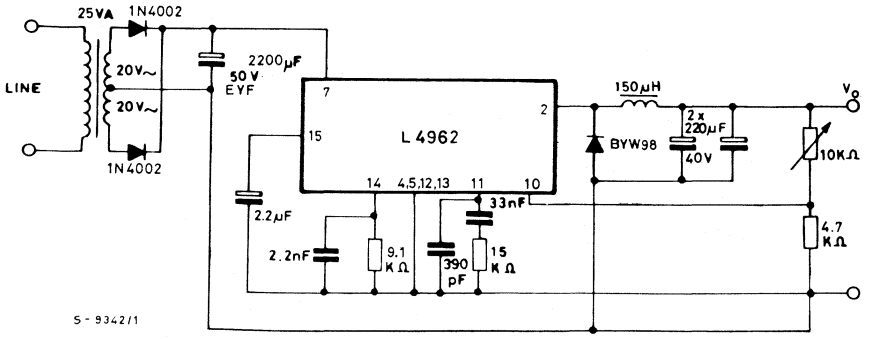
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

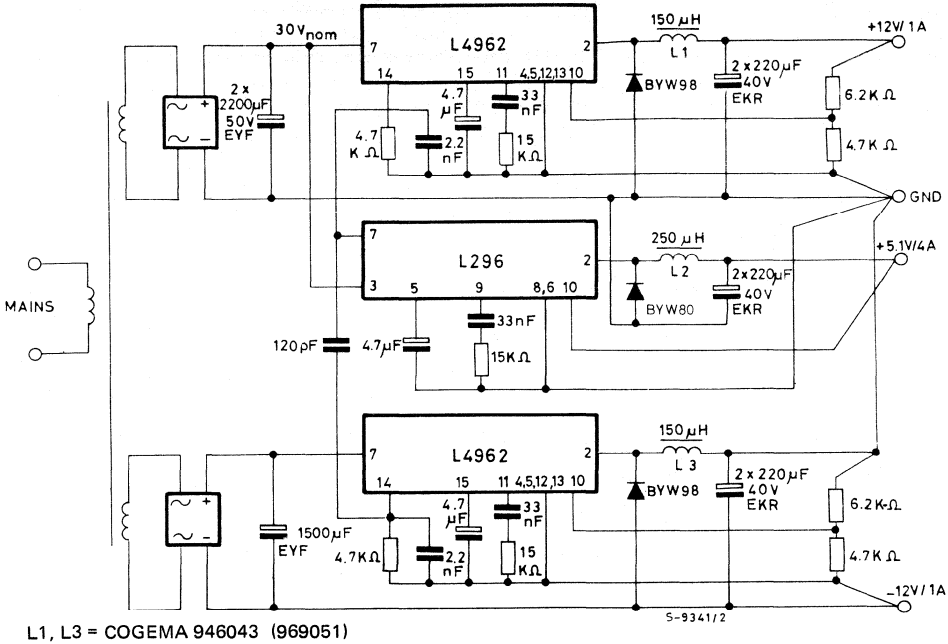
Fig. 28 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

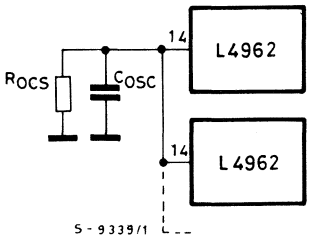
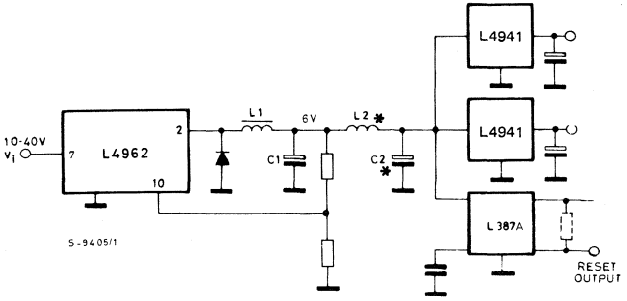


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

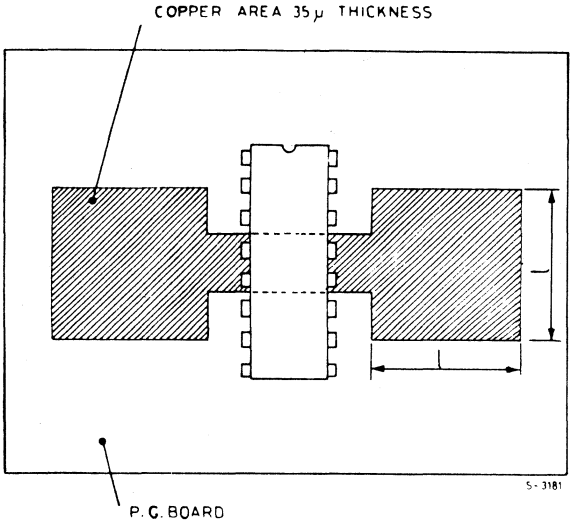
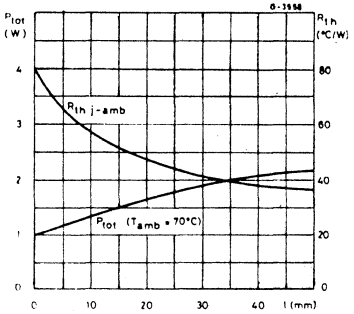
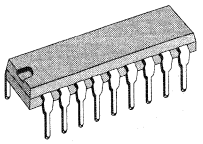


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

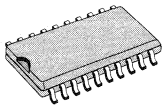


1.5A SWITCHING REGULATOR

- 1.5A OUTPUT LOAD CURRENT
- 5.1 TO 36V OUTPUT VOLTAGE RANGE
- DISCONTINUOUS VARIABLE FREQUENCY MODE
- PRECISE (+/–2%) ON CHIP REFERENCE
- VERY HIGH EFFICIENCY
- VERY FEW EXTERNAL COMPONENTS
- NO FREQ. COMPENSATION REQUIRED
- RESET AND POWER FAIL OUTPUT FOR MICROPROCESSOR
- INTERNAL CURRENT LIMITING
- THERMAL SHUTDOWN



Powerdip12+3+3



SO20

ORDERING NUMBERS:

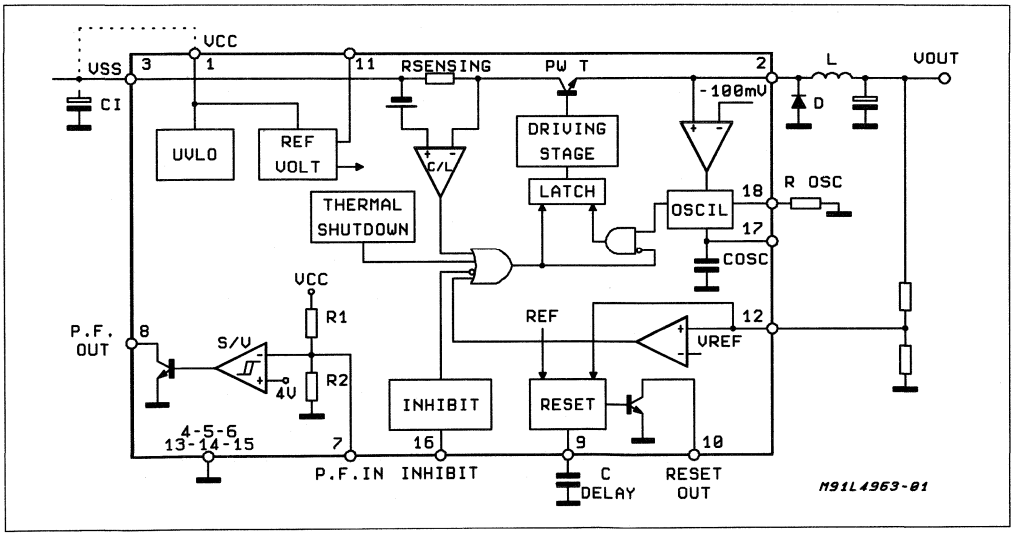
L4963W L4963D

DESCRIPTION

The L4963 is a monolithic power switching regulator delivering 1.5A at 5.1V. The output voltage is adjustable from 5.1V to 36V, working in discontinuous variable frequency mode. Features of the device include remote inhibit, internal current limiting and thermal protection, reset and power fail outputs for microprocessor.

The L4963 is mounted in a 12+3+3 lead Powerdip (L4963) and SO20 large (L4963D) plastic packages and requires very few external components.

BLOCK DIAGRAM

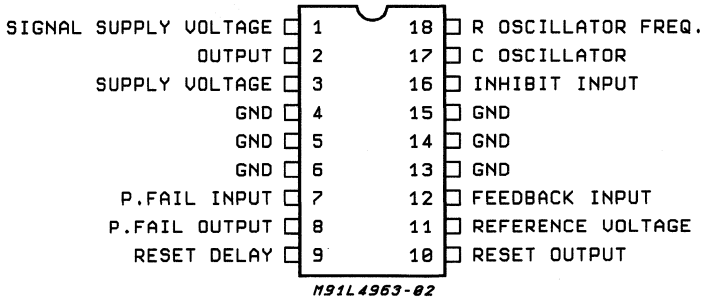


ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
SO20	Powerdip			
V_i		Input Voltage (pin 1 and pin 3 connected togheter)	47	V
V_3–V_2		Input to Output Voltage Difference	47	V
V_2		Negative Output DC Voltage	–1	V
V_2		Negative Output Peak Voltage at t=0.2 µs, f=50kHz	–5	V
V_8	V_7	Power Fail Input	25	V
V_9, V_{11}	V_8, V_{10}	Reset and Power Fail Output	V_i	
V_{10}	V_9	Reset Delay Input	5.5	V
V_{13}, V_{18}	V_{12}, V_{16}	Feedback and Inhibit Inputs	7	V
V_{19}, V_{20}	V_{17}, V_{18}	Oscillator Inputs	5.5	V
P_{tot}		Total Power Dissipation Tpins ≤ 90°C (Power DIP) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C, 4cm^2 copper area on PCB)	5 1.3 2	W W W
T_{stg}, T_j		Storage & Junction Temperature (Tamb = 70°C 6cm^2 copper area on PCB)	–40 to 150 1.45	°C W
P_{tot}		Total Power Dissipation Tpins ≤90°C (SO20L)	4	W

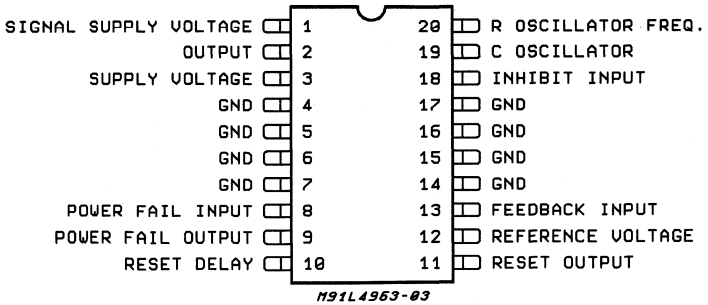
PIN CONNECTION (top view)

Powerdip18



M91L4963-02

SO20



M91L4963-03

PIN FUNCTIONS

SO20L	Power DIP	Name	Description
1	1	SIGNAL SUPPLY VOLTAGE	Must be Connected to pin 3
2	2	OUTPUT	Regulator output
3	3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
4, 5, 6, 7 14, 15, 16, 17	4, 5, 6 13, 14, 15	GROUND	Common ground terminal
8	7	POWER FAIL INPUT	Input of the power fail circuit. The threshold can be modified introducing an external voltage divider between the Supply Voltage and GND.
9	8	POWER FAIL OUTPUT	Open collector power fail signal output. This output is high when the supply voltage is safe.
10	9	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
11	10	RESET OUTPUT	Open collector reset signal output. This output is high when the output voltage value is correct.
12	11	REFERENCE VOLTAGE	Reference voltage output.
13	12	FEEDBACK INPUT	Feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
18	16	INHIBIT INPUT	TTL level remote inhibit. A logic low level on this input disables the device.
19	17	C OSCILLATOR	Oscillator waveform. A capacitor connected between this terminal and ground modifies the maximum oscillator frequency.
20	18	R OSCILLATOR FREQ.	A resistor connected between this terminal and ground defines the maximum switching frequency.

THERMAL DATA

Symbol	Parameter		SO20	Powerdip	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction to Pins	max.	15	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient (*)	max.	85	80	°C/W

(*) See Fig. 28

CIRCUIT DESCRIPTION (Refer to Block Diagram)

The L4963 is a monolithic stepdown regulator providing 1.5A at 5.1V working in discontinuous variable frequency mode. In normal operation the device resonates at a frequency depending primarily on the inductance value, the input and output voltage and the load current. The maximum switching however can be limited by an internal oscillator, which can be programmed by only one external resistor.

The fondamental regulation loop consists of two comparators, a precision 5.1V on-chip reference and a drive latch. Briefly the operation is as follows: when the choke ends its discharge the catch freewheeling recirculation filter diode begins to come but of forward conduction so the output voltage of the device approaches ground. When the output voltage reaches –0.1V the internal comparator sets the latch and the power stage is turned on. Then the inductor current rises linearly until the voltage sensed at the feedback input reaches the 5.1V reference.

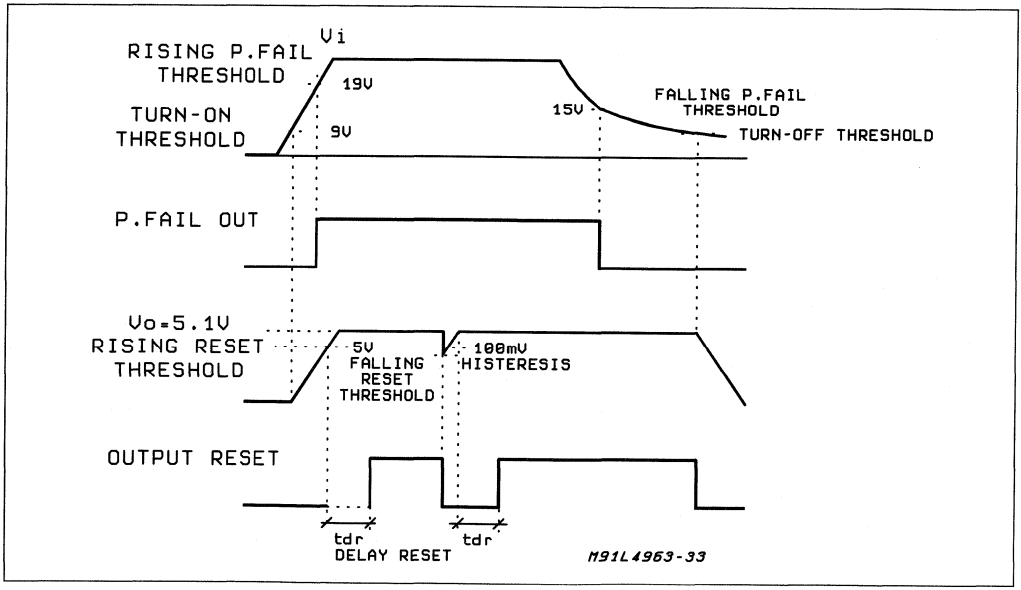
The second comparator then resets the latch and the output stage is turned off. The current in the choke falls linearly until it is fully discharged, then the cycle repeats. Closing the loop directly gives an output voltage of 5.1V. Higher output voltages are obtained by inserting a voltage divider and this method of control requires no frequency compensation network. At output voltages greater than 5.1V the available output current must be derated due to the increased power dissipation of the device.

Output overload protection is provided by an internal current limiter. The load current is sensed by a on-chip metal resistor connected to a comparator which resets the latch and turns off the power stage in overload condition. The reset circuits (see fig. 1) generates an output high signal when the output voltage value is correct. It has an open collector output and the output signal delay time can be programmed with an external capacitor. A power-fail circuit is also available and is used to monitor the supply voltage. Its output goes high when the supply voltage reaches a pre-programmed treshold set by a voltage divider to its input from the supply to ground. With the input left open the threshold is approximately equal to 5.1V. The output of the power fail is an open collector.

A TTL level inhibit is provided for applications such as remote on/off control. This input is activated by a low logic level and disables circuits operation.

The thermal overload circuit disables the device when the junction temperature is about 150°C and has hysteresis to prevent unstable conditions.

Figure 1: Reset and Power Fail Function



ELECTRICAL CHARACTERISTIC (Refer to the test circuit V_i = 30V T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS							
V_o	Output Voltage Range	V_i = 46V I_o = 0.5A	V_{ref}		36	V	2
V_i	Input Voltage Range	V_o = V_{ref} to 36V I_o = 0.5A	9		46	V	2
V_{12}	Feedback Voltage	V_i = 9 to 46V I_o = 0.5A	5	5.1	5.2	V	2
I_{12}	Input Bias Current	V_i = 15V V_{12} = 6V V_{17f} = 5V		5	20	µA	3a
V_{OS12}	Input Offset Voltage			5	10	mV	3a
ΔV_o	Line Regulation	V_i = 9 to 46V V_o = V_{ref} I_o = 0.5A		15	50	mV	2
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5 to 1.5A		15	45	mV	2
V_d	Dropout Voltage Between pin 3 and pin 2	I_2 = 3A V_i = 20V		1.5	2	V	2
I_{2L}	Current Limiting	V_i = 9 to 46V V_o = V_{ref} to 28V	3.5		6.5	A	2
I_o	Maximum Operating Load Current	V_i = 9 to 46V V_o = V_{ref}	1.5			A	2
SVR	Supply Voltage Ripple Rejection	V_i = 2Vrms V_o = V_{ref} fripple = 100Hz I_o = 1.5A	50	56		dB	2
V_{11}	Reference Voltage	V_i = 9 to 46V O < I_{11} < 5mA	5	5.1	5.2	V	3a
	Average Temperature Coefficient of Ref. Volt.	T_j = 0 to 125 °C		0.4		mV/°C	–
ΔV_{11}	V_{ref} Line Regulation	V_i = 9 to 46V		10	20	mV	3a
ΔV_{11}	V_{ref} Line Regulation	I_{ref} = 0 to 5mA V_i = 46V R_{osc} = 51KΩ	65 69	7	15	mV	3a
η	Efficiency	I_o = 1.5A V_o = V_{ref}	65	75		%	2
T_{sd}	Thermal Shutdown Junction Temperature		145	150		°C	–
	Hysteresis			30		°C	–
DC CHARACTERISTICS							
I_q	Quescent Drain Current	V_i = 46V I_o = 0mA	V_{16} = V_{12} = 0		14	20	mA	3a
			V_{16} = V_{ref} V_{12} = 5.3V		11	16	mA	3a
INHIBIT							
V_{16L}	Low Input Voltage	V_i = 9 to 46V	0.3		0.8	V	2
V_{16H}	High Input Voltage	V_i = 9 to 46V	2		5.5	V	2
I_{16L}	Input Current with Low Input Voltage	V_{16} = 0.8V		50	100	µA	2
I_{16L}	Input Current with High Input Voltage	V_{16} = 2V		10	20	µA	2

ELECTRICAL CHARACTERISTIC (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
RESET							
V_{12}	Rising Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –100	V_{ref} –50	mV	3b
V_{12}	Falling Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –200	V_{ref} –250	mV	3b
V_{9D}	Delay Rising Thereshold Voltage	V_7 = OPEN	4.3	4.5	4.7	V	3b
V_{9F}	Delay Falling Thereshold Voltage		1	1.5	2	V	3b
$-I_{9SO}$	Delay Source Current	V_9 = 4.7V V_{12} = 5.3V	70	110	140	µA	3b
I_{9SI}	Delay Sink Current	V_9 = 4.7V V_{12} = 4.7V	10			mA	3b
I_{10}	Output Leakage Current	V_i = 46V V_7 = 8.5V	50			µA	3b
V_{10}	Output Saturation Volt.	I_{10} = 15mA; V_I = 3 to 46V			0.4	V	3b
POWER FAIL							
V_R	Rising Threshold Voltage	Pin7 = open	17.5	19	20.5	V	3C
V_F	Falling Threshold Voltage	Pin7 = open	14.25	15	15.75	V	3c
V_7	Rising Threshold Voltage	V_i = 20V	4.14	4.5	4.86	V	–
V_7	Falling Threshold Voltage	V_i = 20V	3.325	3.5	3.675	V	–
V_s	Output Saturation Volt.	I_a = 5mA			0.4	V	3c
I_s	Output Leakage Current	V_i = 46V			50	µA	3c
OSCILLATOR							
f	Oscillator Frequency	R_T = 51KΩ	46	60	79	kHz	–
f	Oscillator Frequency	V_I = 9 to 46V T_j = 0 to 125°C R_T = 51KΩ	42		83	kHz	–

Figure 2: Test Circuit

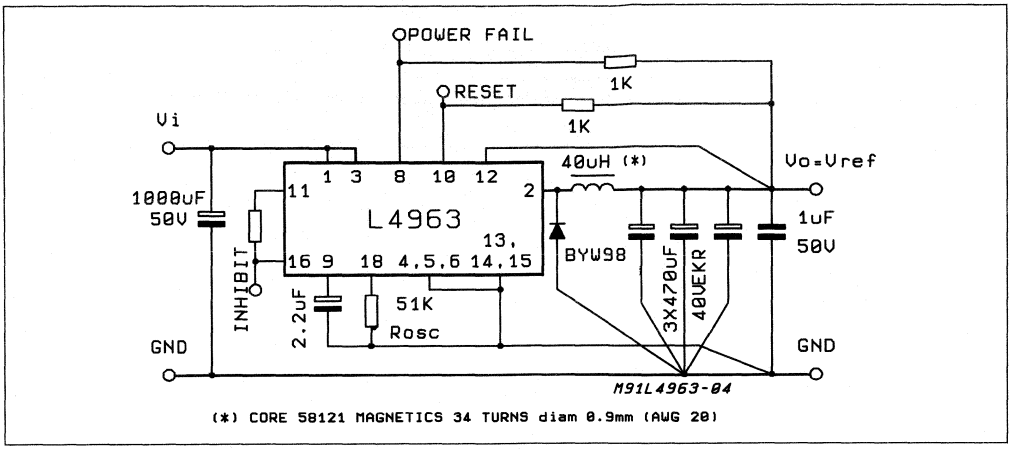


Figure 3: DC Test Circuit

Figure 3a

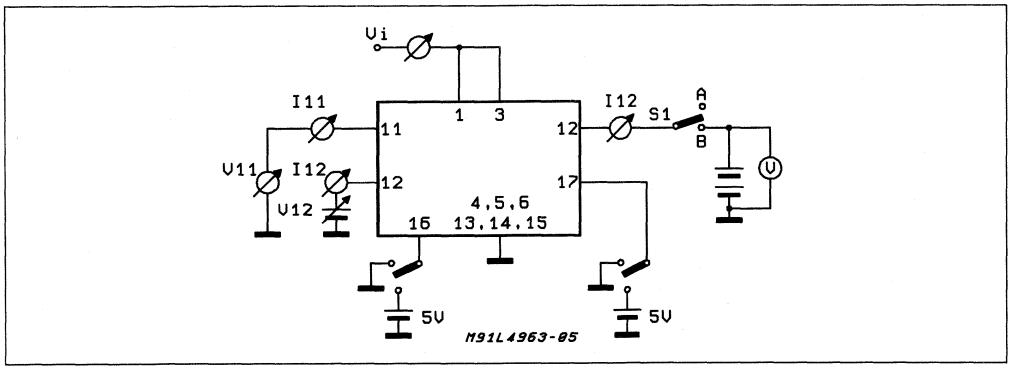


Figure 3b

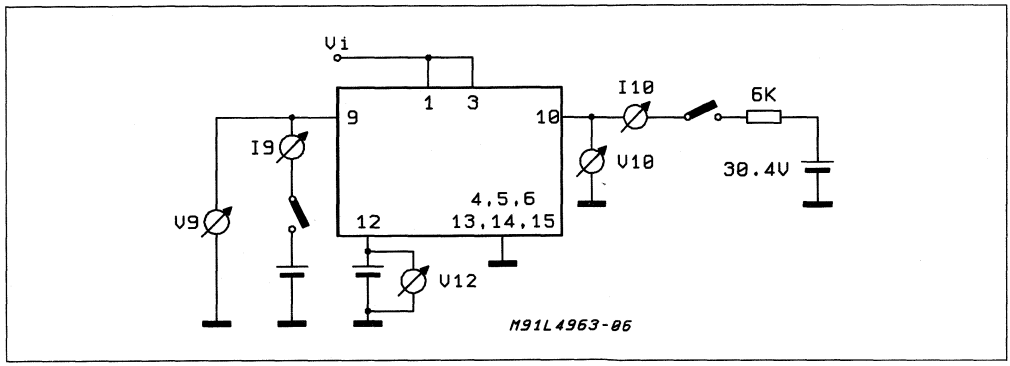


Figure 3c

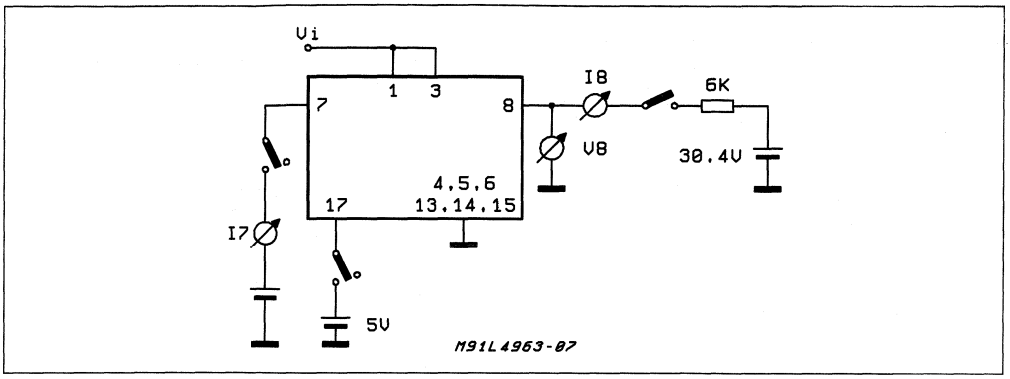


Figure 4: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

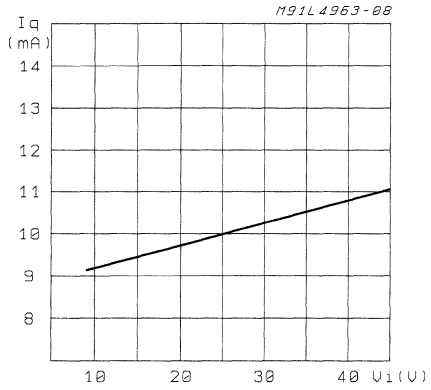


Figure 5: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)

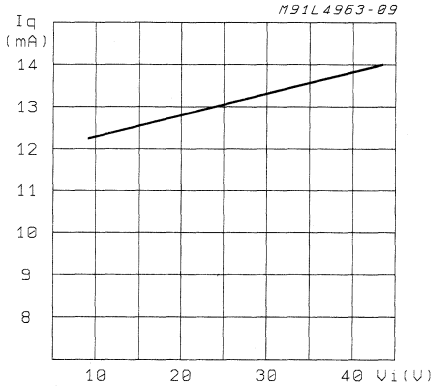


Figure 6: Quiescent Drain Current vs. Junction Temperature (0% Duty Cycle)

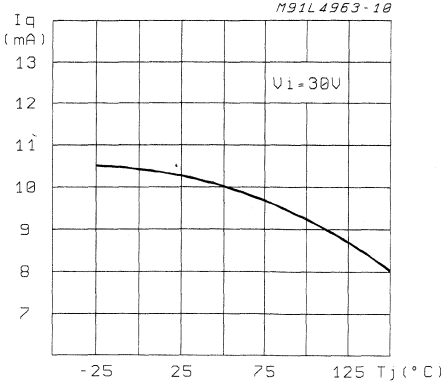


Figure 7: Quiescent Drain Current vs. Junction Temperature (100% Duty Cycle)

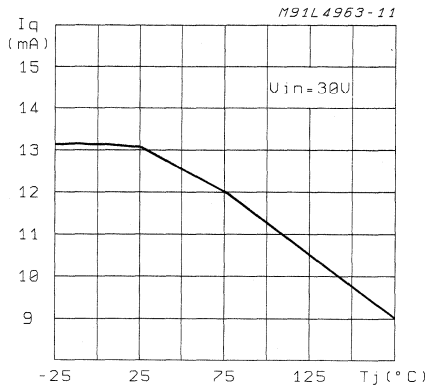


Figure 8: Reference Voltage vs. V_i

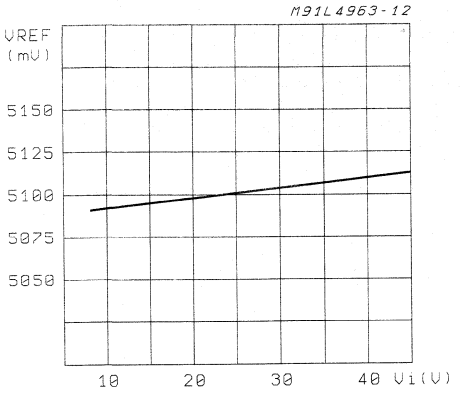


Figure 9: Reference Voltage vs. T_j

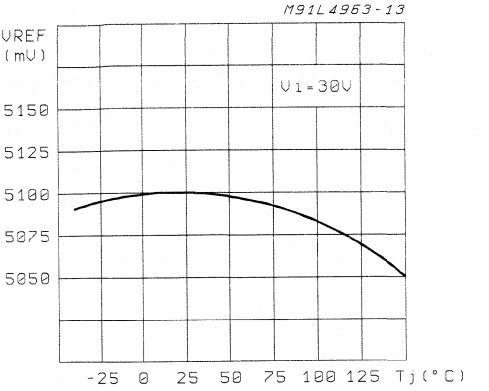


Figure 10: Line Transient Response

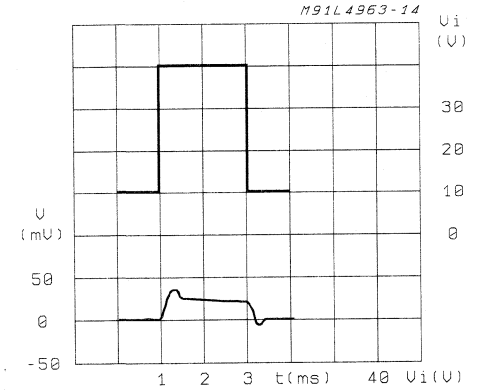


Figure 11: Load Transient

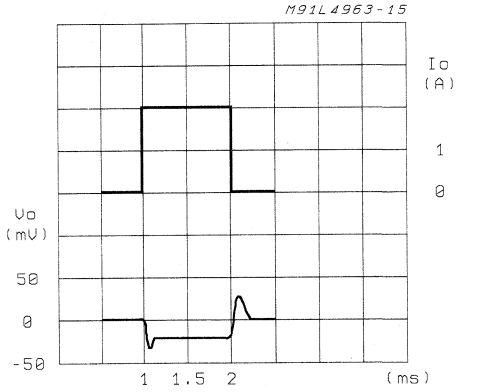


Figure 12: Supply Voltage Ripple Rejection vs. Frequency

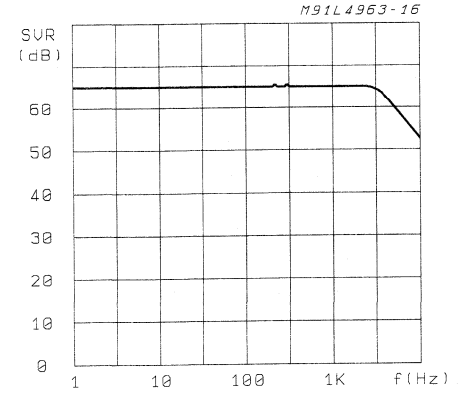


Figure 13: Dropout Voltage Between pi3 and 2 vs. Current at pin2

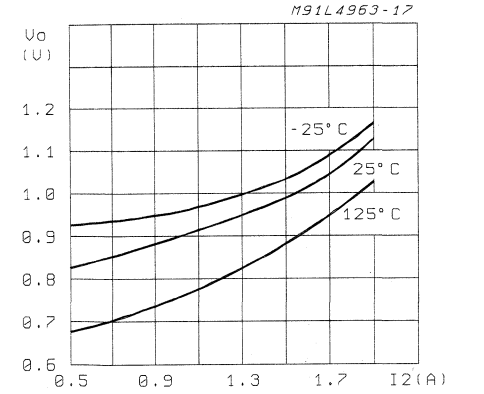


Figure 14: Dropout Voltage Between pin3 and 2 vs. Junction Temperature

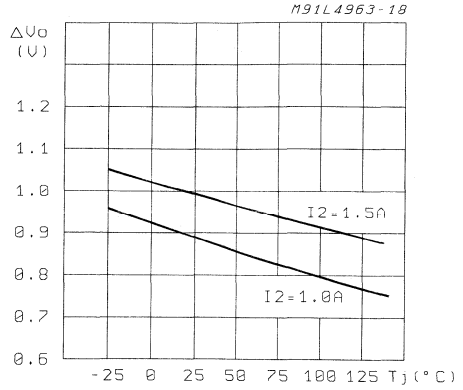


Figure 15: Maximum Allowable PowerDissipation vs. Ambient Temperature (Powerdip Package Only)

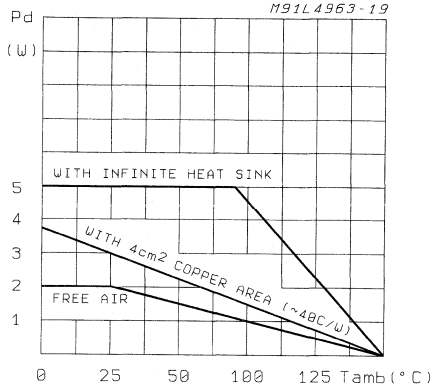


Figure 16: Power Dissipation (device only) vs. Input Voltage (Powerdip Package Only)

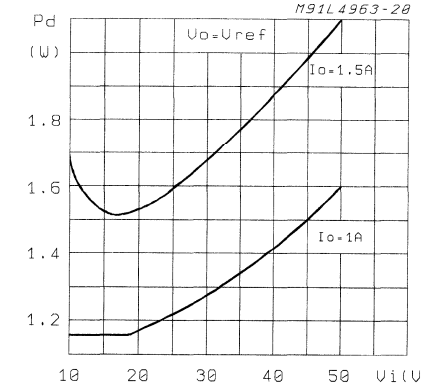


Figure 17: Power Dissipation (device only) vs. Output Voltage (Powerdip Package Only)

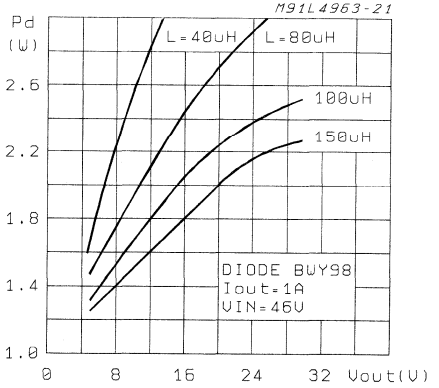


Figure 18: Voltage and Current Waveform at pin2

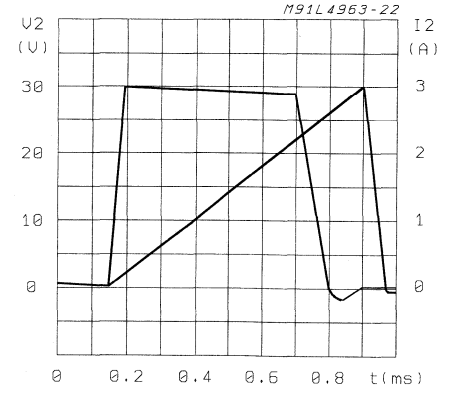


Figure 19: Efficiency vs. Output Current (Powerdip Package Only)

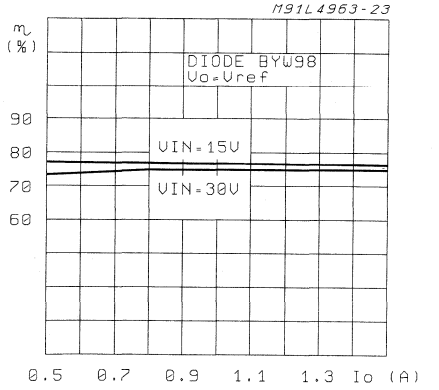


Figure 20: Efficiency vs. Output Voltage (Power-dip Package Only)

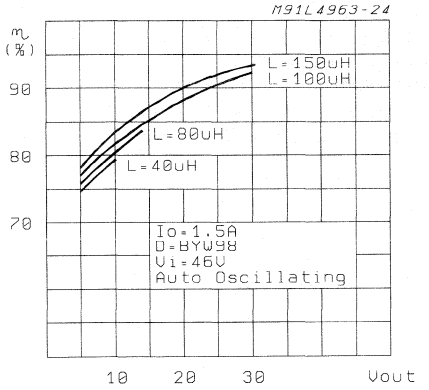


Figure 21: Current Limit vs. Junction Temperature V_i = 30V

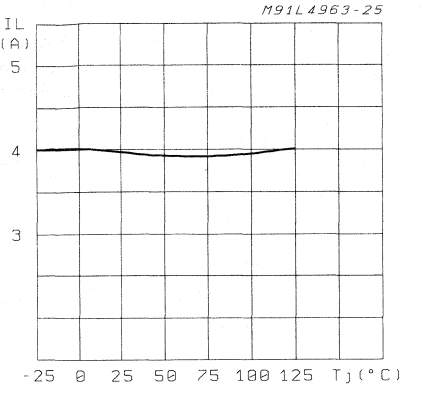


Figure 22: Current Limit vs. Input Voltage

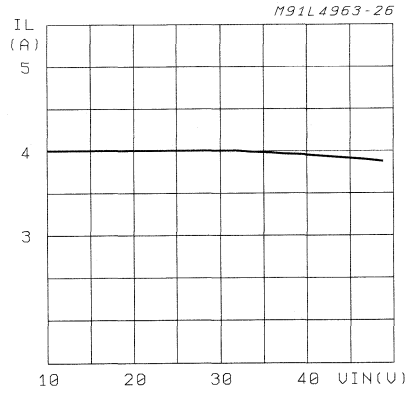


Figure 23: Oscillator Frequency vs. R2 (see fig. 26)

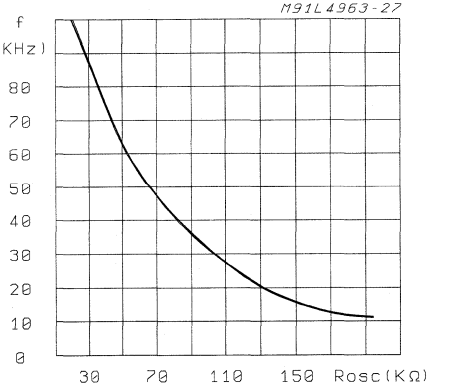


Figure 24: Oscillator Frequency vs. Junction Temperature

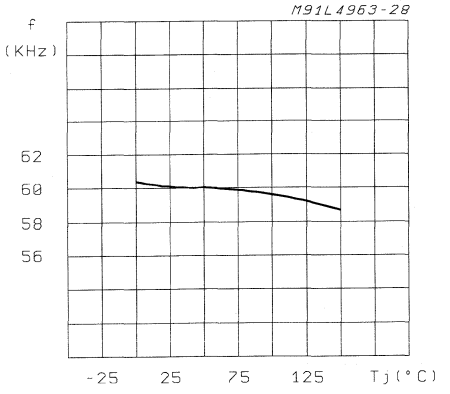


Figure 25: Oscillator Frequency vs. Input Voltage

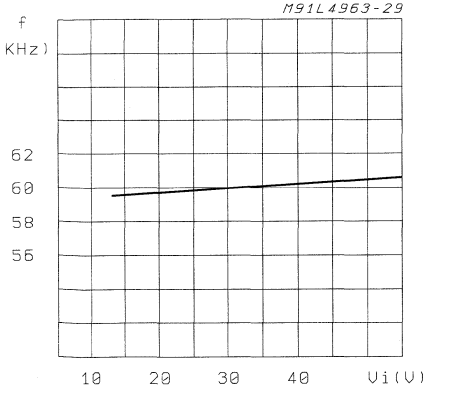
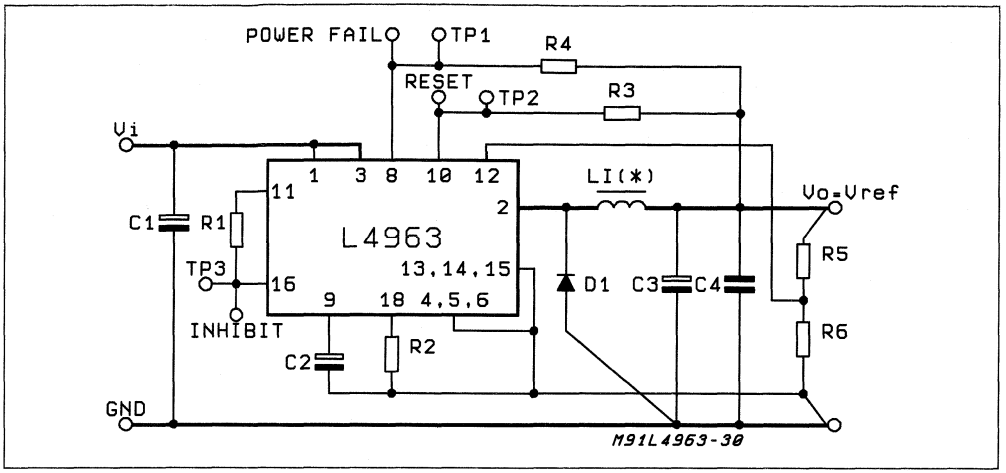


Figure 26: Evaluation Board Circuit



PART LIST

CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2mF 16V
C3	1000µF 40V with low ESR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
V_O	R6	R5
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP 34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 27: P.C. Board and Component Layout of the Circuit of fig. 26 (Powerdip Package) (1:1 scale).

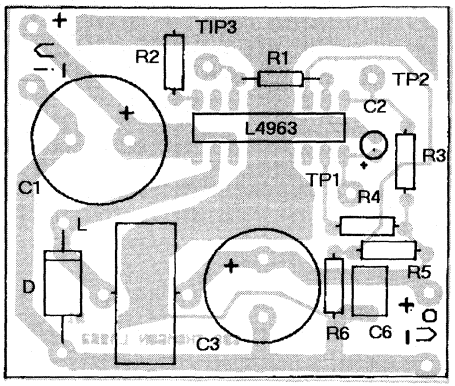


Figure 28: Thermal Characteristics

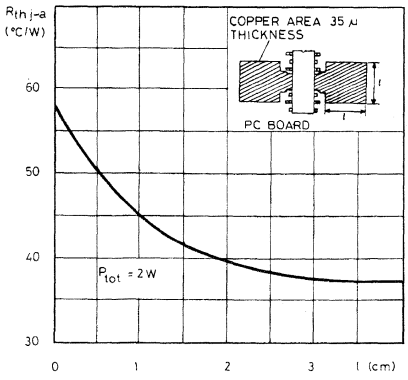


Figure 29: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

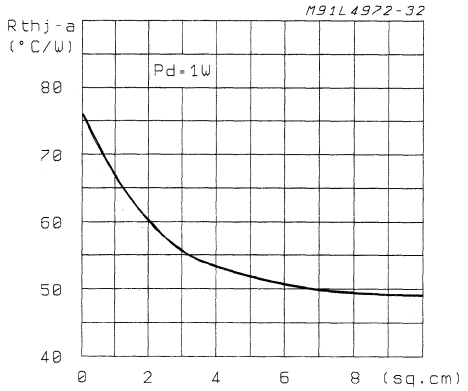


Figure 30: A Minimal 5.1 Fixed Regulator — Very Few Components are Required

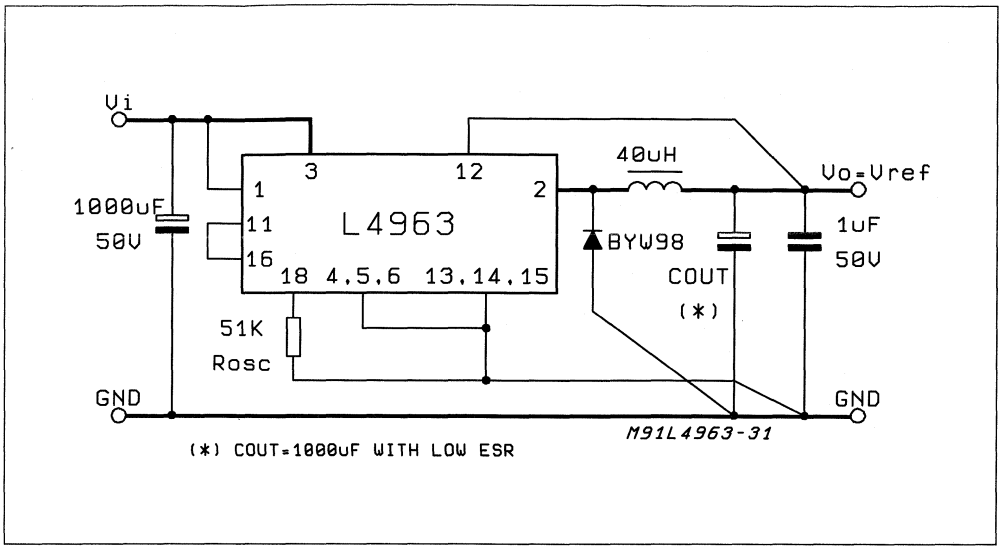
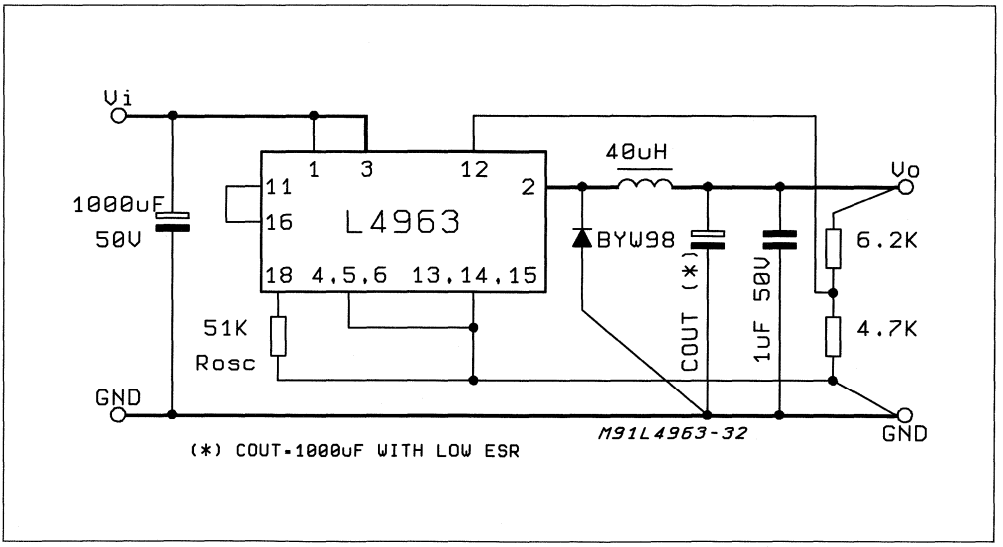


Figure 31: A Minimal Components count for V_O = 12V



HIGH CURRENT SWITCHING REGULATOR

- 4 A OUTPUT CURRENT
- 5.1 V TO 28 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (± 3 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 120 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- CURRENT LIMITING
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

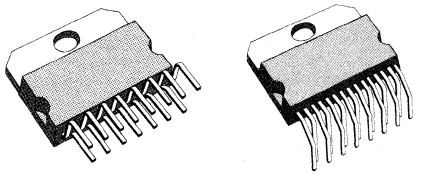
The L4964 is a stepdown power switching regulator delivering 4 A at a voltage variable from 5.1 V to 28 V.

Features of the device include overload protection, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L4964 is mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

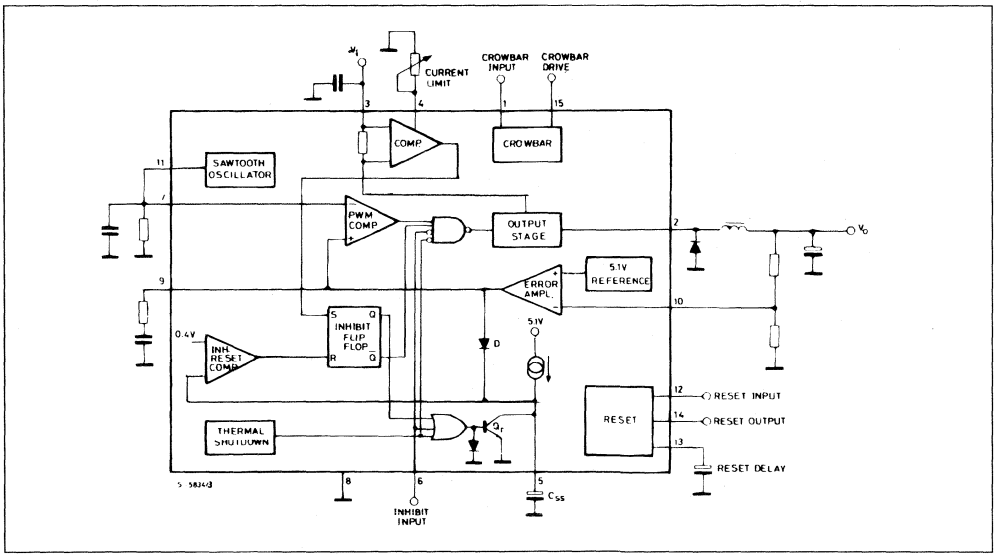
Efficient operation at switching frequencies up to 120 KHz allows a reduction in the size and cost of external filter components.

Multiwatt®
(15-lead)



ORDER CODES : L4964
L4964HT

BLOCK DIAGRAM



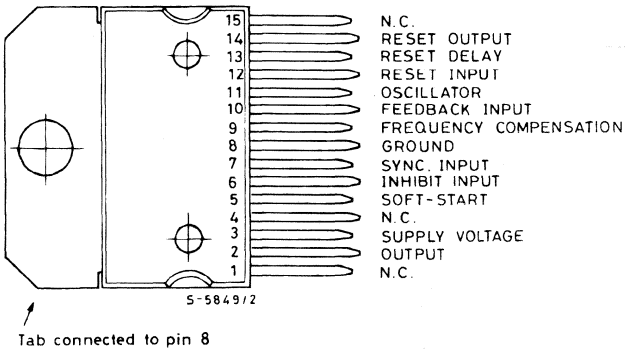
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage (pin 3)	36	V
$V_i - V_2$	Input to Output Voltage Difference	38	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 μsec f = 100 kHz	−1 −7	V V
V_{12}	Voltage at Pin 12	10	V
V_5, V_7, V_9	Voltage at Pins 5, 7 and 9	5.5	V
V_{10}, V_6, V_{13}	Voltage at Pins 10, 6 and 13	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	− 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

CONNECTION DIAGRAM (top view)



Note : Pins 1, 4, 15 must not be connected. Leave open circuit.

PIN FUNCTIONS

N°	Name	Function
1	N.C.	Must not be connected. Leave open circuit.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unregulated Voltage Input. An internal regulator powers the L4964's internal logic.
4	N.C.	Must not be connected. Leave open circuit.
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL - Level Remote Inhibit. A logic high level on this input disables the L4964.
7	SYNC INPUT	Multiple L4964's are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. The pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the beedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open Collector Reset Signal Output. This output is high when the supply is safe.
15	N.C.	Must not be connected. Leave open circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L4964 is a monolithic stepdown switching regulator providing output voltages from 5.1 V to 28 V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 3 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be ajusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{SS} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enable and the output voltage rises under contro of the soft start network. If the overload condition is still present the limiter will trigger again when the thershold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

A TTL - level input is provided for applications such as remote on/off control. This input is activated by high level and disables circuit operation. After an inhibit the L4964 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.

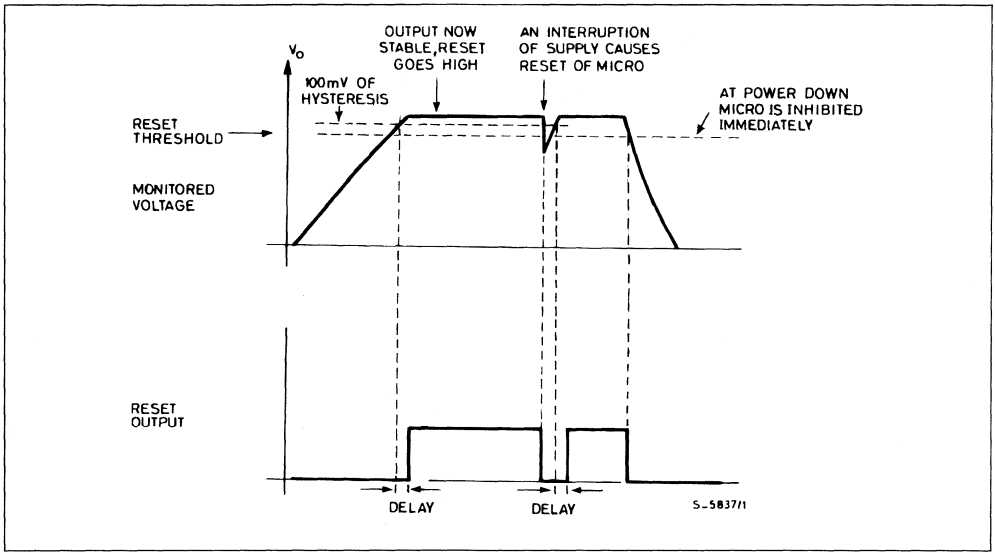


Figure 2 : Soft Start Waveforms.

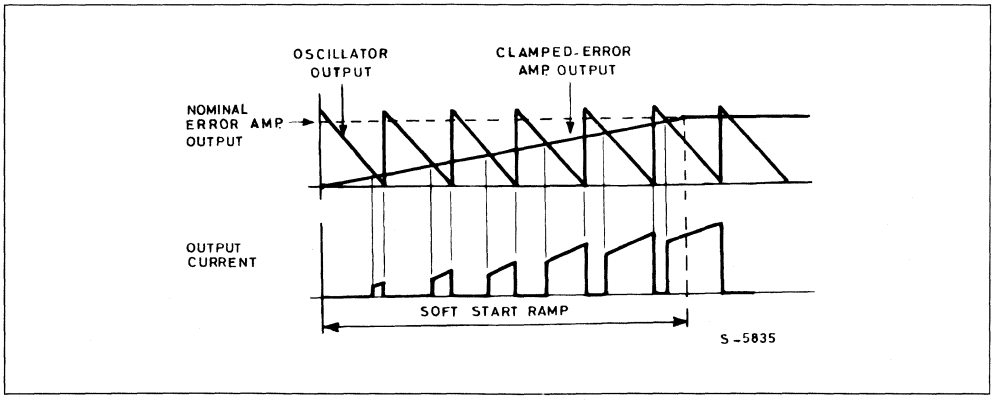
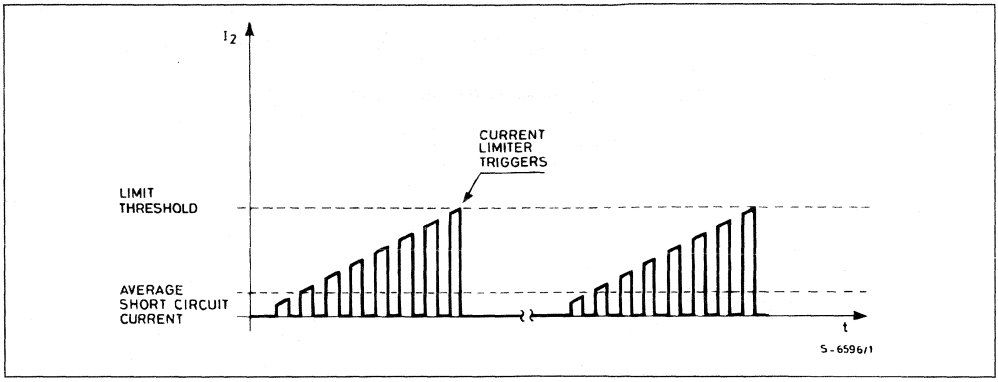


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 25 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V_o	Output Voltage Range	V_i = 36 V I_o = 1 A	V_{ref}		28	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 28 V I_o = 3 A	9		36	V	4
ΔV_o	Line Regulation	V_i = 10 V to 30 V, $V_o = V_{ref}$, I_o = 2 A		15	70	mV	4
ΔV_o	Load Regulation	I_o = 1 A to 2 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 3 A		15	50	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 36 V I_o = 2 A	4.95	5.1	5.25	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage between Pin 2 and Pin 3	I_o = 3 A		2	3.2	V	4
		I_o = 2 A		1.5	2.4	V	4
Io_m	Maximum Operating Load Current	V_I = 9 V to 36 V, $V_o = V_{ref}$ to 28 V	4			A	4
I_{2L}	Current Limiting Threshold (pin 2)	V_i = 9 V to 36 V $V_o = V_{ref}$ to 28 V	4.5		8	A	4
I_{SH}	Input Average Current	V_i = 36 V ; Output Short-circuited		80	140	mA	4

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (continued)

η	Effiency	I_o = 3 A	$V_o = V_{ref}$		75		%	4
			V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms} $V_o = V_{ref}$	f_{ripple} = 100 Hz I_o = 2 A	46	56	–	dB	4
f	Switching Frequency			40	50	60	kHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 36 V			0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C			1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$ I_o = 1 A		120			kHz	–
T_{sd}	Thermal Shutdown Junction Temperature			135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	V_i = 36 V V_7 = 0 V S1 : B S2 : B	V_6 = 0		66	100	mA	6a
			V_6 = 3 V		30	50	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 36 V, V6 = 3 V, S1 : B, S2 : A, V_7 = 0 V				2	mA	6a

SOFT START

I_{5so}	Source Current	V_6 = 0 V,	V_5 = 3 V	80	130	180	µA	6b
I_{5si}	Sink Current	V_6 = 3 V,	V_5 = 3 V	40	70	140	µA	6b

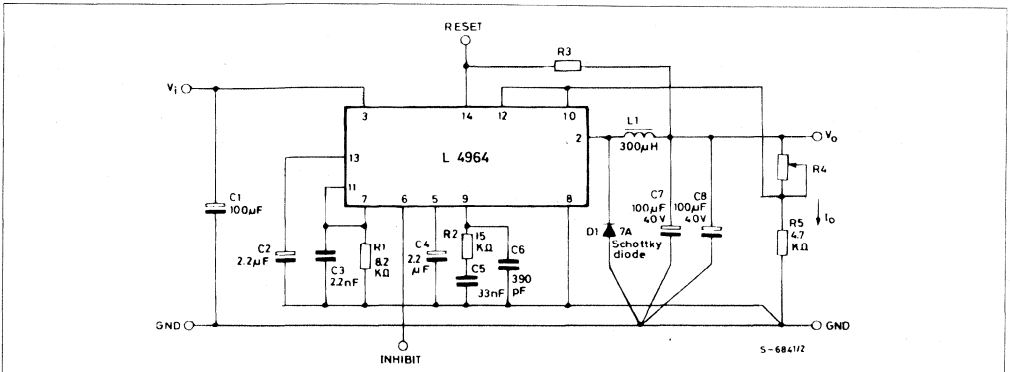
INHIBIT

V_{6L}	Low Input Voltage	V_i = 9 V to 36 V	S1 : B S2 : B	– 0.3		0.8	V	6a
V_{6H}	High Input Voltage	V_7 = 0 V		2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	V_i = 9 V to 36 V V_7 = 0 V	V_6 = 0.8 V			20	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	S1 : B S2 : B	V_6 = 2 V			10	µA	6a

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
ERROR AMPLIFIER							
V_{9H}	High Level Output Voltage	V_{10} = 4.7 V, I_9 = 100 µA, S1 : A, S2 : A	3.4			V	6c
V_{9L}	Low Level Output Voltage	V_{10} = 5.3 V, I_9 = 100 µA, S1 : A, S2 : E			0.6	V	6c
$I_{9\,si}$	Sink Output Current	V_{10} = 5.3 V, S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	V_{10} = 4.7 V, S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	V_{10} = 5.2 V S1 : B		2	20	µA	6c
G_v	DC Open Loop Gain	V_9 = 1 V to 3 V, S1 : A, S2 : C	40	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
$-I_7$	Input Bias Current of PWM Comparator	V_7 = 0.5 V to 3.5 V			10	µA	6a
$-I_{11}$	Oscillator Source Current	V_{11} = 2 V, S1 : A, S2 : B	4		–	mA	6a
RESET							
V_{12R}	Rising Threshold Voltage	V_i = 9 V to 36 V, S1 : B, S2 : B,	V_{ref} −150mV	V_{ref} −100mV	V_{ref} −50mV	V	6d
V_{12F}	Falling Threshold Voltage		4.75	V_{ref} −150mV	V_{ref} −100mV	V	6d
V_{13D}	Delay Threshold Voltage	V_{12} = 5.3 V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
V_{13H}	Delay Threshold Voltage Hysteresis			100		mV	6d
V_{14S}	Output Saturation Volt.	I_{14} = 5 mA ; V_{12} = 4.7 V ; S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	V_{12} = 0 V to V_{ref}, S1 : B, S2 : B		1	10	µA	6d
$-I_{13\,so}$	Delay Source Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 5.3 V	60	110	150	µA	6d
$I_{13\,si}$	Delay Sink Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 4.7 V	8			mA	6d
I_{14}	Output Leakage Current	V_i = 36 V, V_{12} = 5.3 V, S1 : B, S2 : A			100	µA	6d

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A
R = 500 mΩ

Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG)

Figure 5 : PC. Board and Component Layout of the Circuit of Fig. 4 (1:1 scale).

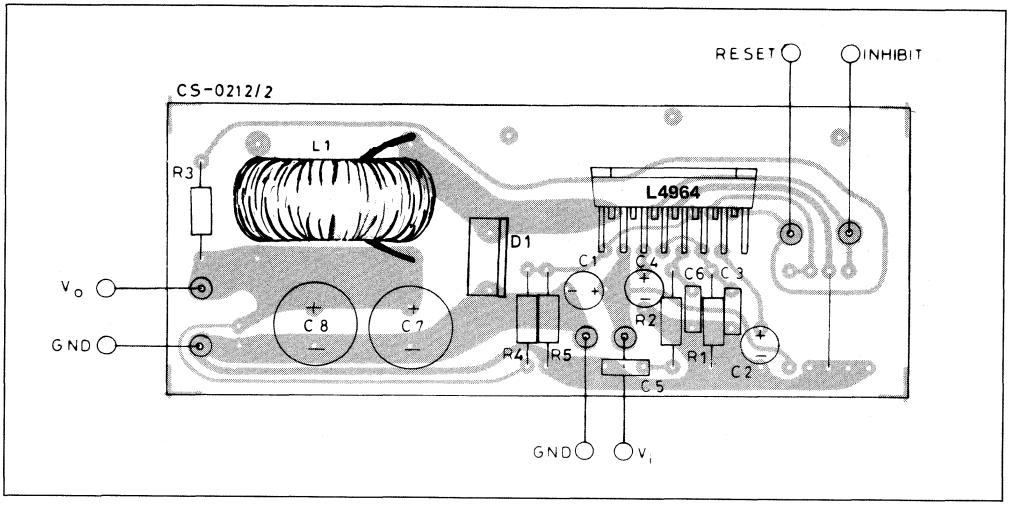


Figure 6 : DC Test Circuits.

Figure 6a.

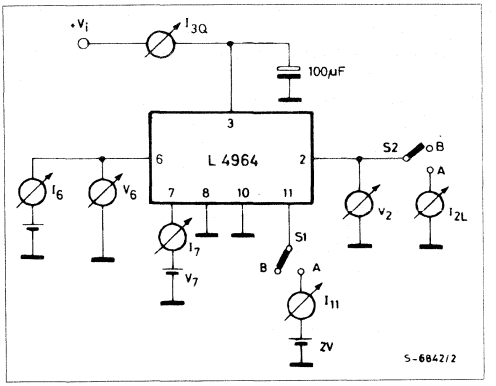


Figure 6b.

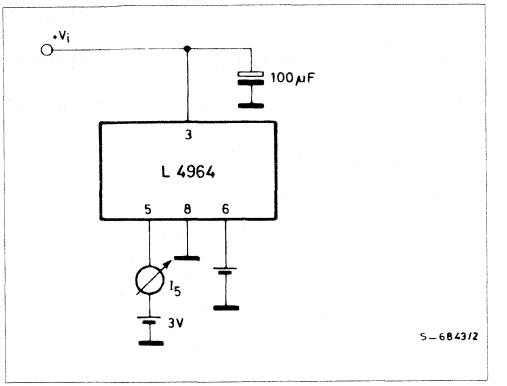


Figure 6c.

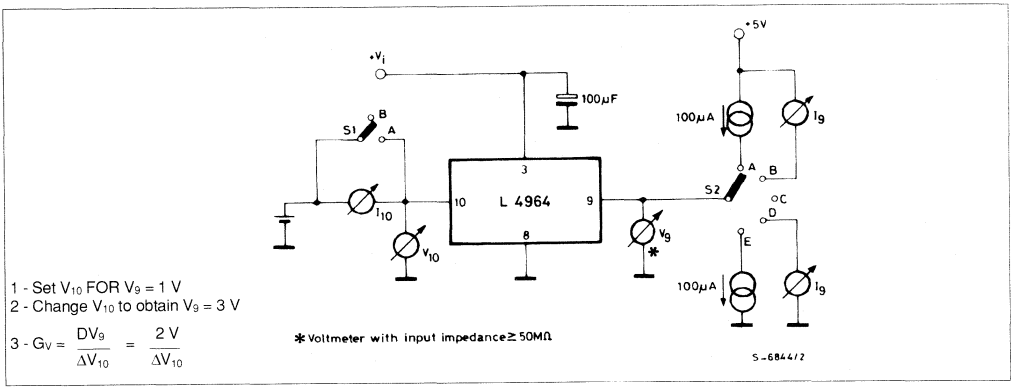


Figure 6d.

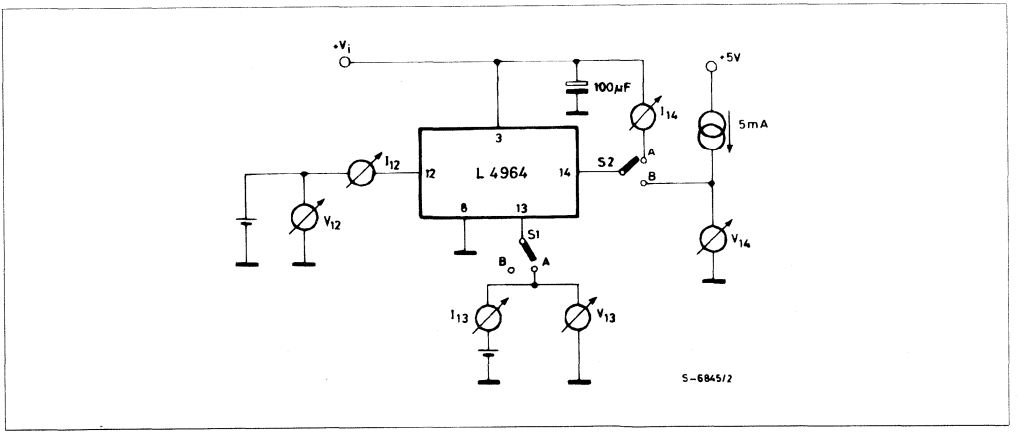


Figure 7 : Switching Frequency vs. R1 (see fig. 4).

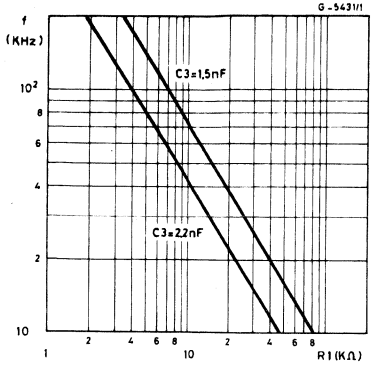


Figure 8 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

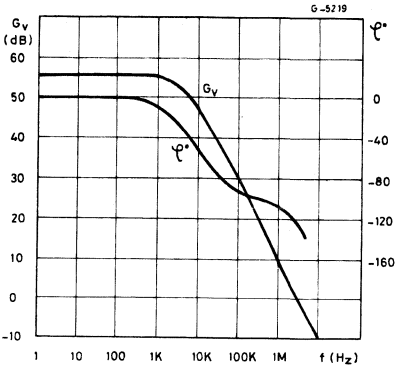


Figure 9 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

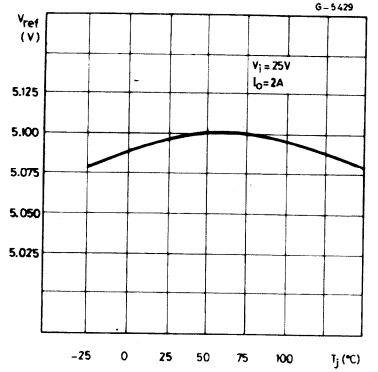


Figure 10 : Power Dissipation (L4964 only) vs. Input Voltage.

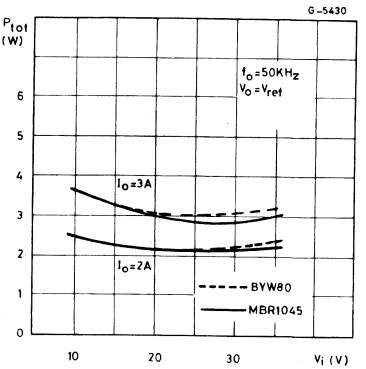


Figure 11 : Efficiency vs. Output Voltage.

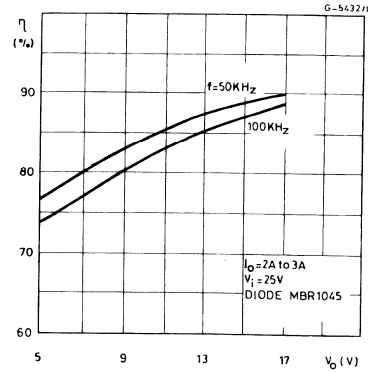
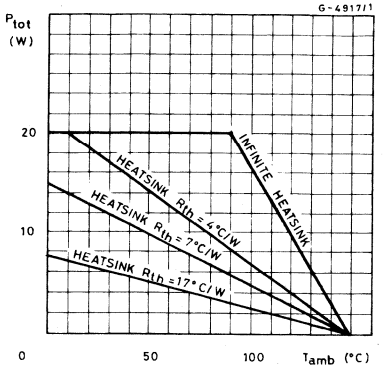


Figure 12 : Power Dissipation Derrating Curve.



SGS-THOMSON MICROELECTRONICS

APPLICATION INFORMATION

CHOOSING THE INDUCTOR AND CAPACITOR

The input and output capacitors of the L4964 must have a low ESR and low inductance at high current ripple.

Preferably, the inductor should be a toroidal type or wound on a Moly-Permalloy nucleus.Saturation must not occur at current levels below 1.5 times the current limiter level. MPP nuclei have very soft saturation characteristics.

$$L = \frac{(V_i - V_o)\, V_o}{V_i f \Delta I_L}$$

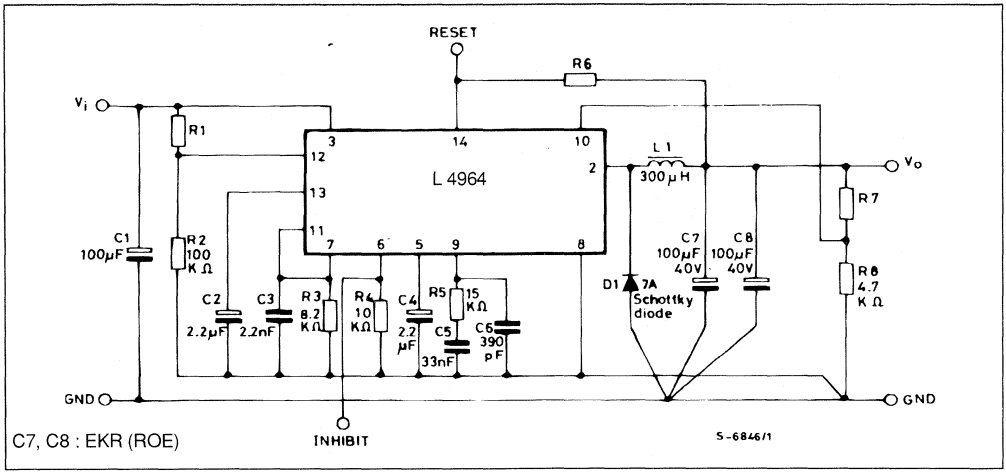
$$C = \frac{(V_i - V_o)\, V_o}{8L f^2 \Delta V_o}$$

F = frequency

ΔI_L = Inductance current ripple

ΔV_o = Output ripple voltage

Figure 13 : Typical Application Circuit.



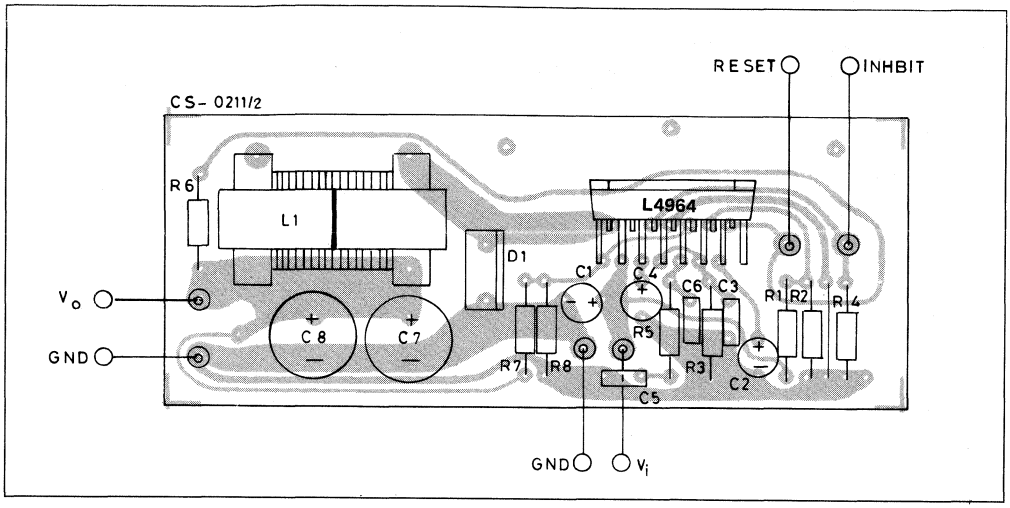
C7, C8 : EKR (ROE)

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	50	0.8 mm	0.7 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_o	R8	R7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ

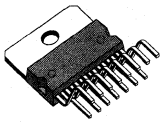
Figure 14 : P.C. Board and Component Layout of the Circuit of Fig. 13 (1:1 scale).



10A SWITCHING REGULATOR

- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



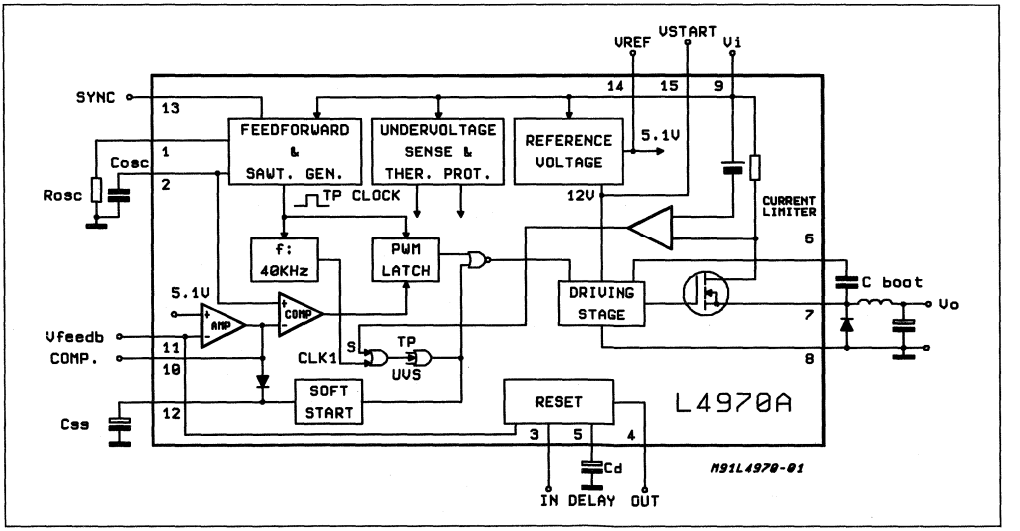
Multiwatt15V
ORDERING NUMBER: L4970A

DESCRIPTION

The L4970A is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

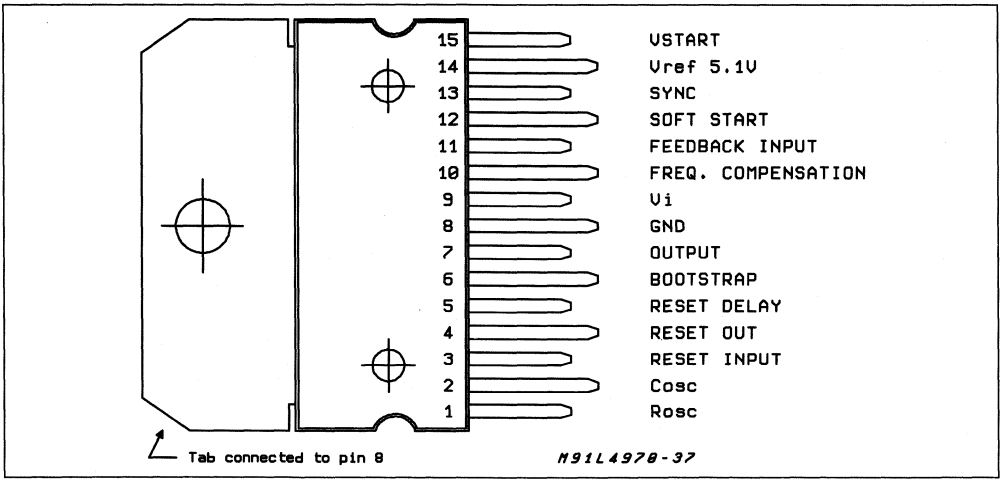
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4970A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4970A is a 10A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 10A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

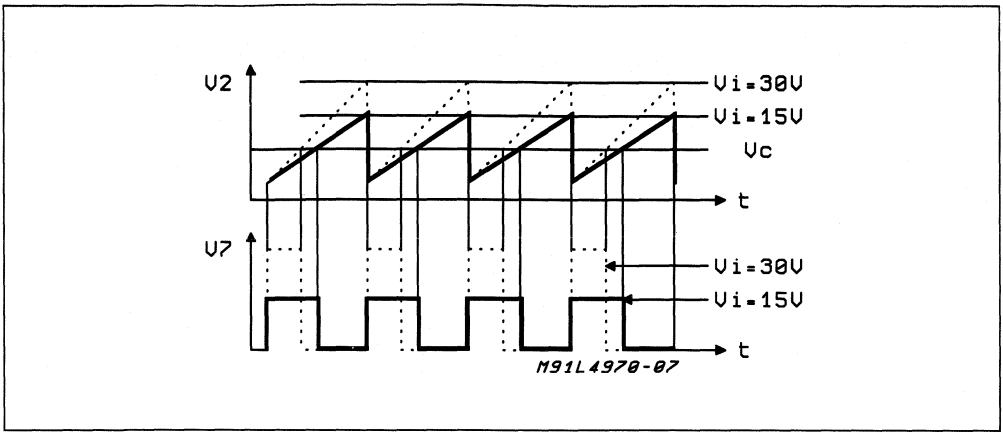


Figure 2: Soft Start Function

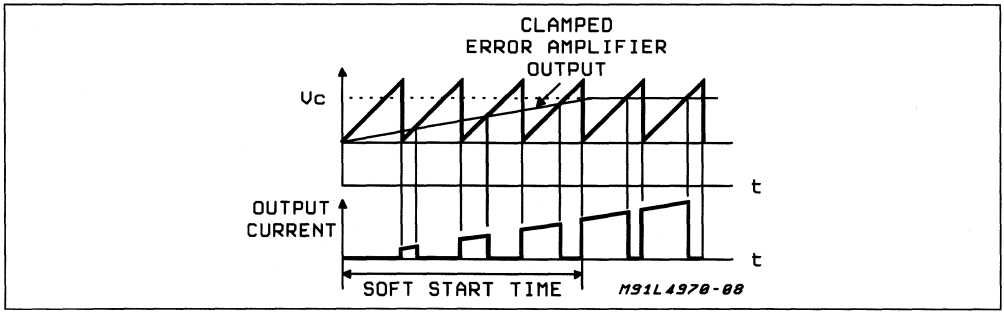
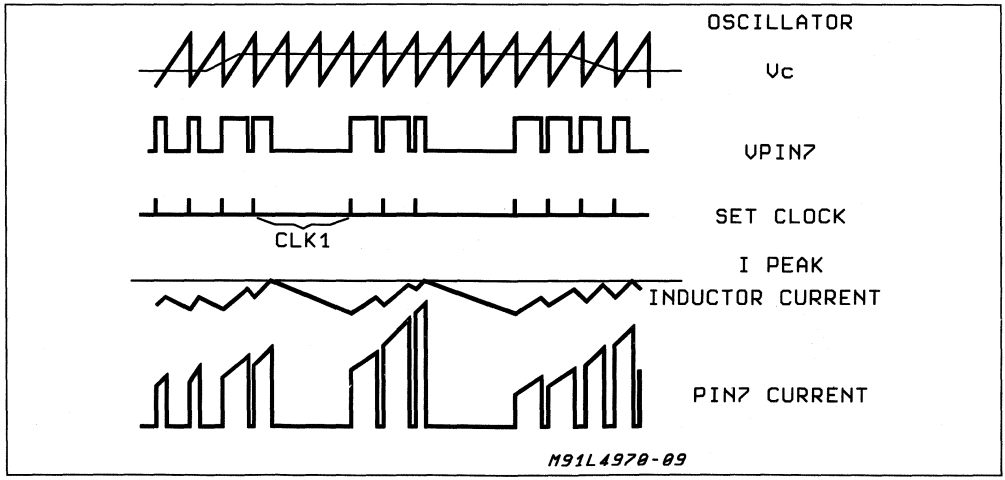


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

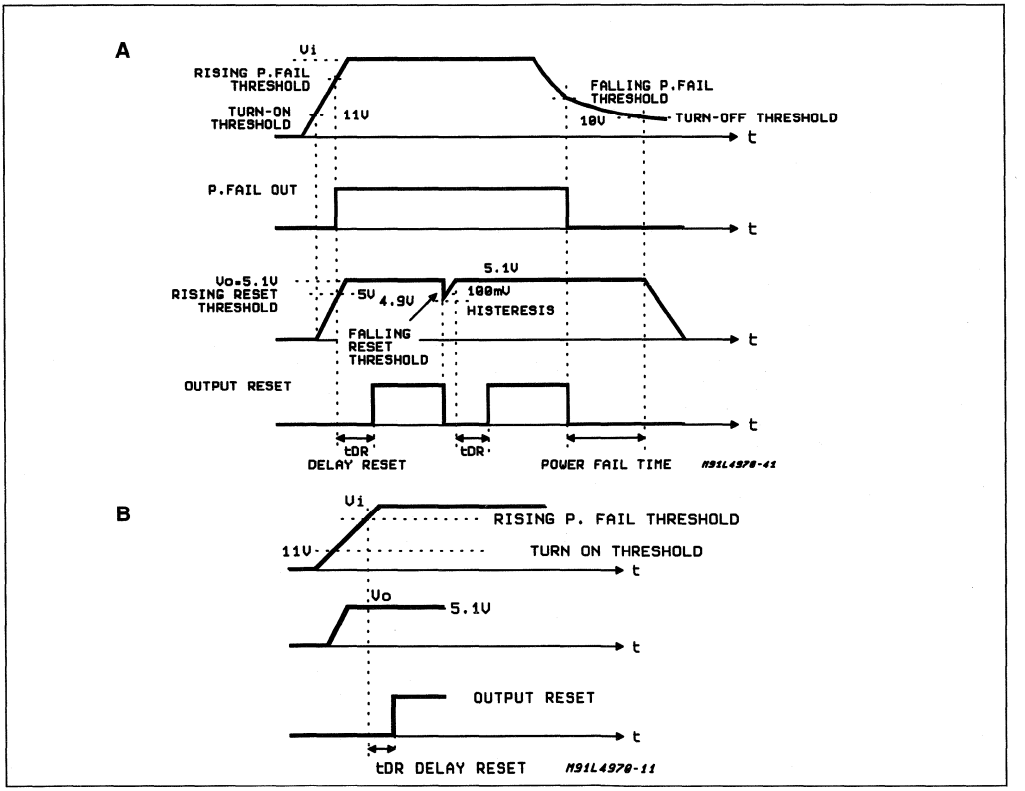
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	$V_o = V_{ref}$ to 40V I_o = 10A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 5A; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 5A; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 3A to 6A I_o = 2A to 10A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 10A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V	11	13	15	A	5
η	Efficiency	I_o = 5A $V_o = V_{ref}$ V_o = 12V	80	 85 92		 % %	5
		I_o = 10A $V_o = V_{ref}$ V_o = 12V	75	 80 87		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 5A f = 100Hz; $V_o = V_{ref}$	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; R_4 = 10KΩ I_o = 10A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C;	V_i = 15V		2.5		V	7A
		S2 = B;	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA		2.4	2.7		mA	7A

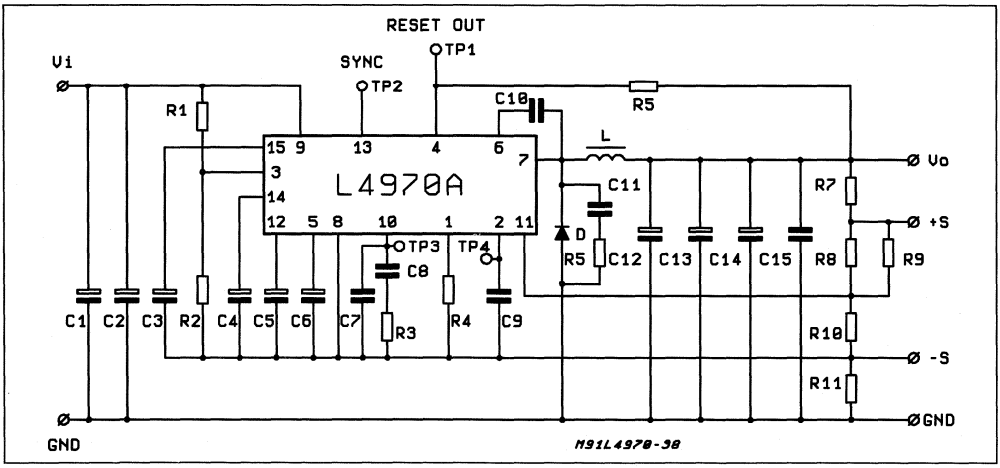
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_{13} = V_2 = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

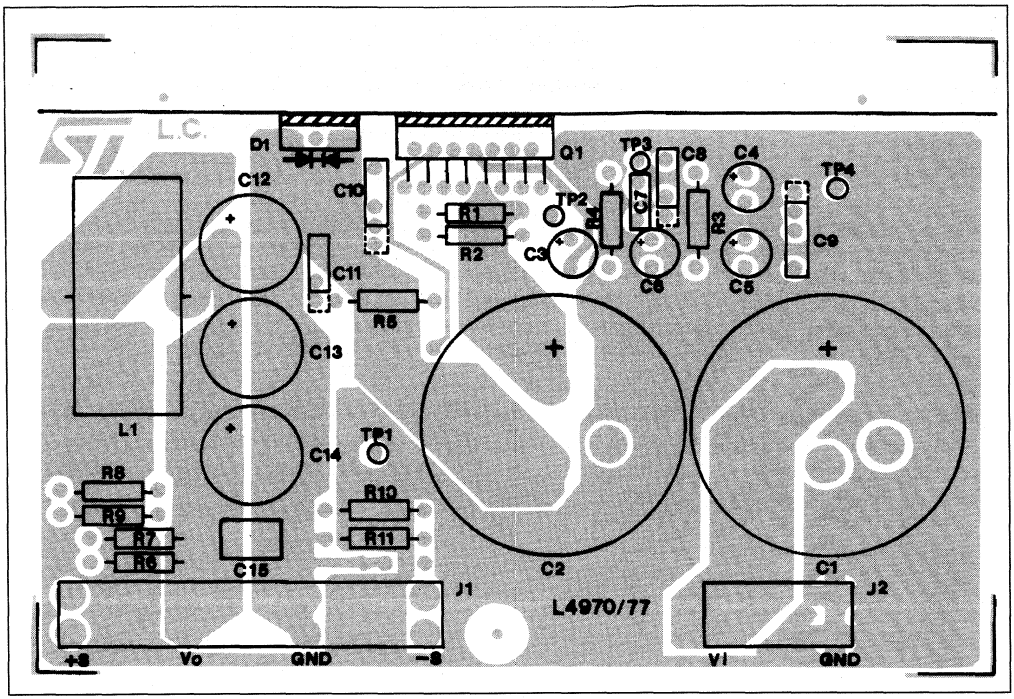
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 10A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

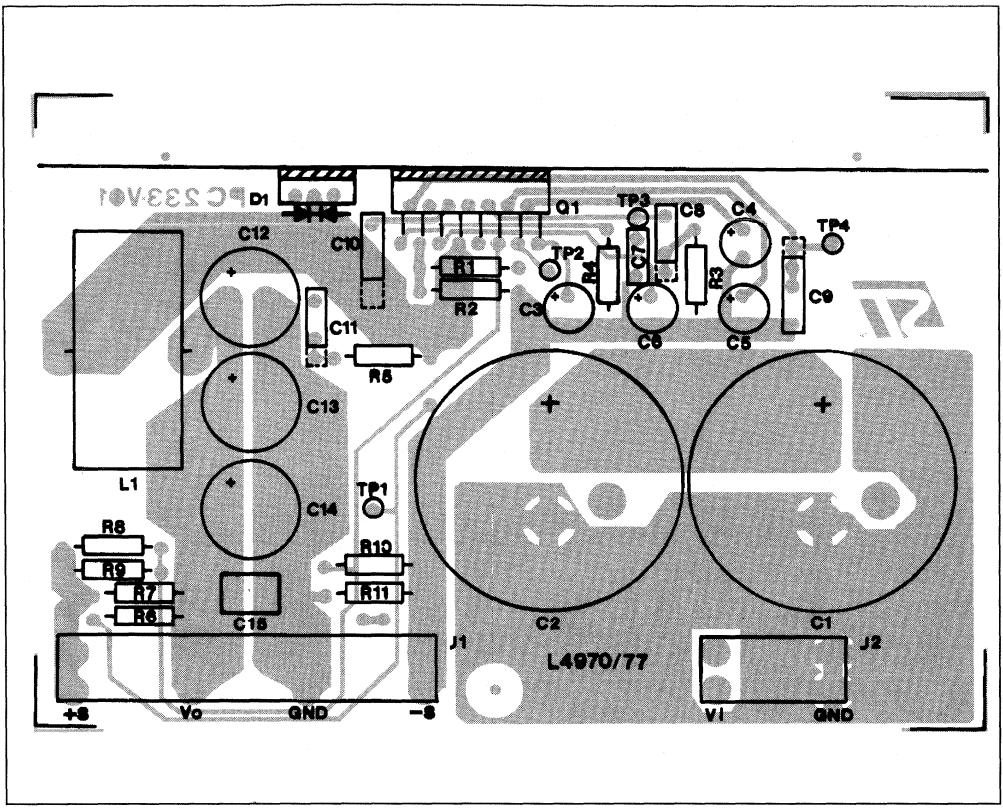


Figure 7: DC Test Circuits

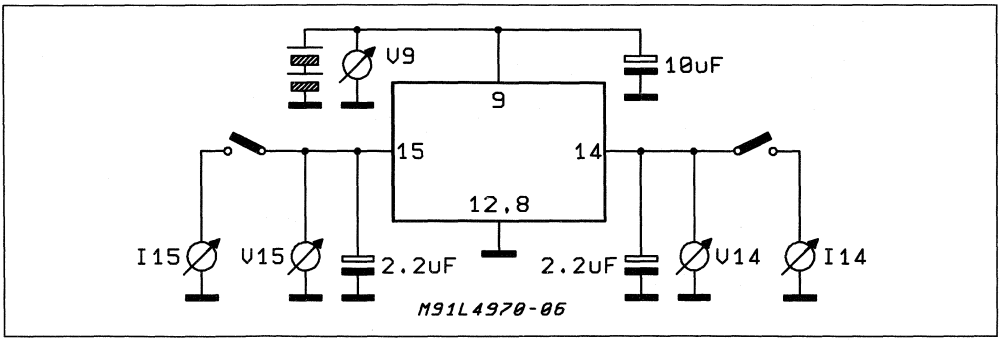


Figure 7A

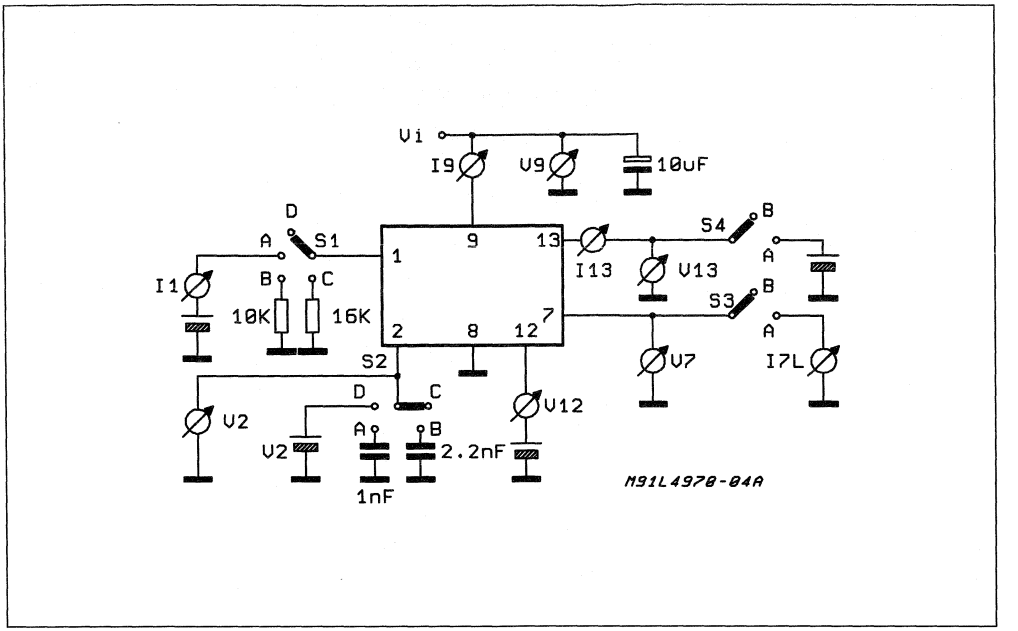


Figure 7B

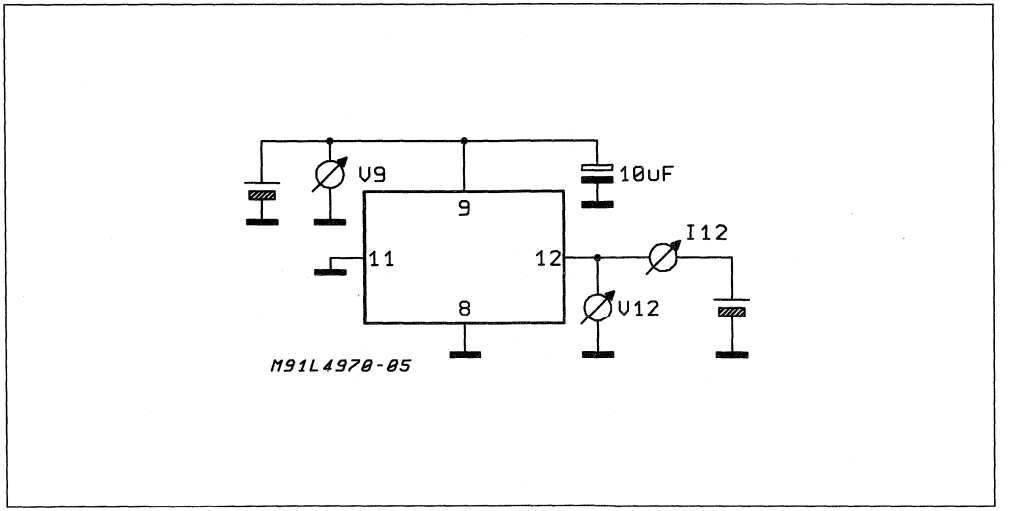


Figure 7D

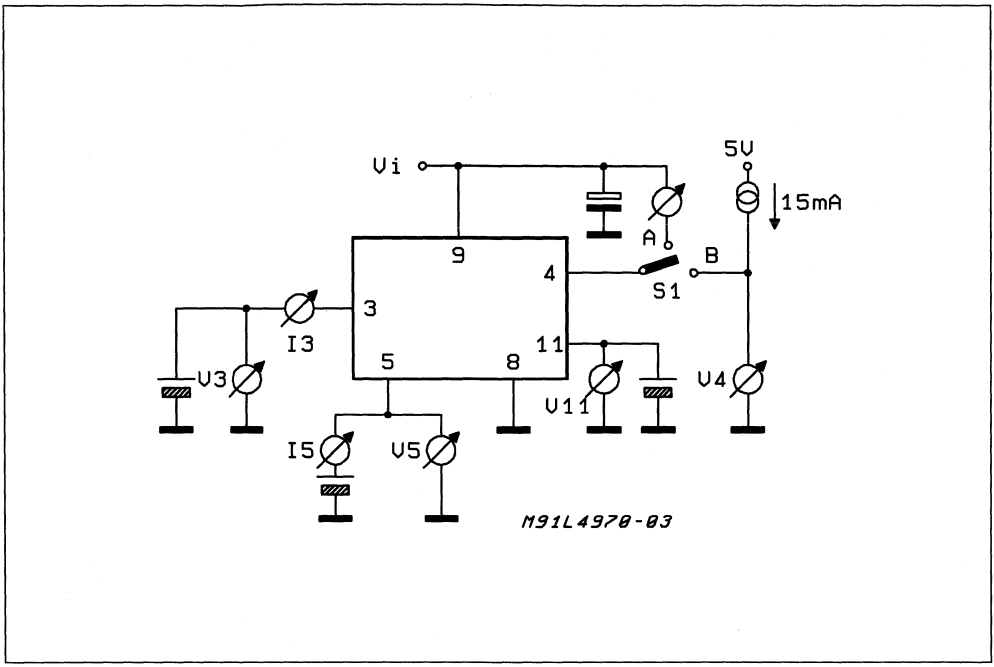


Figure 7C

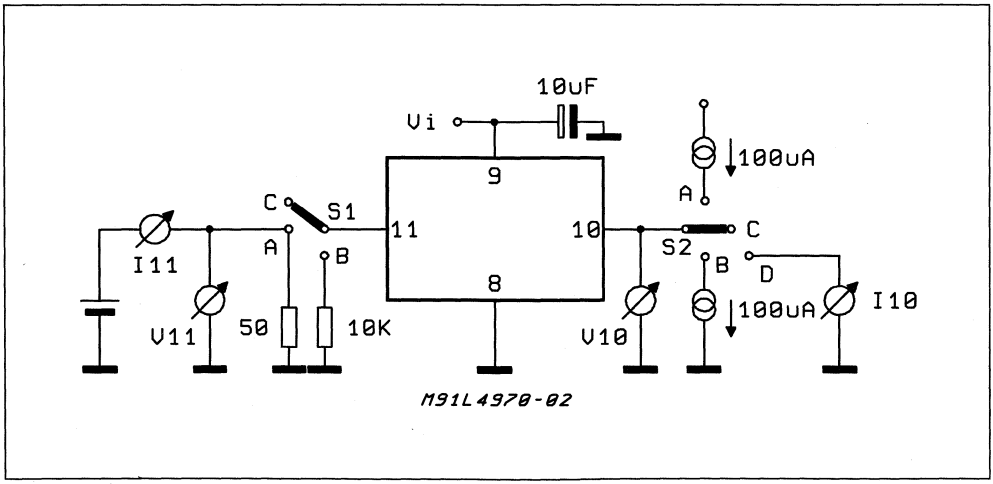


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

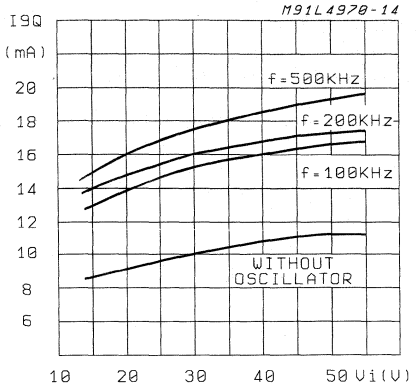


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

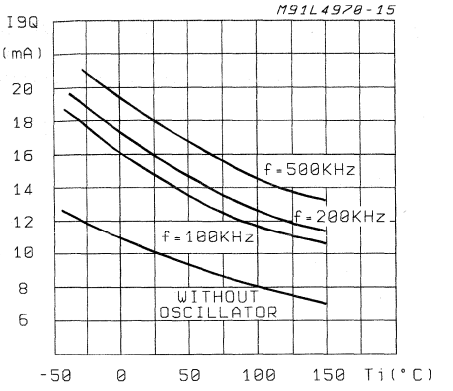


Figure 10: Quiescent Drain Current vs. Duty Cycle

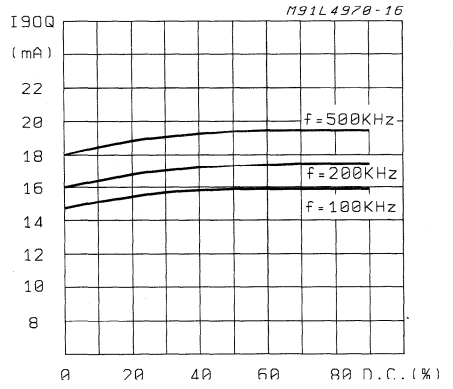


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

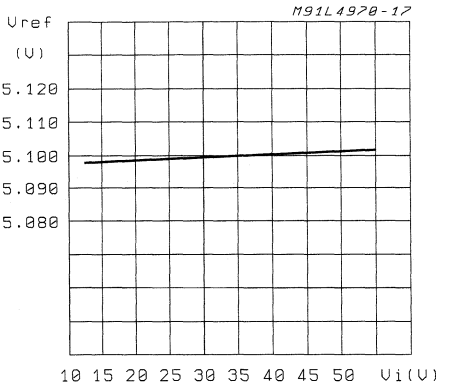


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

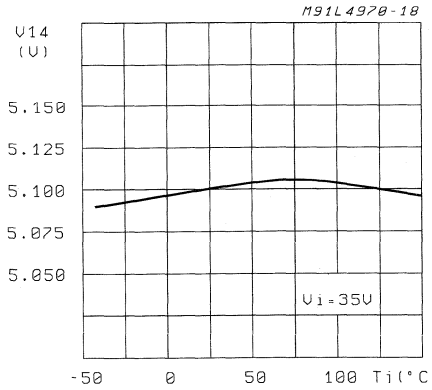


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

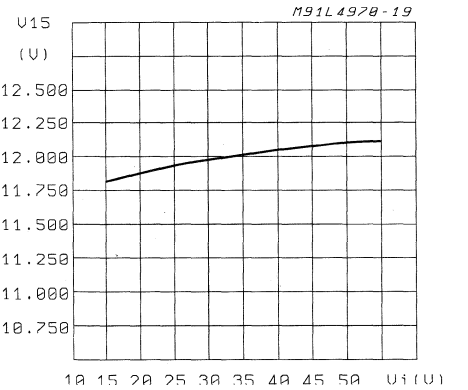


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

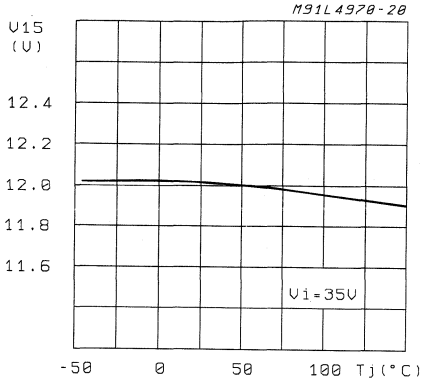


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

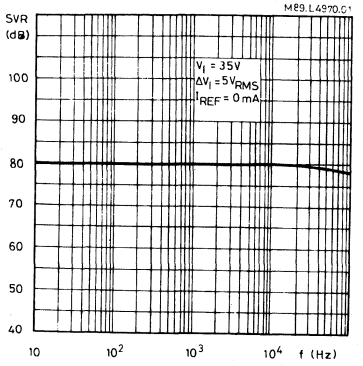


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

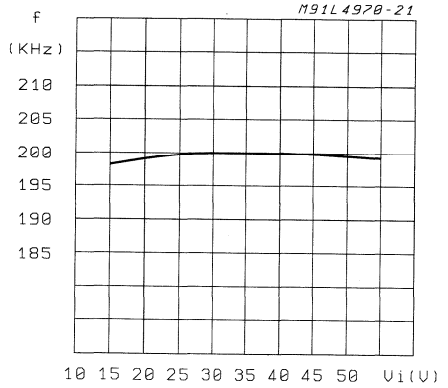


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

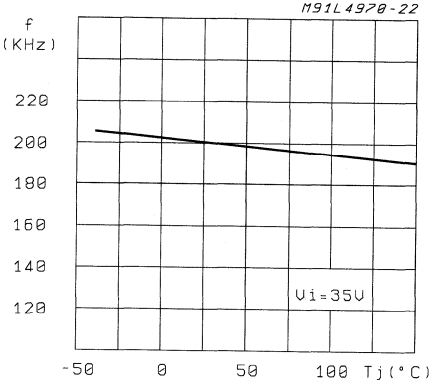


Figure 18: Switching Frequency vs. R4 (see fig. 5)

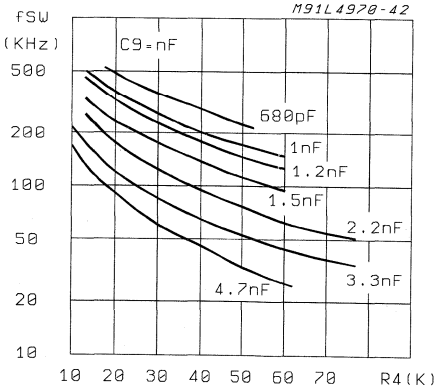


Figure 19: Max. Duty Cycle vs. Frequency

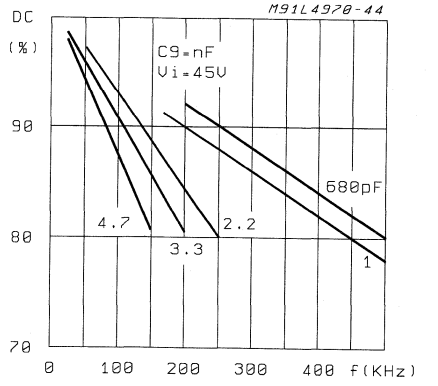


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

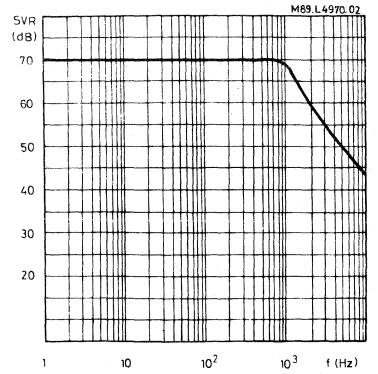


Figure 21: Line Transient Response (see fig. 5)

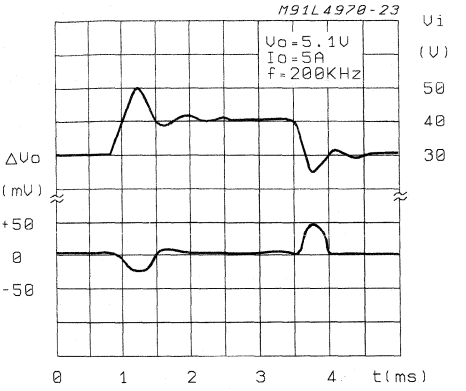


Figure 22: Load Transient Response (see fig. 5)

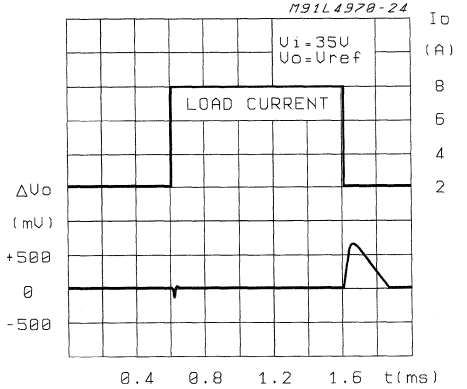


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

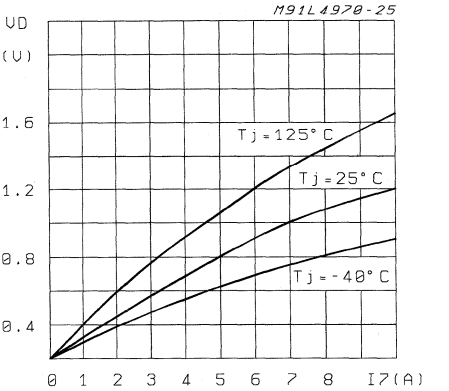


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

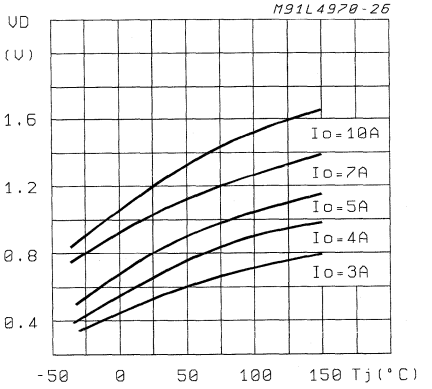


Figure 25: Power Dissipation (device only) vs. Input Voltage

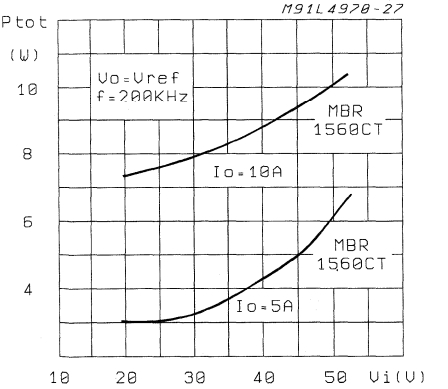


Figure 26: Power Dissipation (device only) vs. Output Voltage

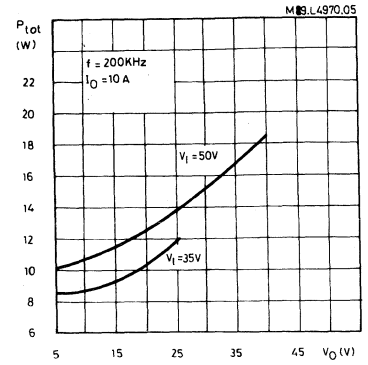


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

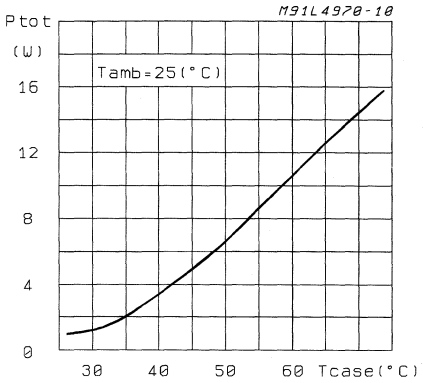


Figure 28: Efficiency vs. Output Current

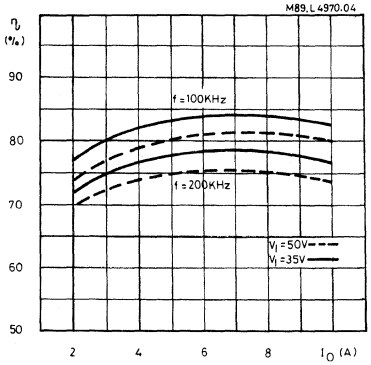


Figure 29: Efficiency vs. Output Voltage

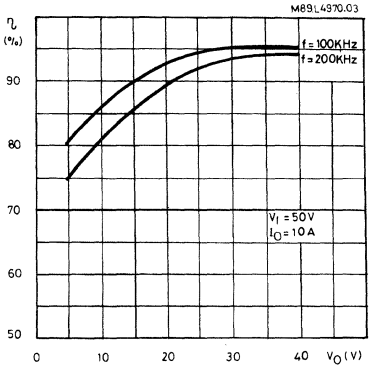


Figure 30: Efficiency vs. Output Voltage

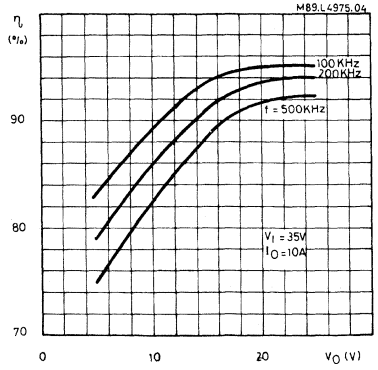


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

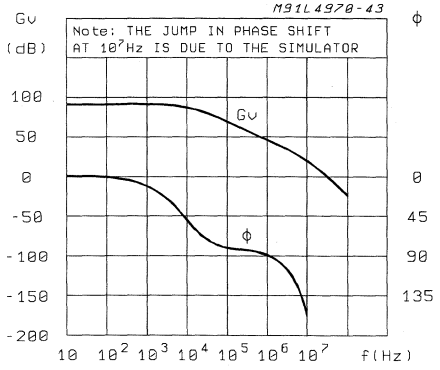


Figure 32: Power Dissipation Derating Curve

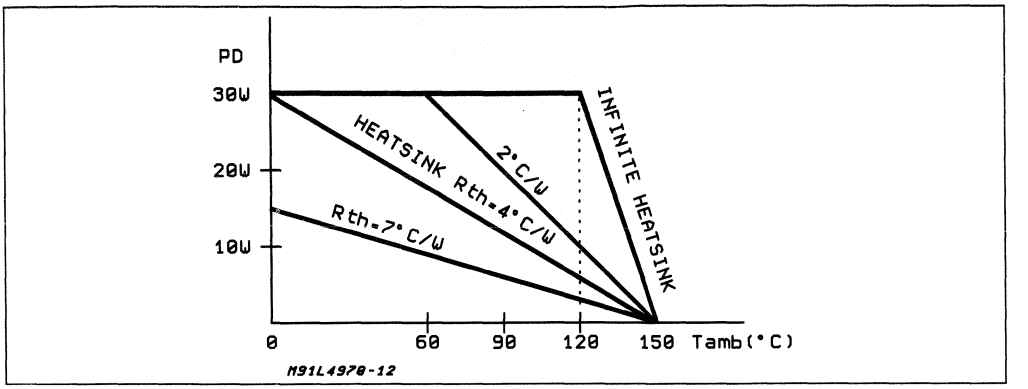


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4970A and the L4974A

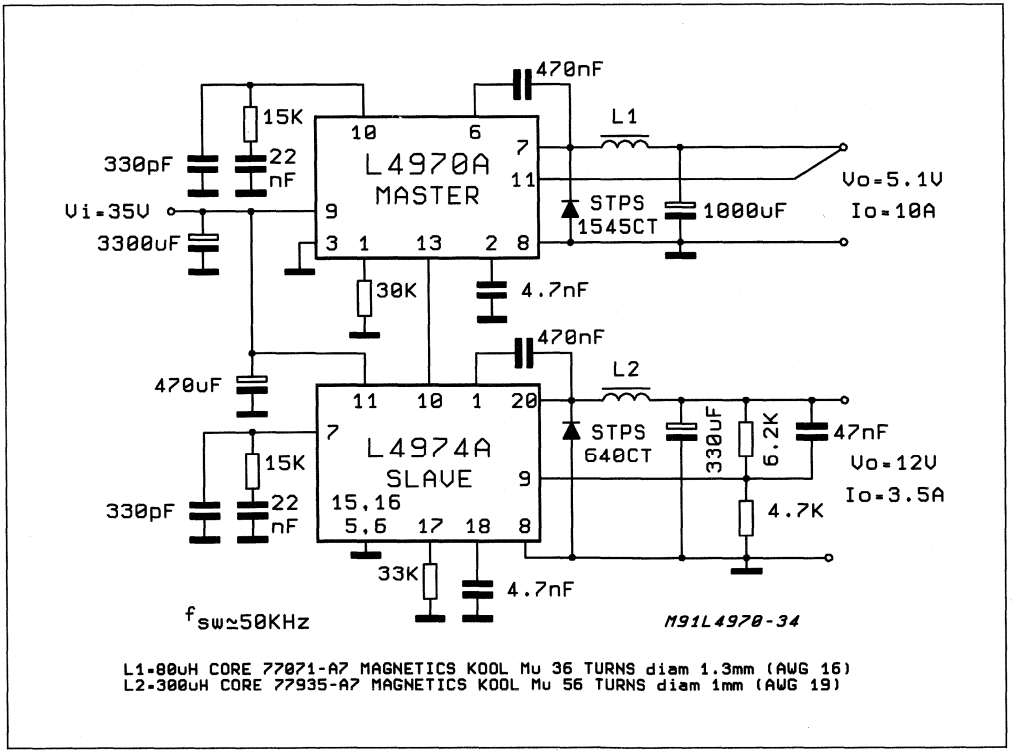


Figure 34: 5.1V / 10A Low Cost Application

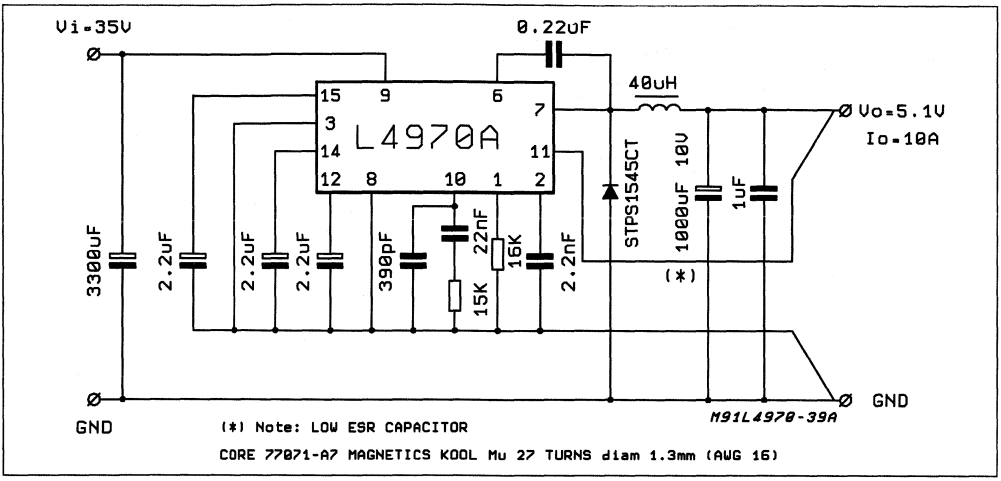


Figure 35: 10A Switching Regulator, Adjustable from 0V to 25V.

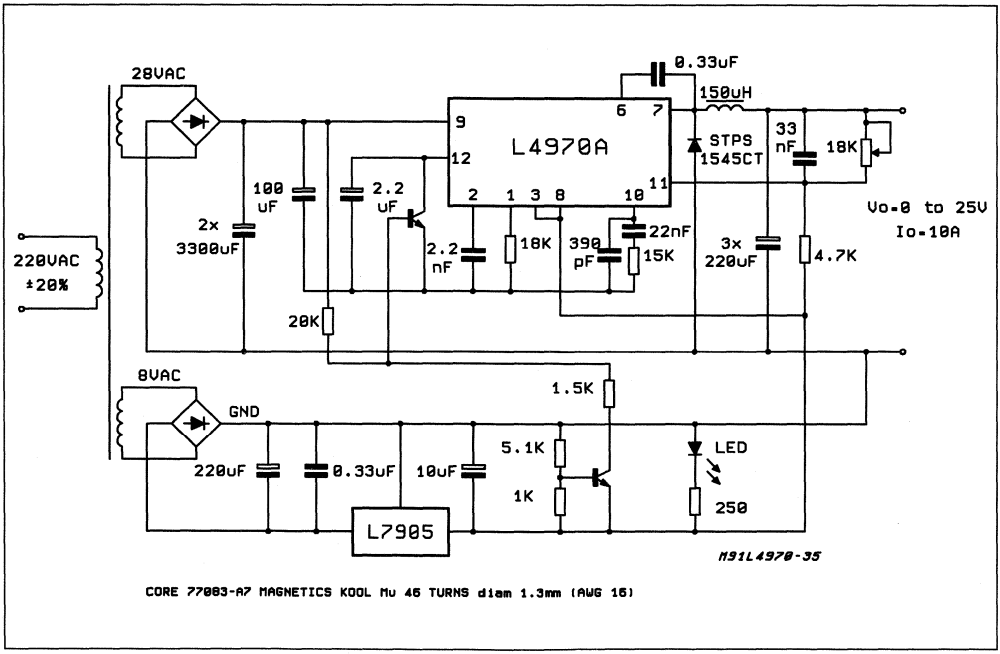
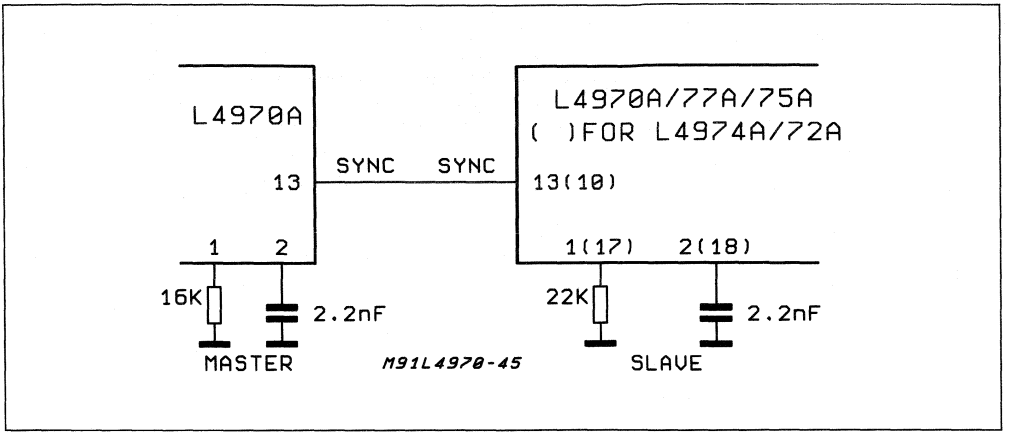


Figure 36: L4970A's Sync. Example



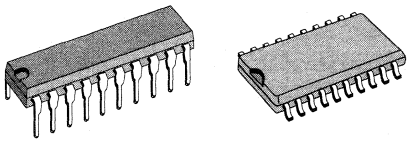
SGS-THOMSON MICROELECTRONICS

L4972A
L4972AD

2A SWITCHING REGULATOR

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

SO20

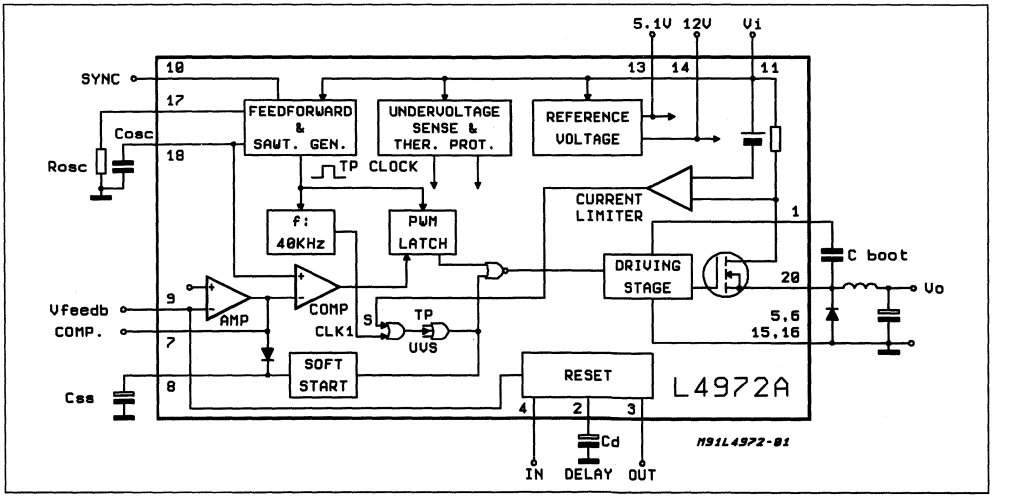
ORDERING NUMBERS : L4972A (Powerdip)
L4972AD (SO20)

DESCRIPTION

The L4972A is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

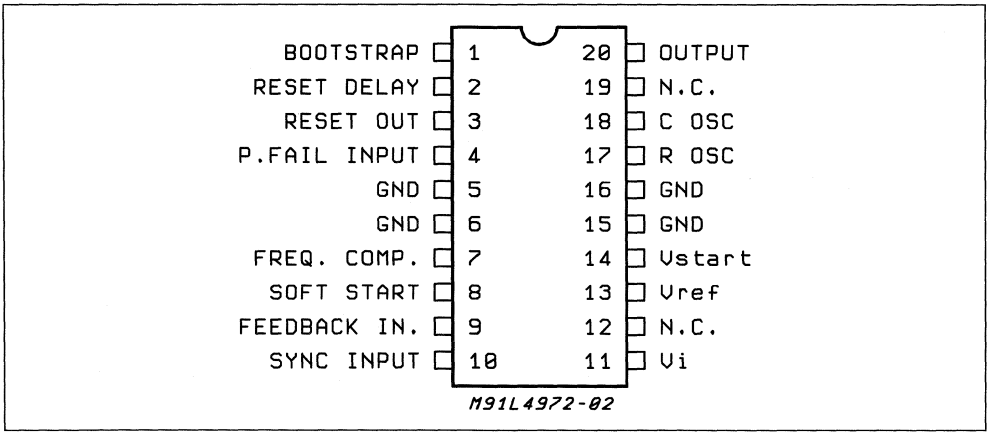


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 / 3.75(*) 1.3/1 (*)	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

(*) SO-20

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Powerdip	SO-20
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12°C/W	16°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60°C/W	80°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972A's are synchronized by connecting pin 10 inputs togheter or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4972A is a 2A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

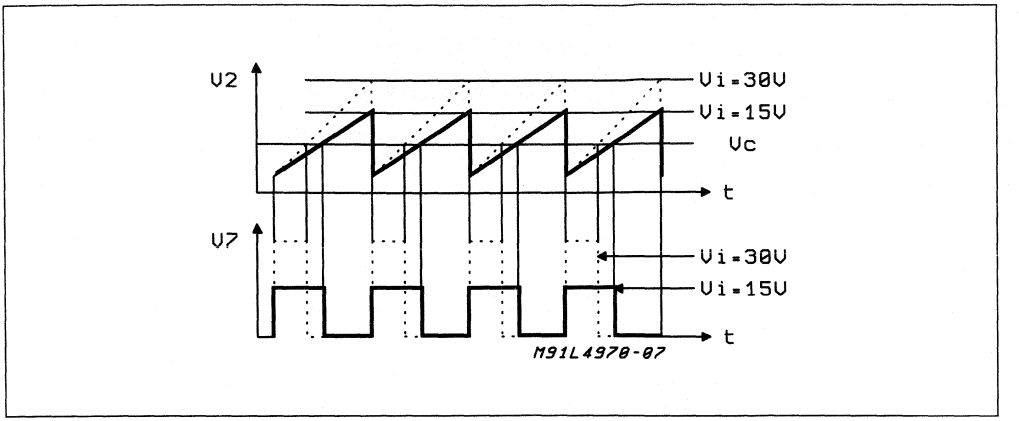


Figure 2 : Soft Start Function.

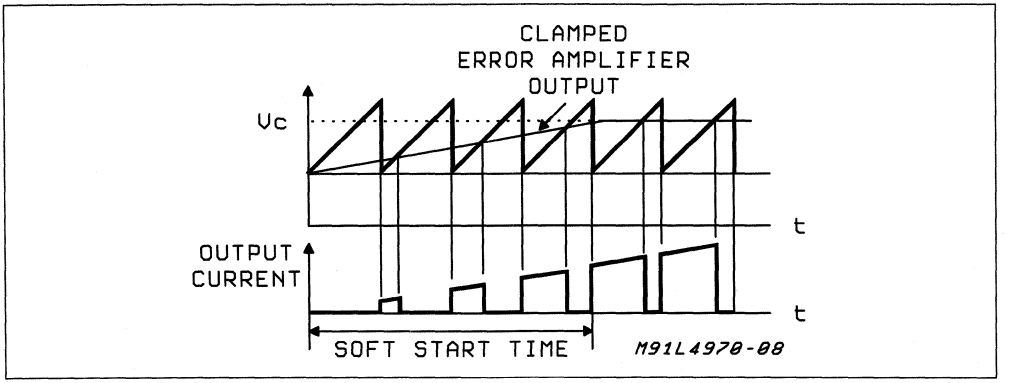


Figure 3 : Limiting Current Function.

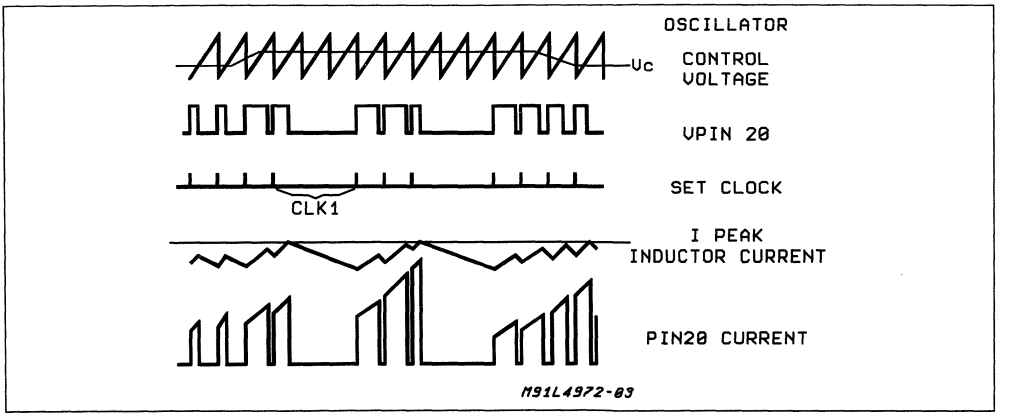
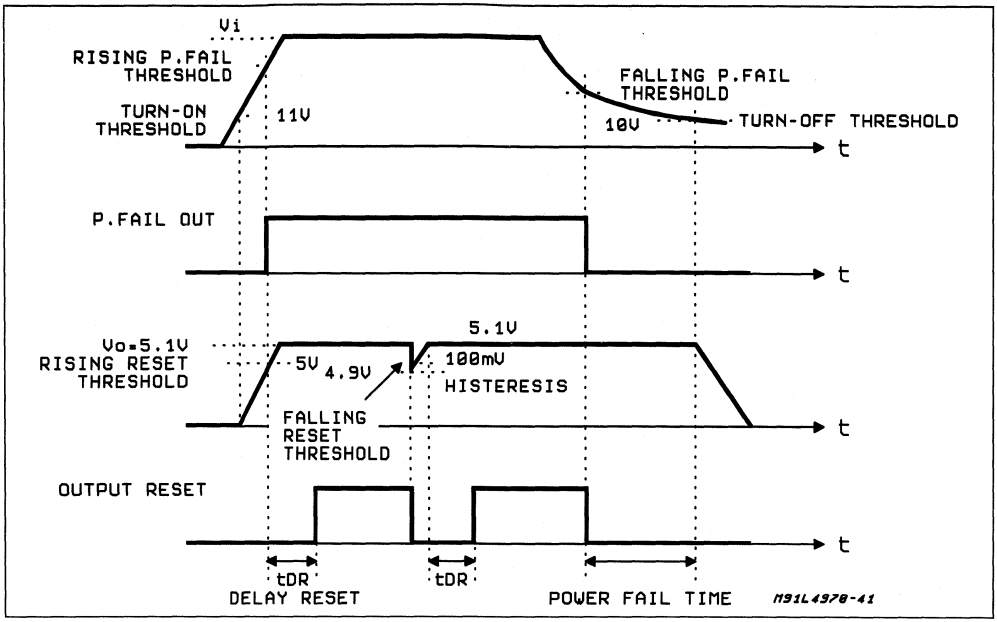
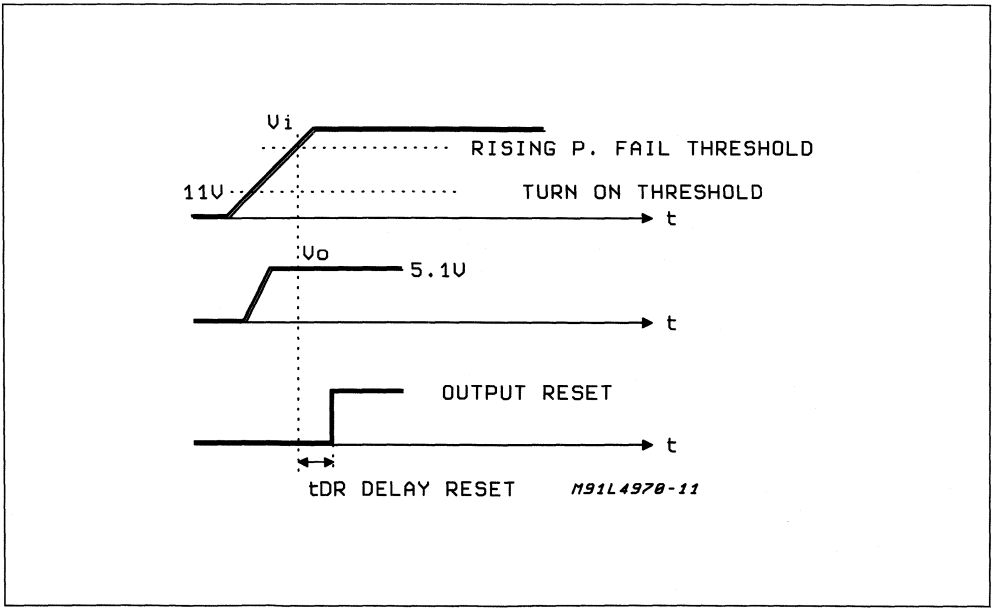


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 2A (**)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 1A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 0.5A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5A to 2A		7	20	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A		0.25	0.4	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	2.5	2.8	3.5	A	
η	Efficiency (*)	I_o = 2A, f = 100KHz V_o = V_{ref} V_o = 12V	75	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 1A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 2A C_9 = 2.2nF	200			KHz	5

(*) Only for DIP version (**) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\,Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	70	100	130	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

SYNC FUNCTION (pin 10)

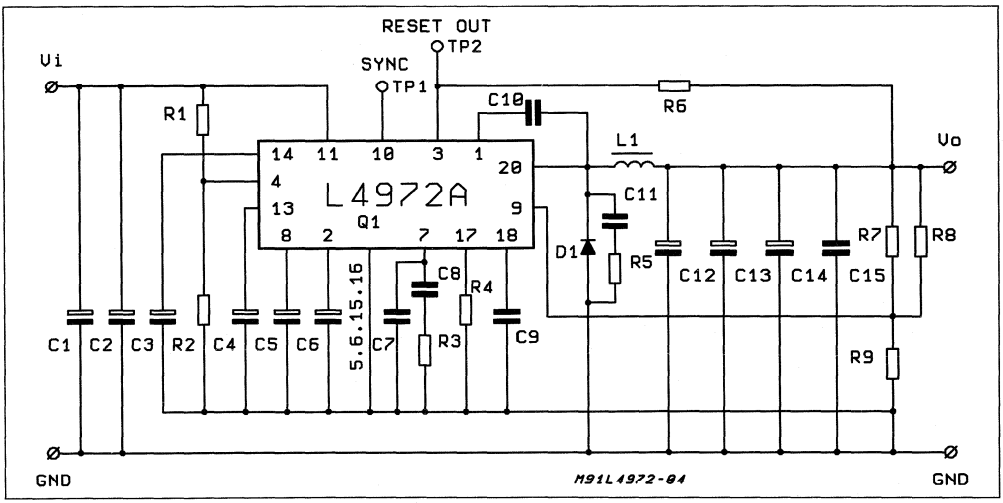
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	V8 = 0; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
I_{10L}	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
I_{10H}	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
tw	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -120	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	40	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.95	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 2A ; f_{SW} = 100KHz)

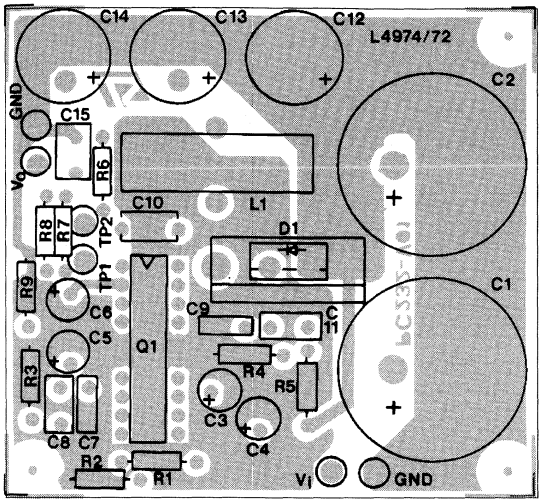
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 7mV (I_o = 0.5 to 2A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available (only for DIP version)



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A.

V_0	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

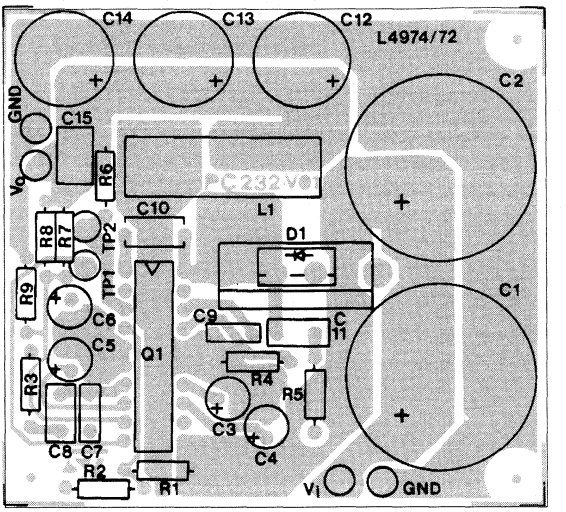


Figure 7 : DC Test Circuits.

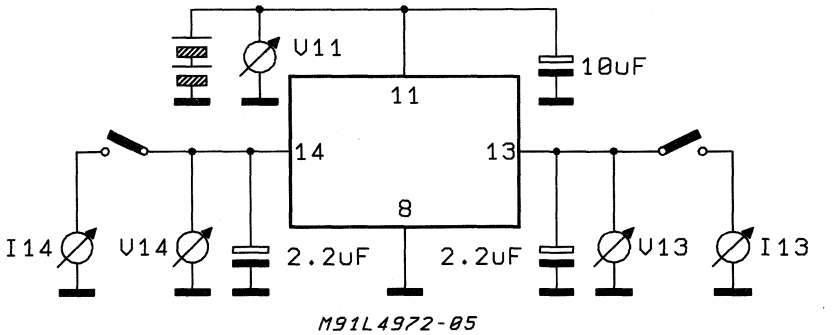


Figure 7A.

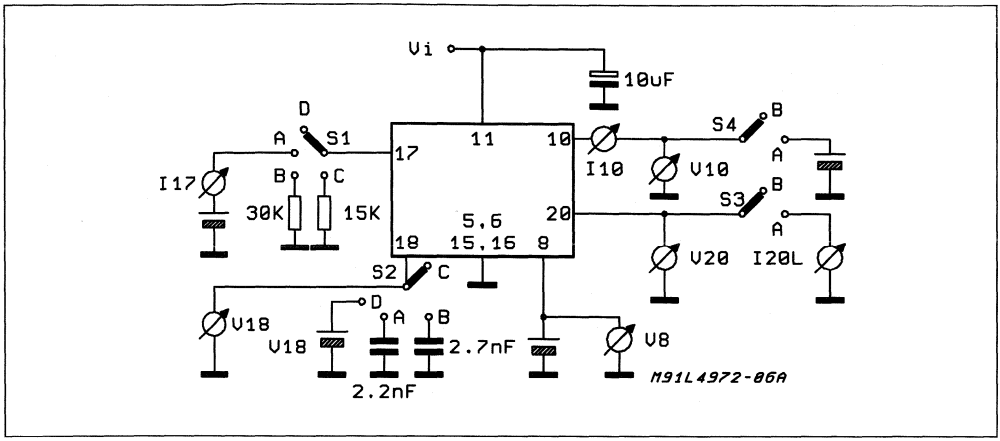


Figure 7B.

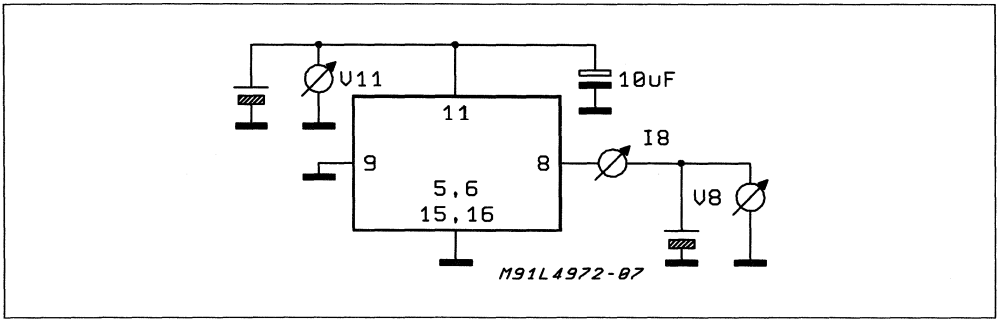


Figure 7C.

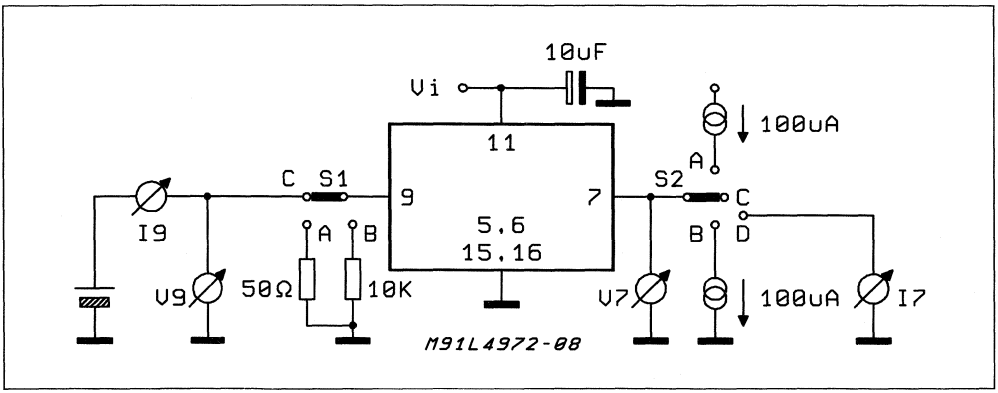


Figure 7D.

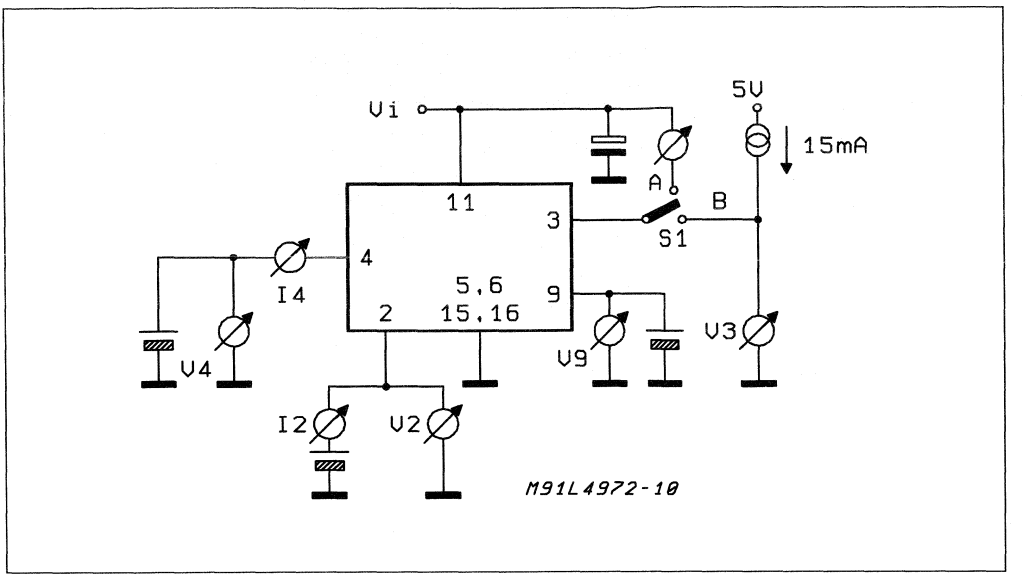


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

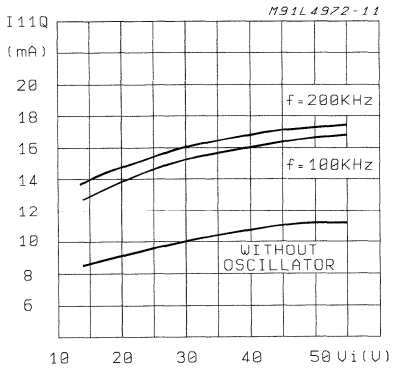


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

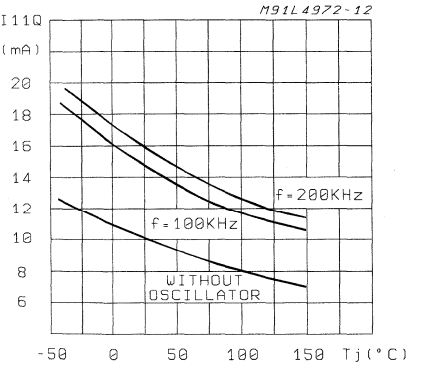


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

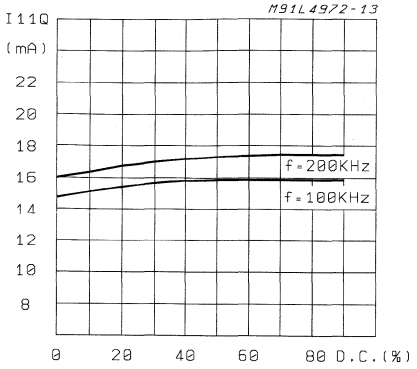


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

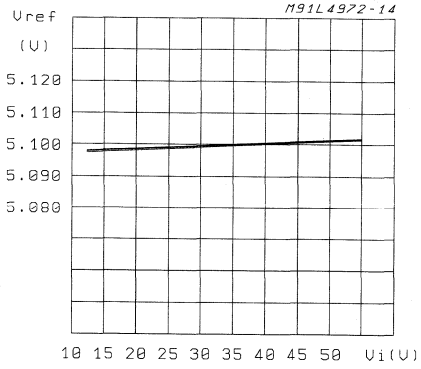


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

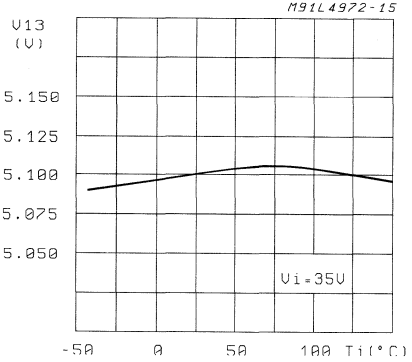


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

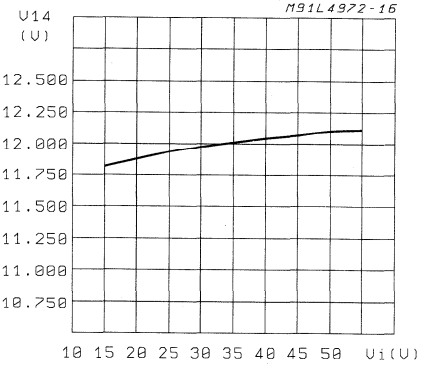


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

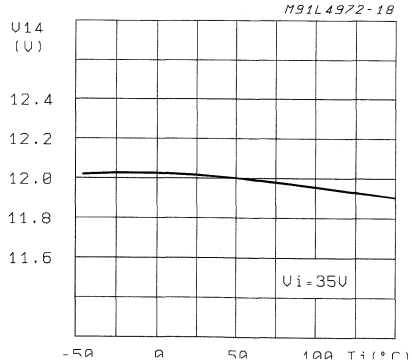


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-

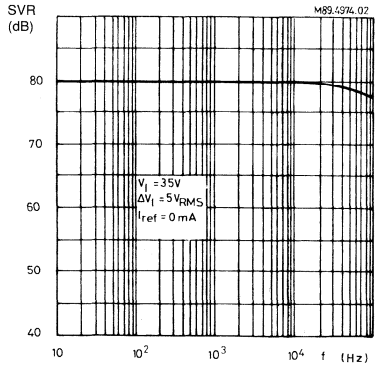


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

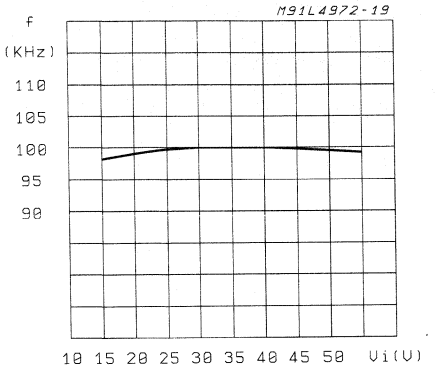


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

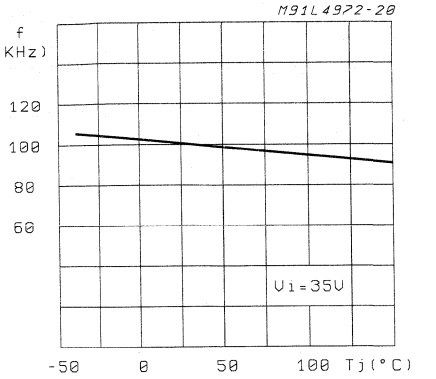


Figure 18 : Switching Frequency vs. R4 (see fig.5).

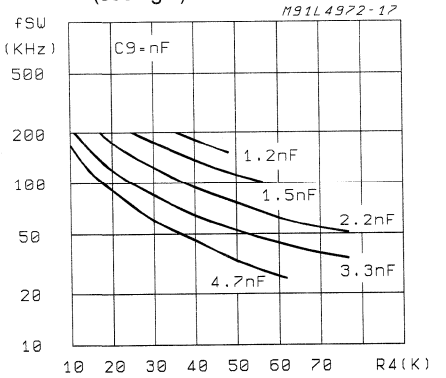


Figure 19 : Maximum Duty Cycle vs. Frequency.

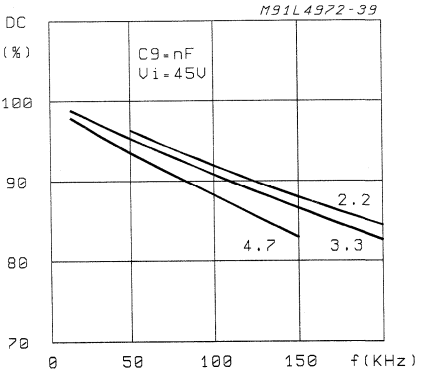


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

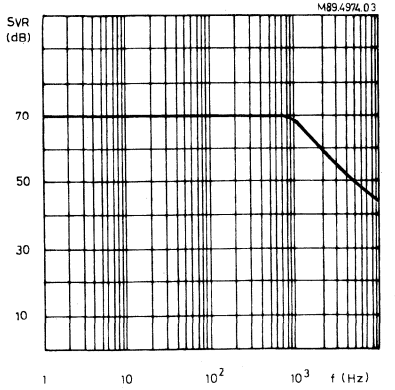


Figure 21 : Efficiency vs. Output Voltage.

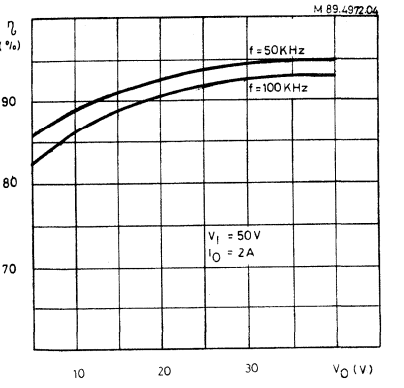


Figure 22 : Line Transient Response (see fig. 5).

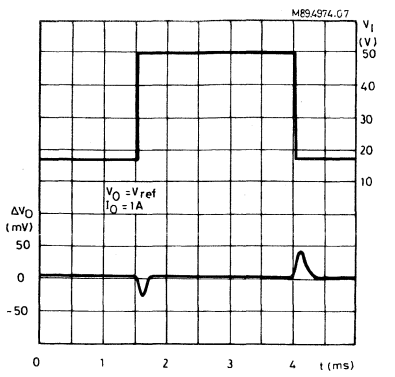


Figure 23 : Load Transient Response (see fig. 5).

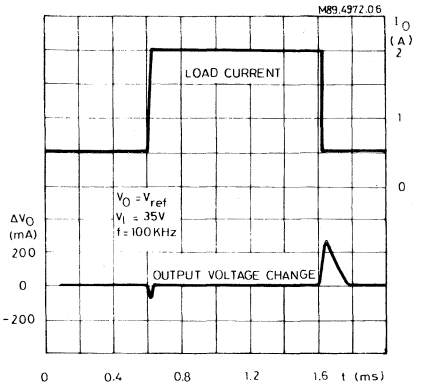


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

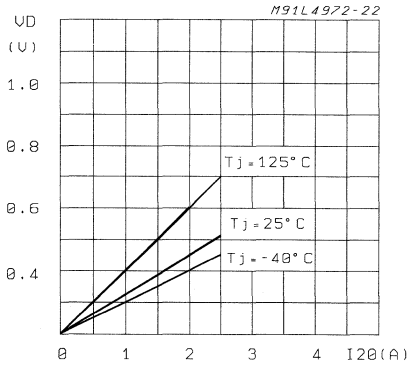


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

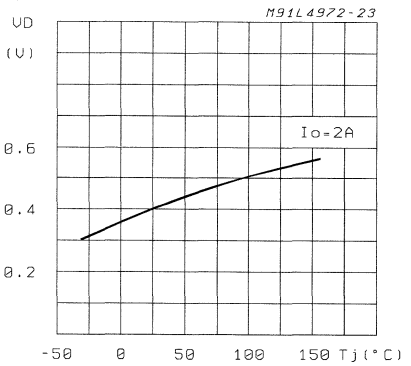


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

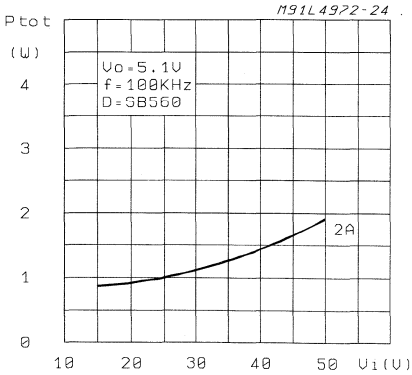


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

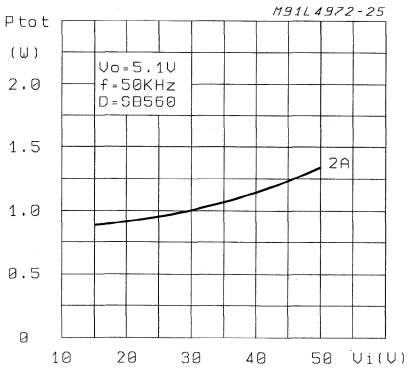


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

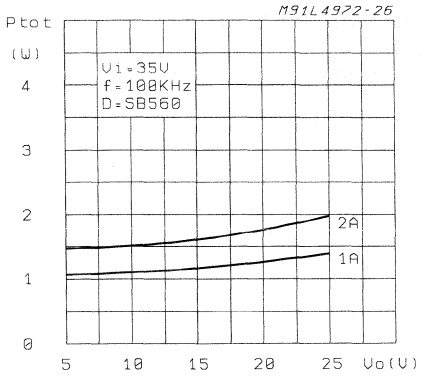


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

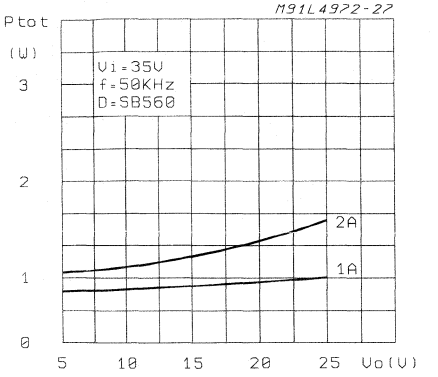


Figure 30 : Power Dissipation (device only) vs. Output Current.

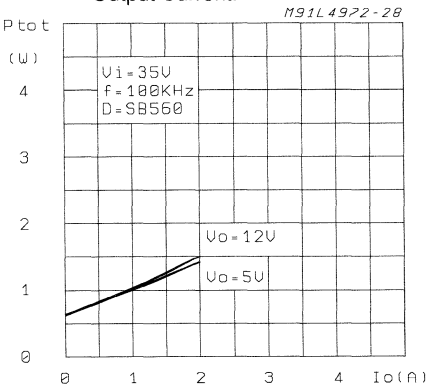


Figure 31 : Power Dissipation (device only) vs. Output Current.

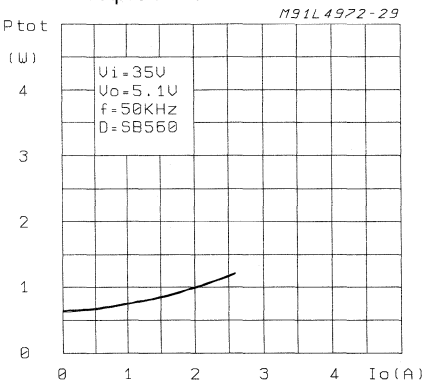


Figure 32 : Efficiency vs. Output Current.

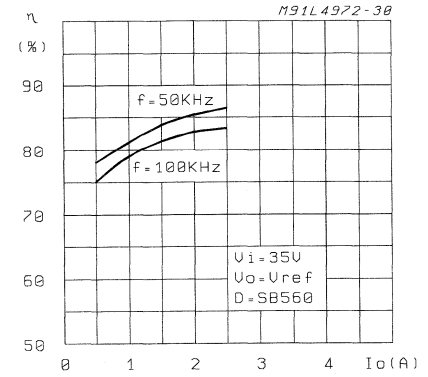


Figure 33 : Test PCB Thermal Characteristic.

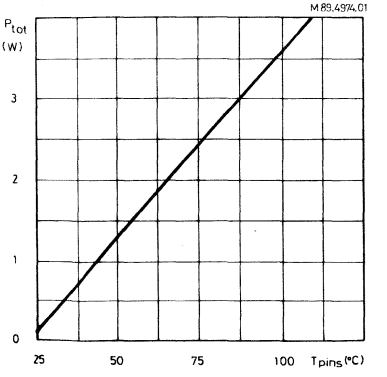


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

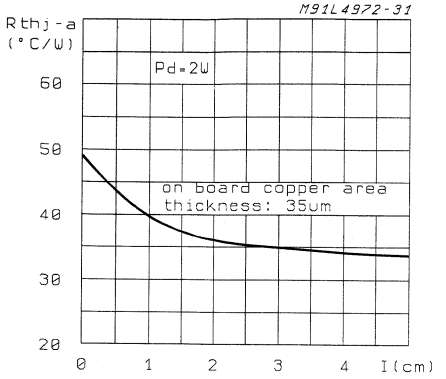


Figure 35: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

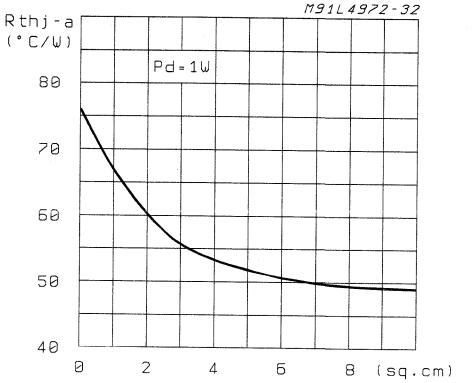


Figure 36: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

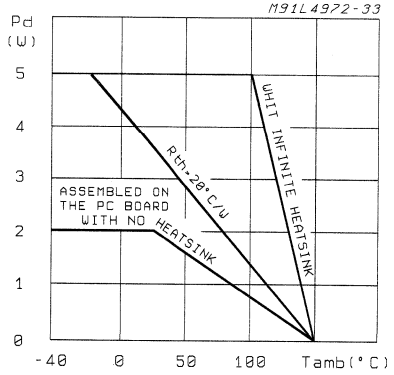


Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature (SO20)

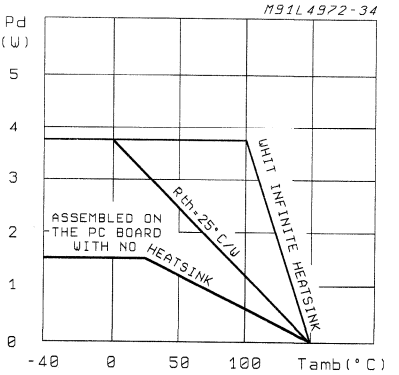


Figure 38: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

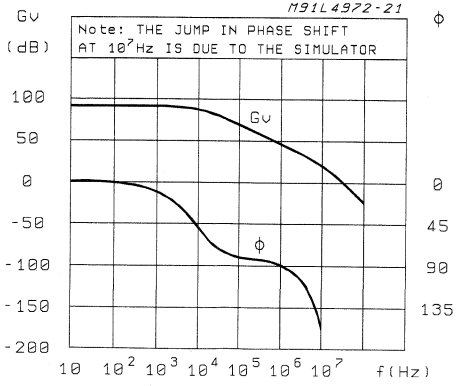


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Figure 39 : 2A – 5.1V Low Cost Application Circuit.

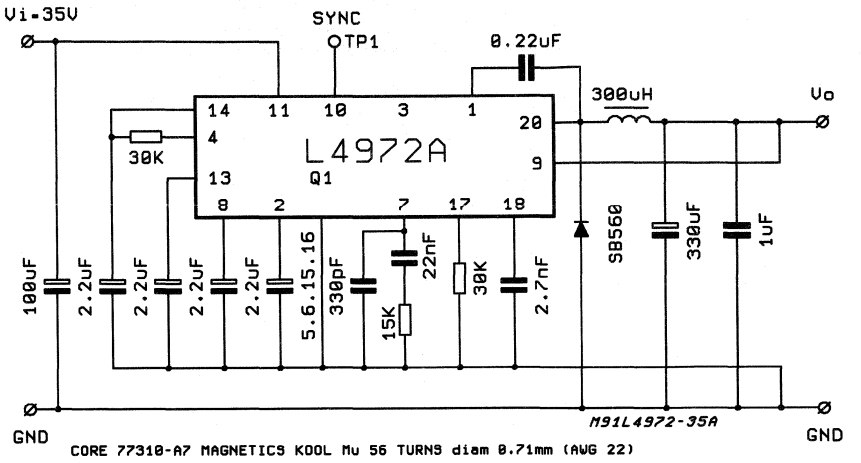


Figure 40 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972A and L4970A.

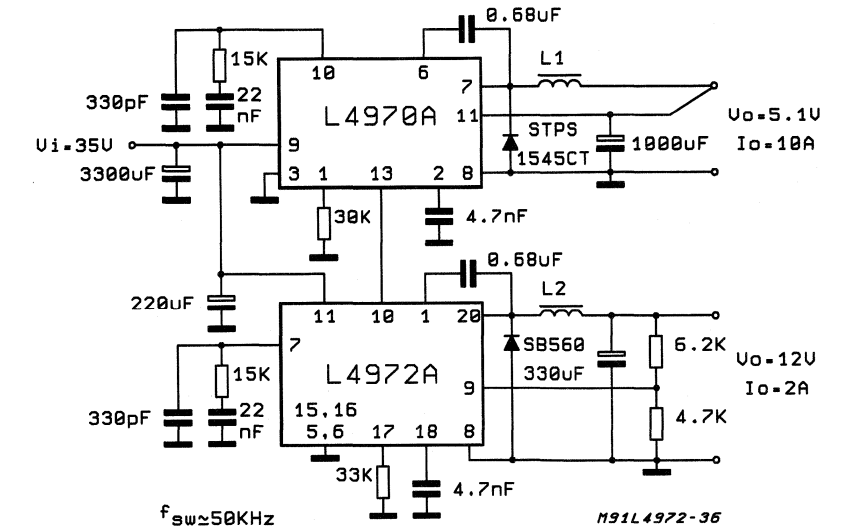


Figure 41 : L4972A's Sync. Example.

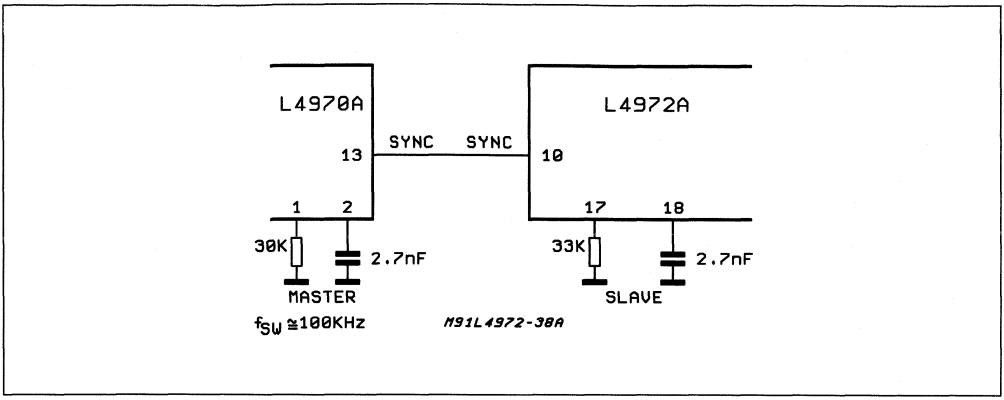
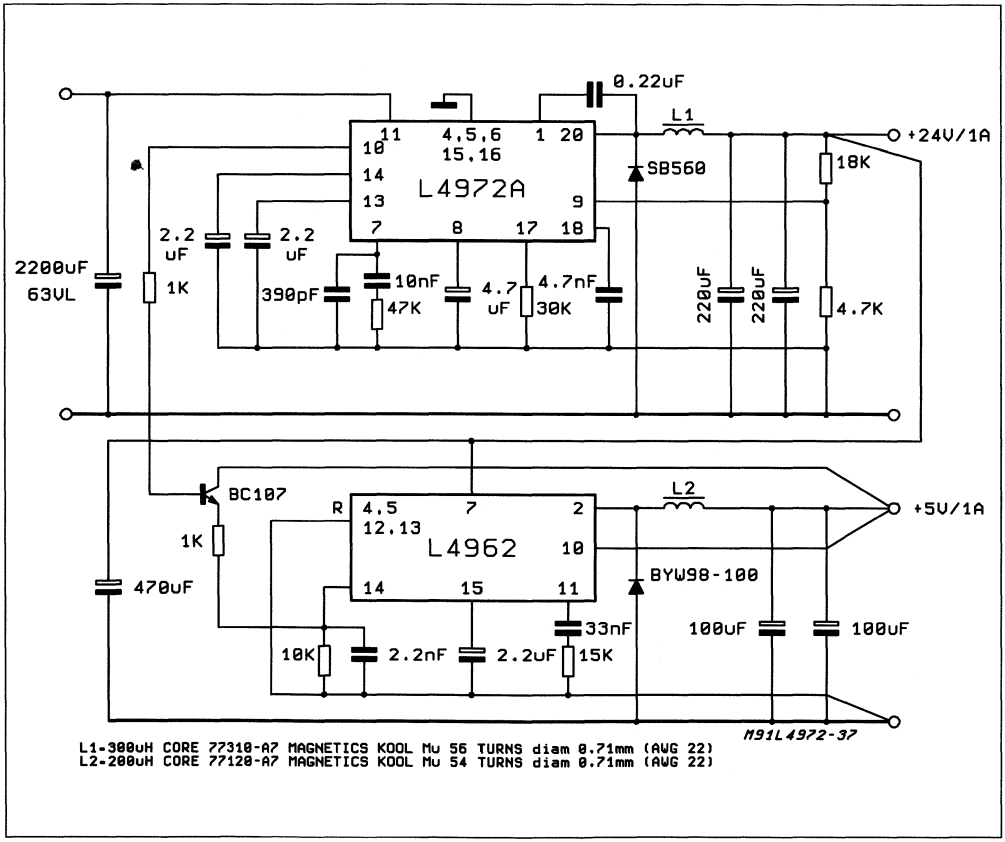


Figure 42: 1A/24V Multiple Supply. Note the synchronization between the L4972A and L4962



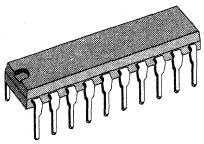
SGS-THOMSON MICROELECTRONICS

L4974A

3.5A SWITCHING REGULATOR

- 3.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

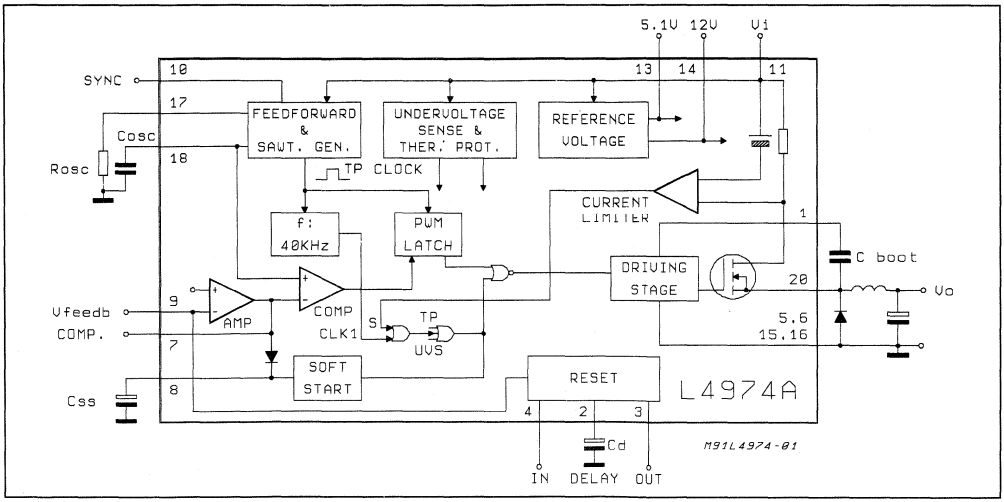
ORDERING NUMBER : L4974A

DESCRIPTION

The L4974A is a stepdown monolithic power switching regulator delivering 3.5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4974A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 plastic package and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

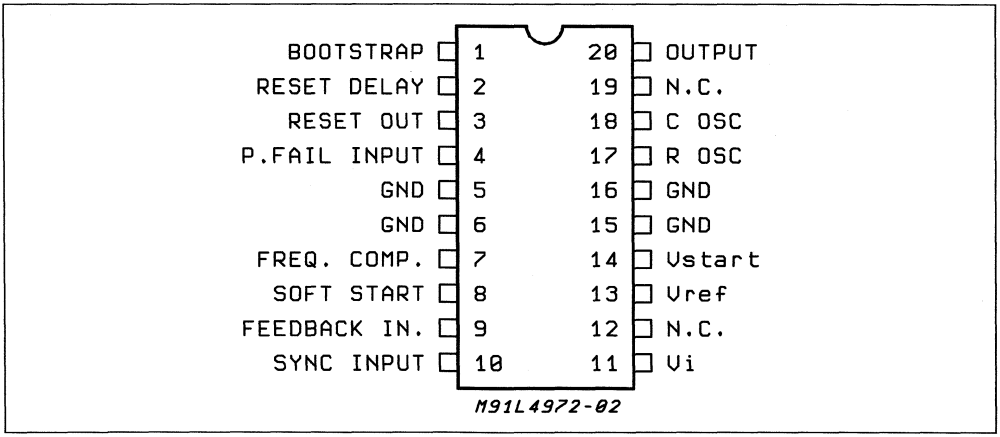
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 1.3	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60	°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4974A's are synchronized by connecting pin 10 inputs togheter or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4974A is a 3.5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 3.5A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

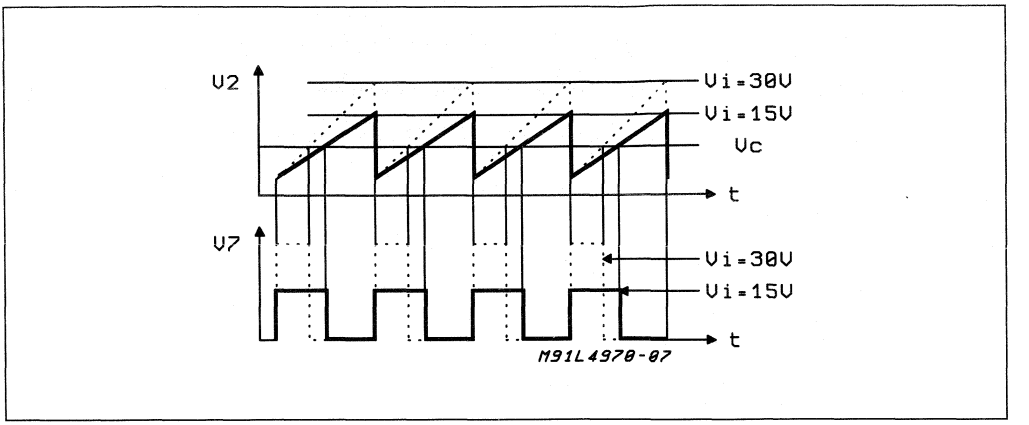


Figure 2 : Soft Start Function.

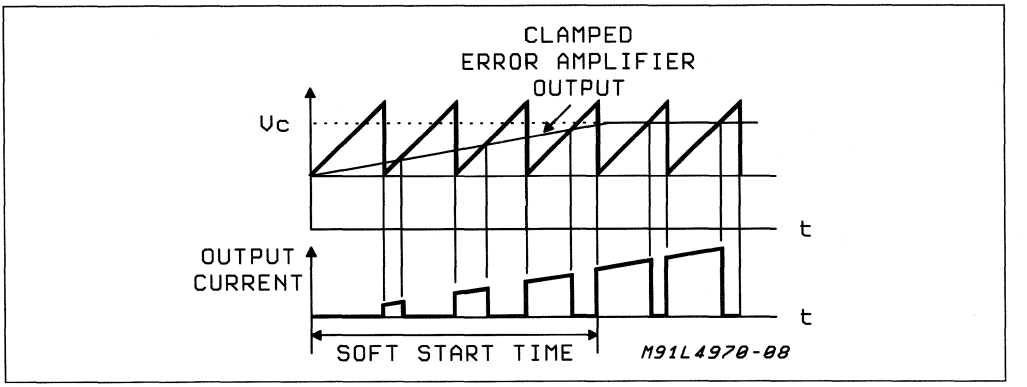


Figure 3 : Limiting Current Function.

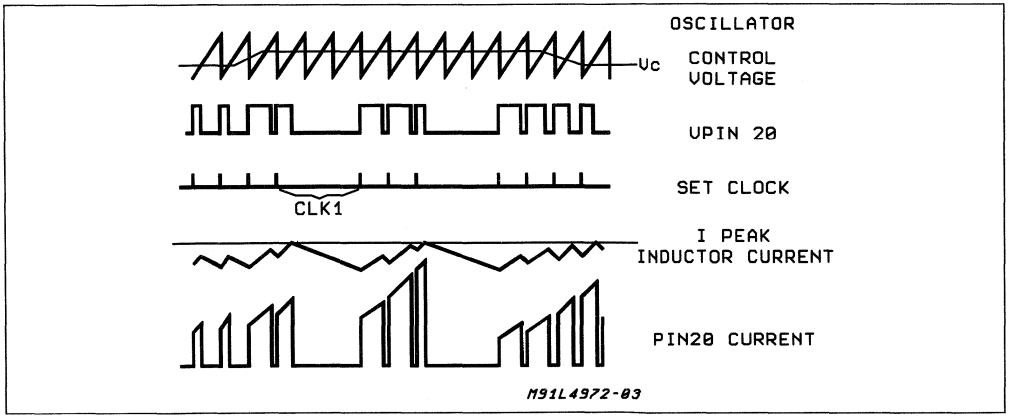
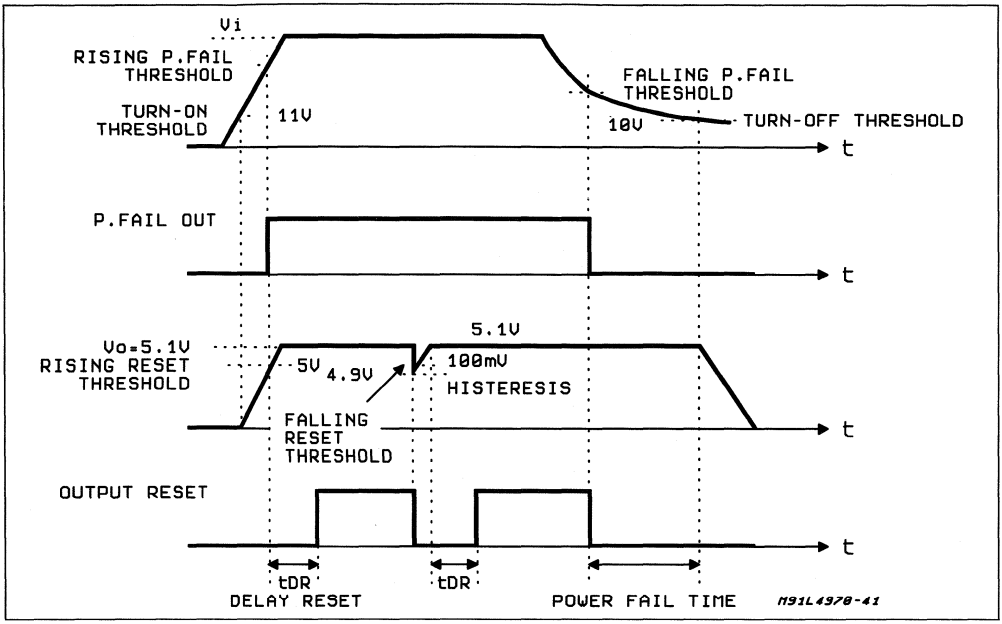
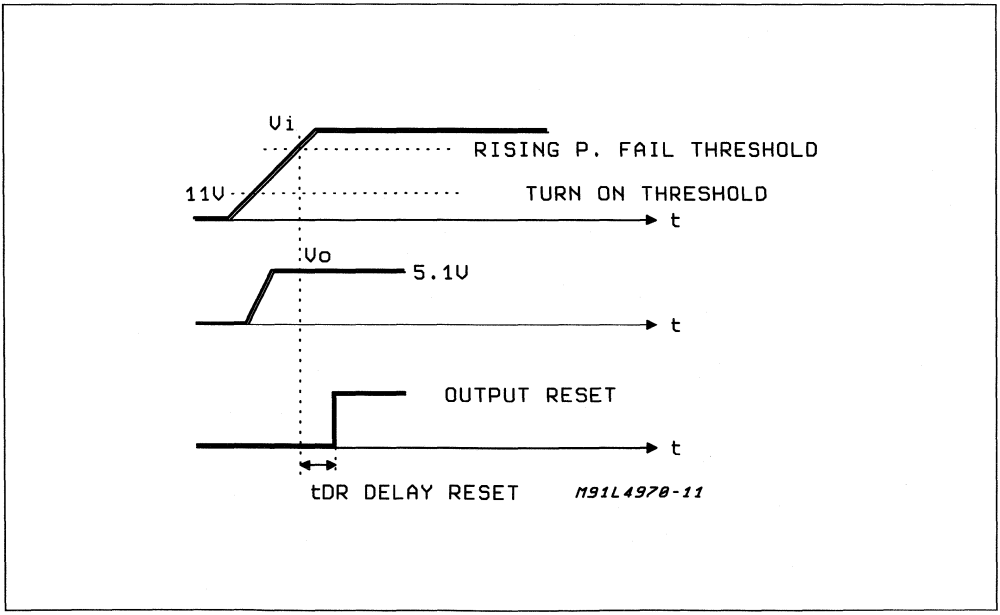


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	$V_o = V_{ref}$ to 40V I_o = 3.5A (*)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 2A; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_I = 15V to 50V I_o = 1A; $V_o = V_{ref}$		12	30	mV	
ΔV_o	Load Regulation	$V_O = V_{ref}$ I_o = 1A to 3.5A		8	25	mV	
		I_o = 2A to 3A		4	10	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A I_o = 3.5A		0.25 0.45	0.4 0.7	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V $V_o = V_{ref}$ to 40V	4	4.75	5.5	A	
η	Efficiency	I_o = 3.5A, f = 100KHz $V_o = V_{ref}$ V_o = 12V	80	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 5A f = 100Hz; $V_o = V_{ref}$	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$ R_4 = 15KΩ I_o = 3.5A C_9 = 2.2nF	200			KHz	5

(*) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\,Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	70	100	130	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = -100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

SYNC FUNCTION (pin 10)

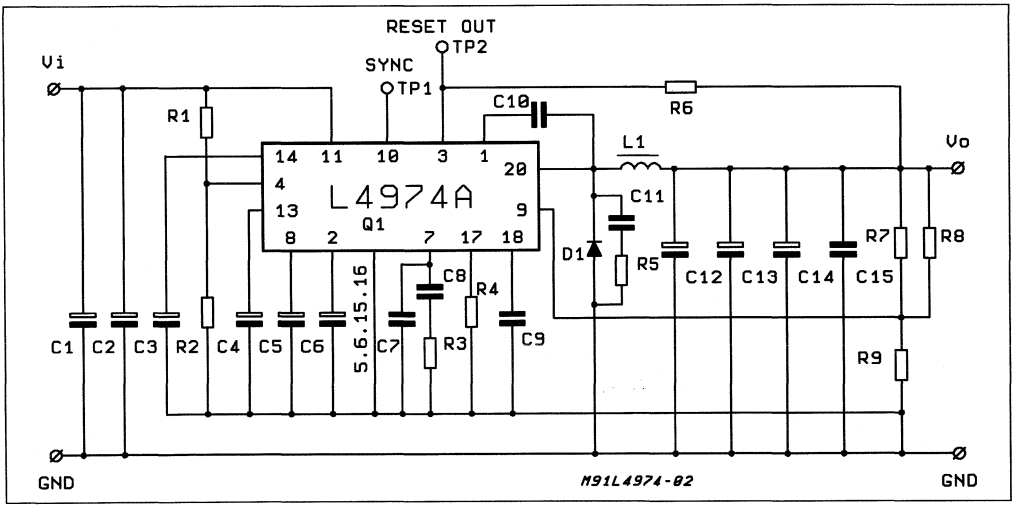
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	$V_8 = 0$; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
$+I_{10L}$	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
$+I_{10H}$	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -120	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	40	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.955	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 3.5A ; f_{sw} = 100KHz)

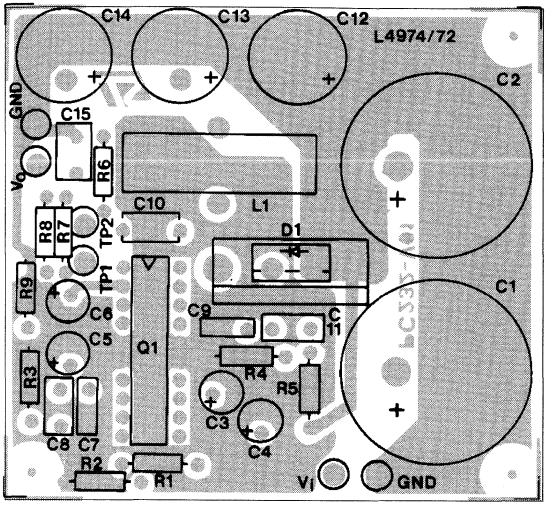
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 8mV (I_o = 1 to 3.5A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A.

V_0	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

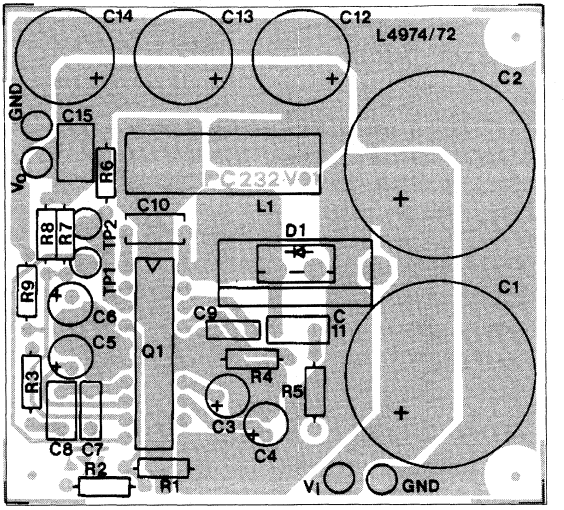


Figure 7 : DC Test Circuits.

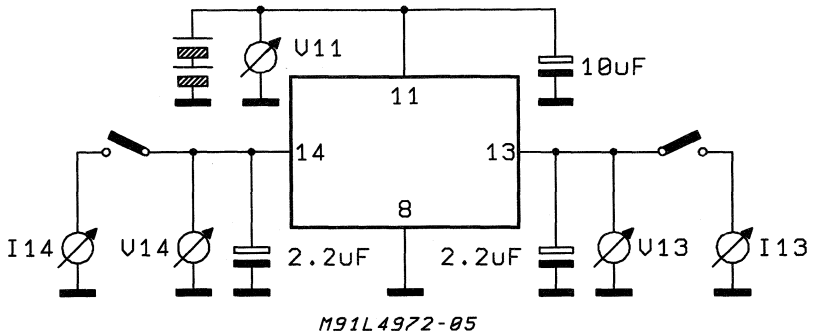


Figure 7A.

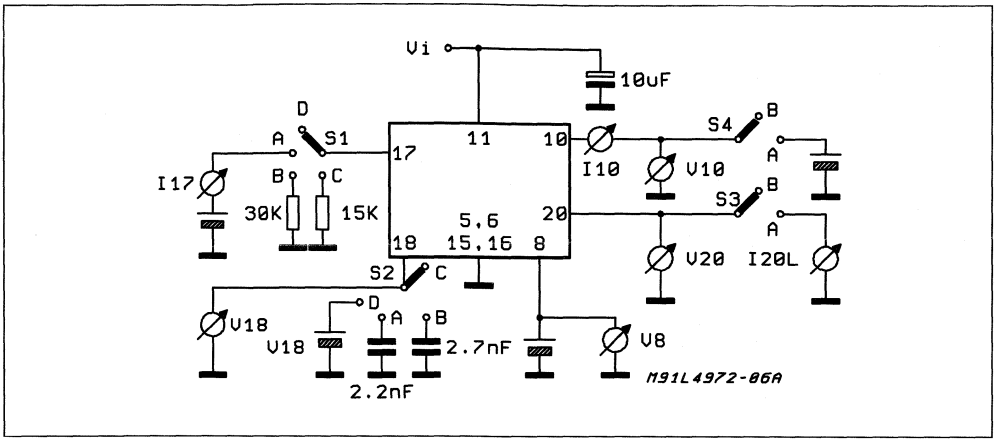


Figure 7B.

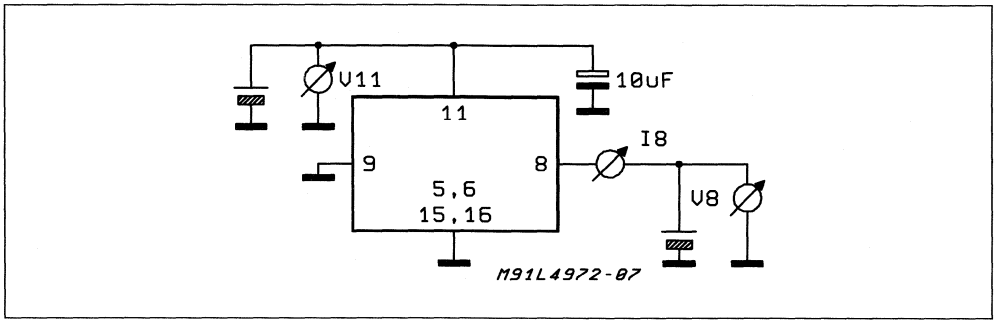


Figure 7C.

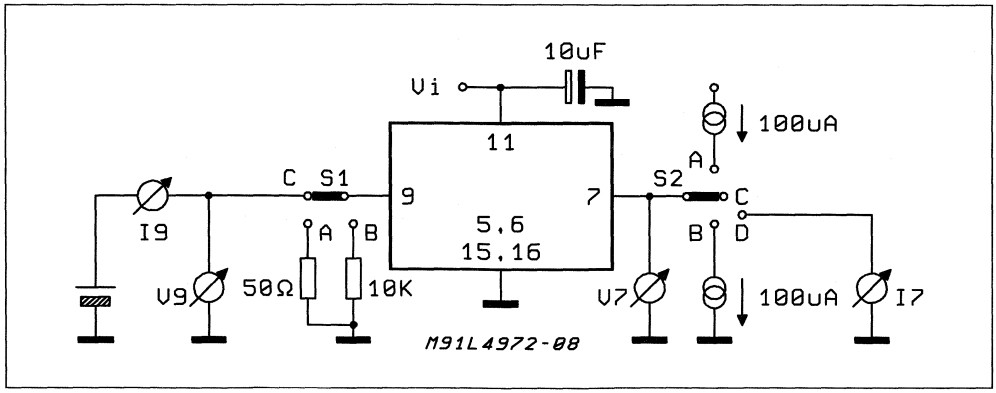


Figure 7D.

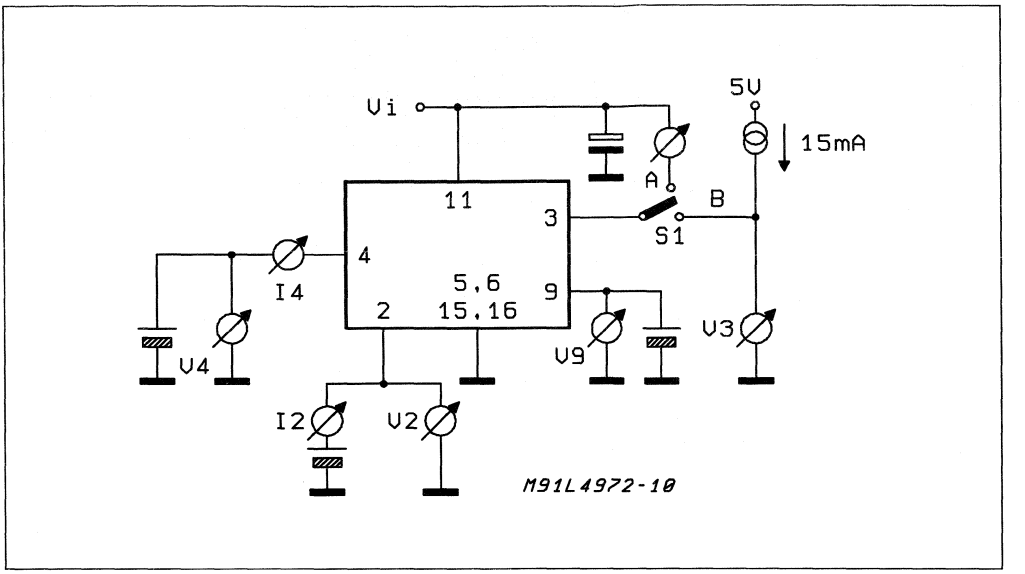


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

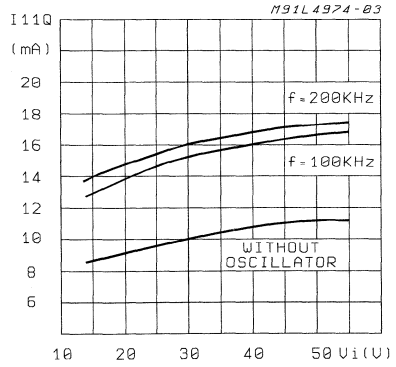


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

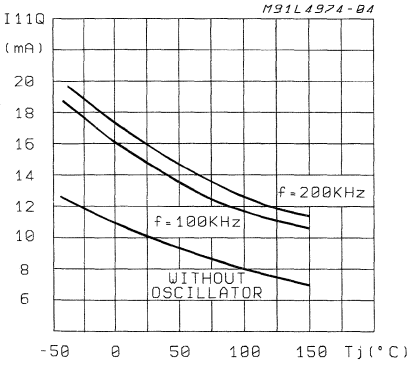


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

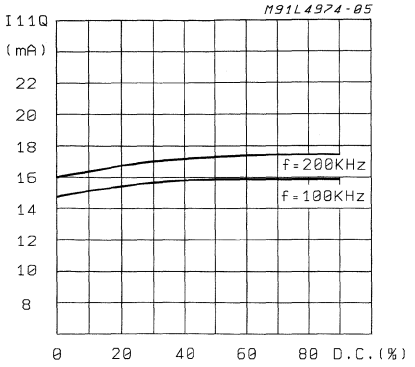


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

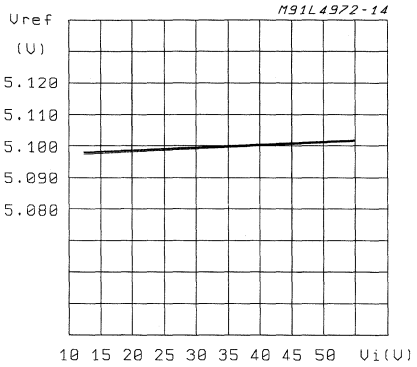


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

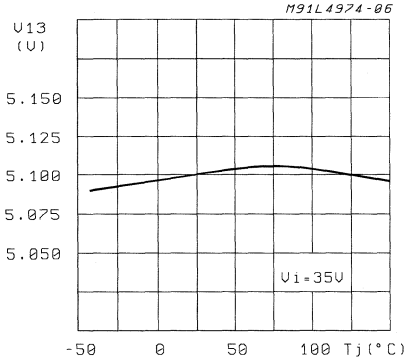


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

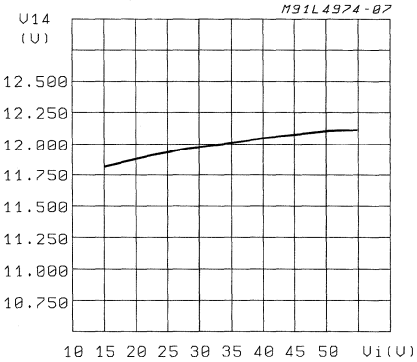


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

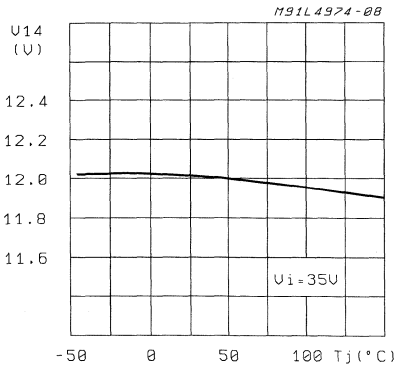


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-

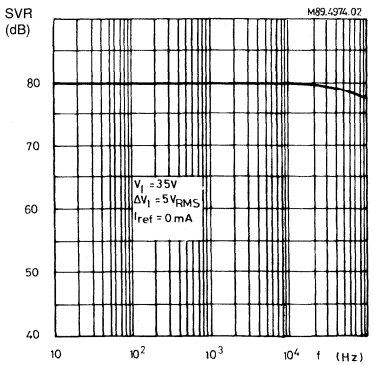


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

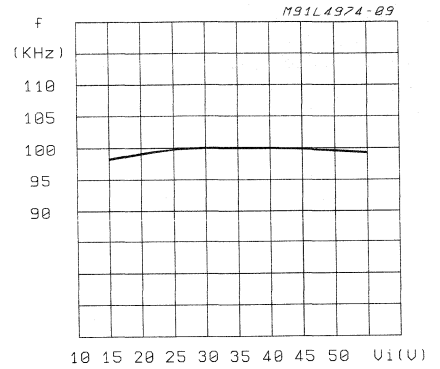


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

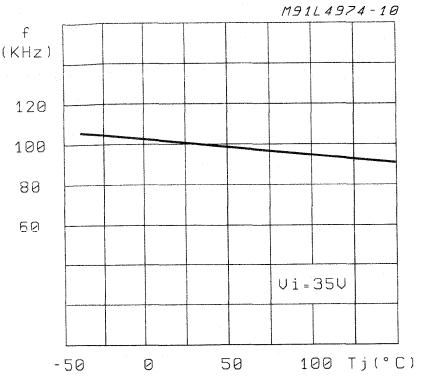


Figure 18 : Switching Frequency vs. R4 (see fig.5).

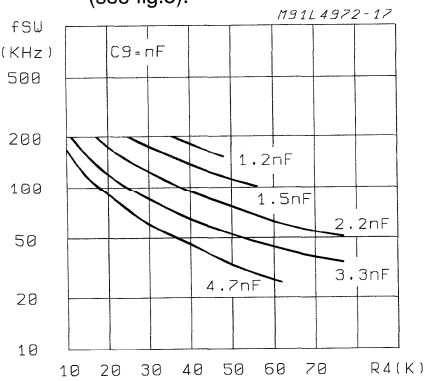


Figure 19 : Maximum Duty Cycle vs. Frequency.

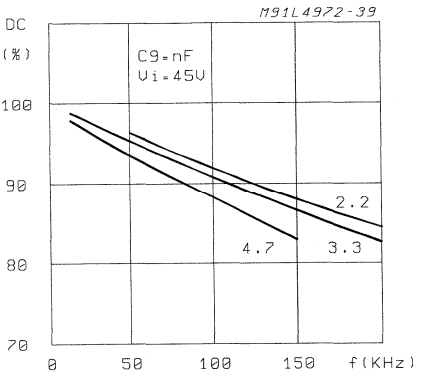


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

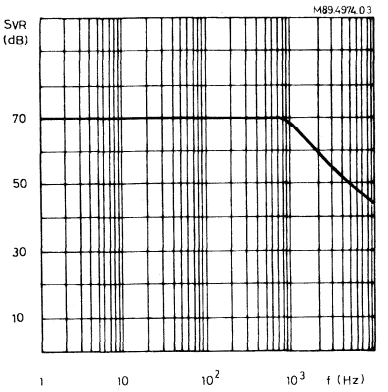


Figure 21 : Efficiency vs. Output Voltage.

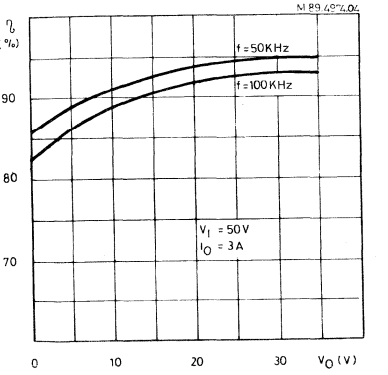


Figure 22 : Line Transient Response (see fig. 5).

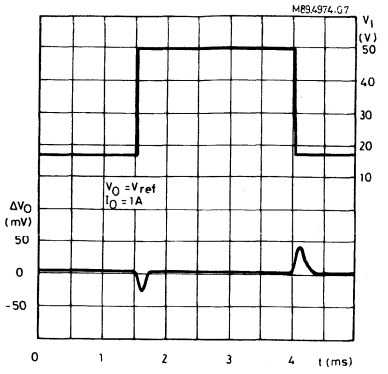


Figure 23 : Load Transient Response (see fig. 5).

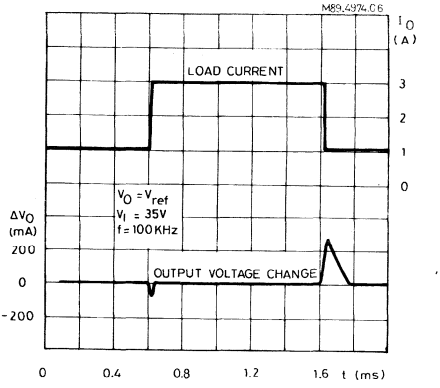


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

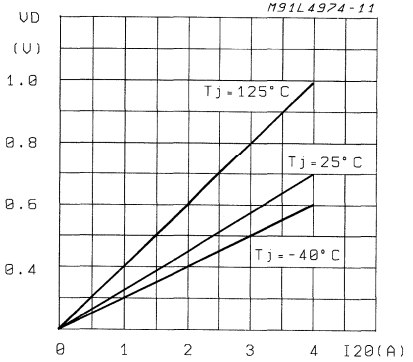


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

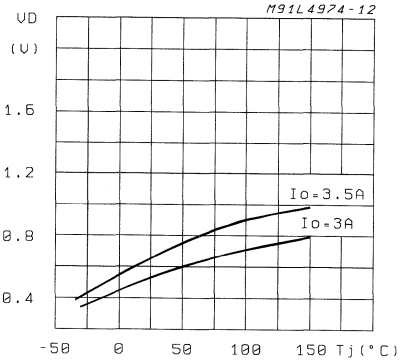


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

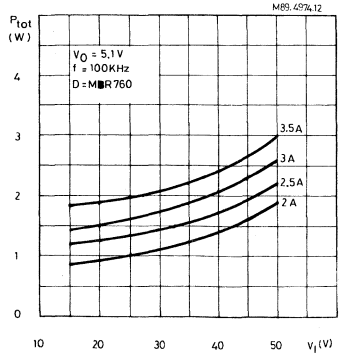


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

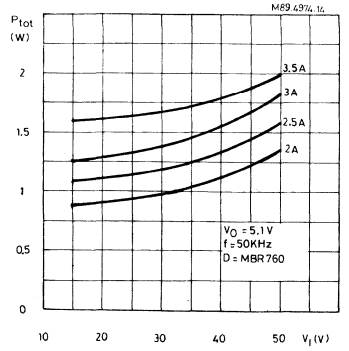


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

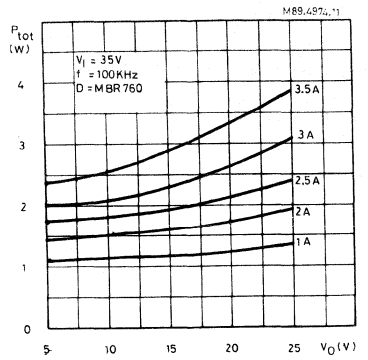


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

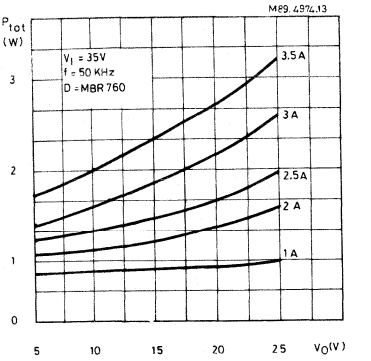


Figure 30 : Power Dissipation (device only) vs. Output Current.

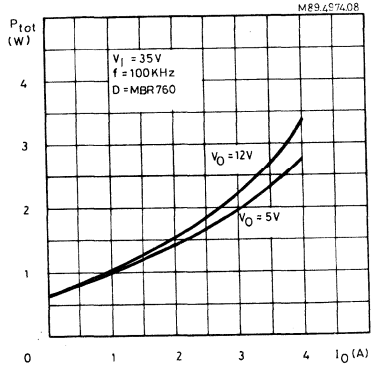


Figure 31 : Power Dissipation (device only) vs. Output Current.

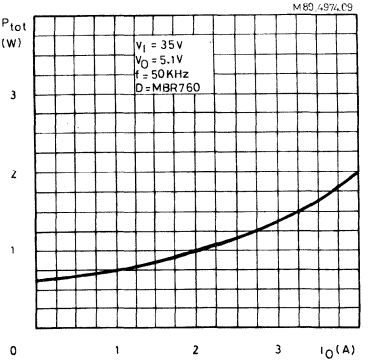


Figure 32 : Efficiency vs. Output Current.

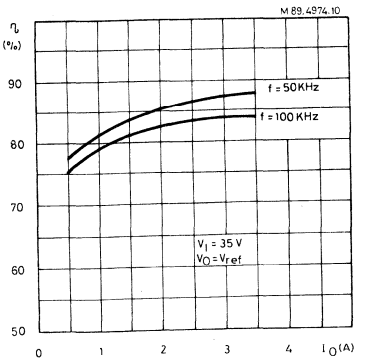


Figure 33 : Test PCB Thermal Characteristic.

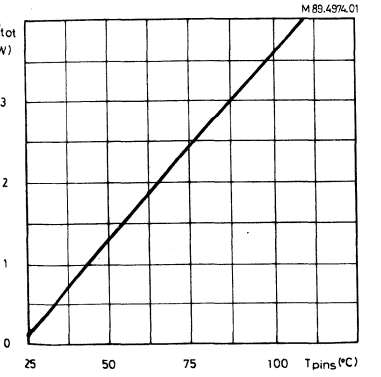


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

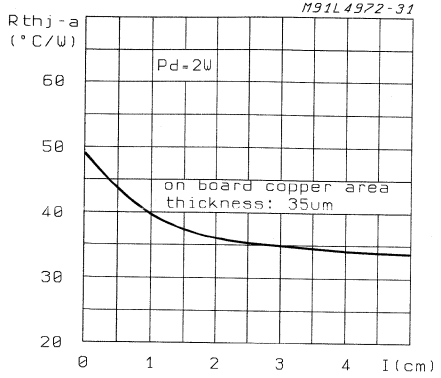


Figure 35: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

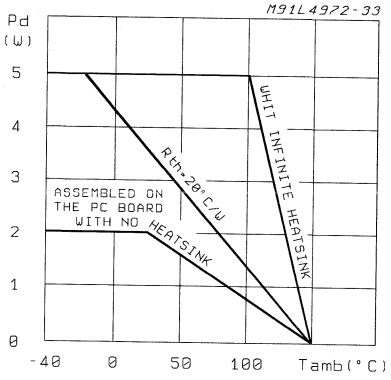


Figure 36: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

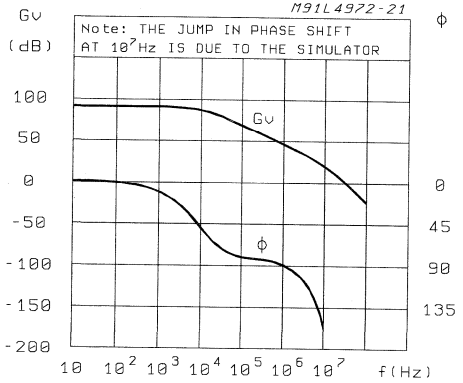


Figure 37 : 3.5A – 5.1V Low Cost Application Circuit.

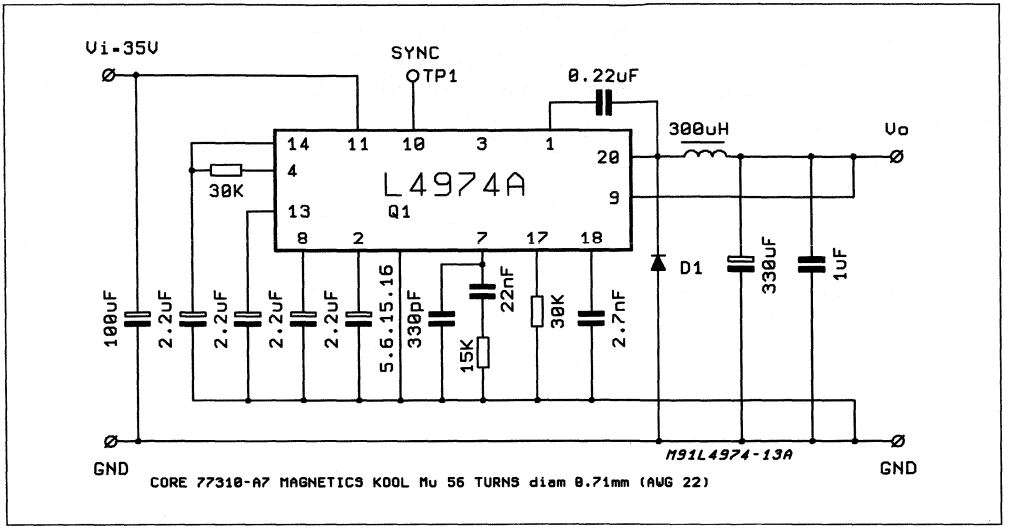


Figure 38 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4974A and L4970A.

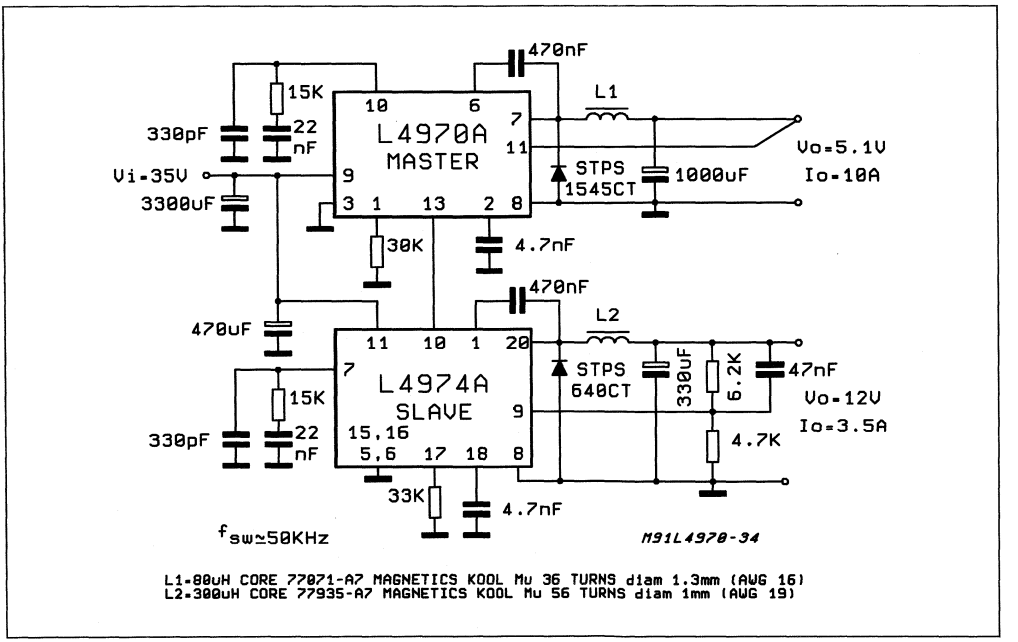


Figure 39 : L4974A's Sync. Example.

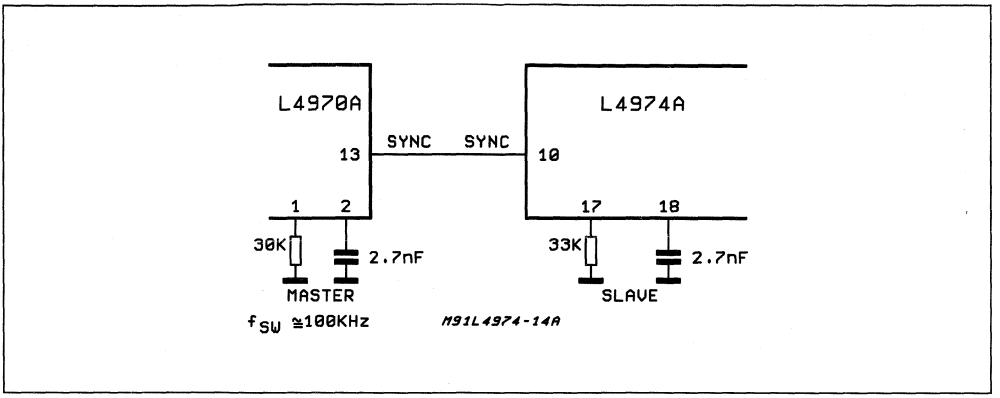
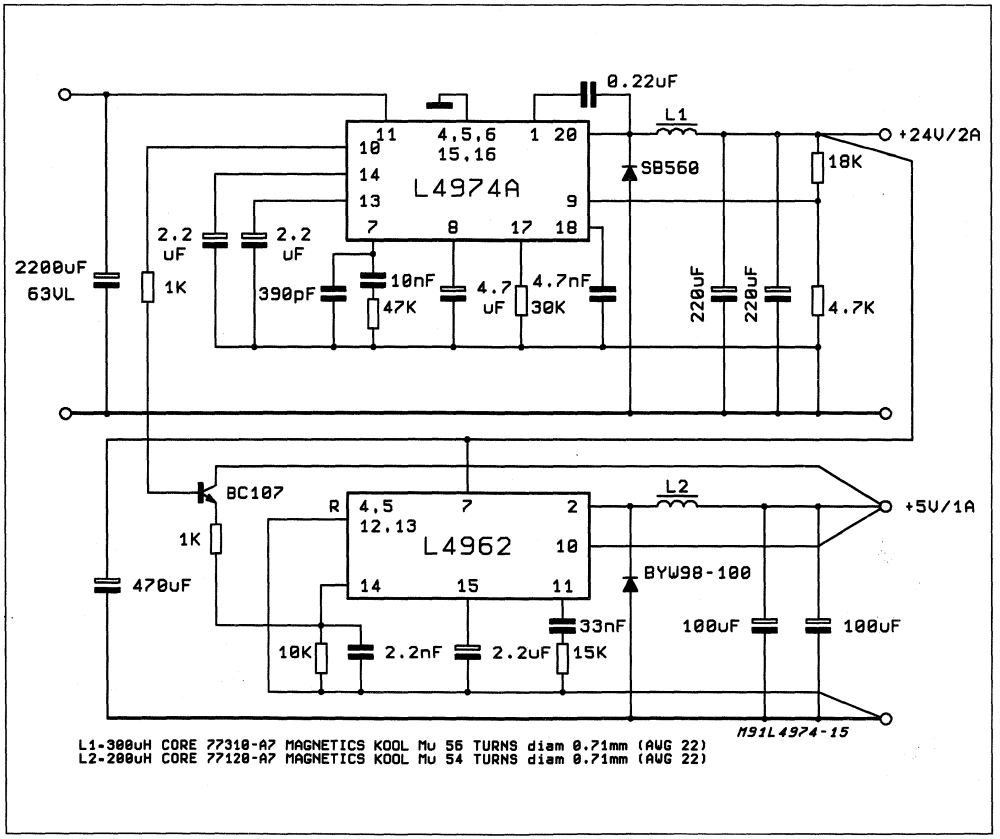


Figure 40: 1A/24V Multiple Supply. Note the synchronization between the L4974A and L4962



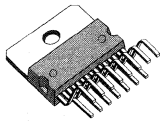
SGS-THOMSON MICROELECTRONICS

L4975A

5A SWITCHING REGULATOR

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



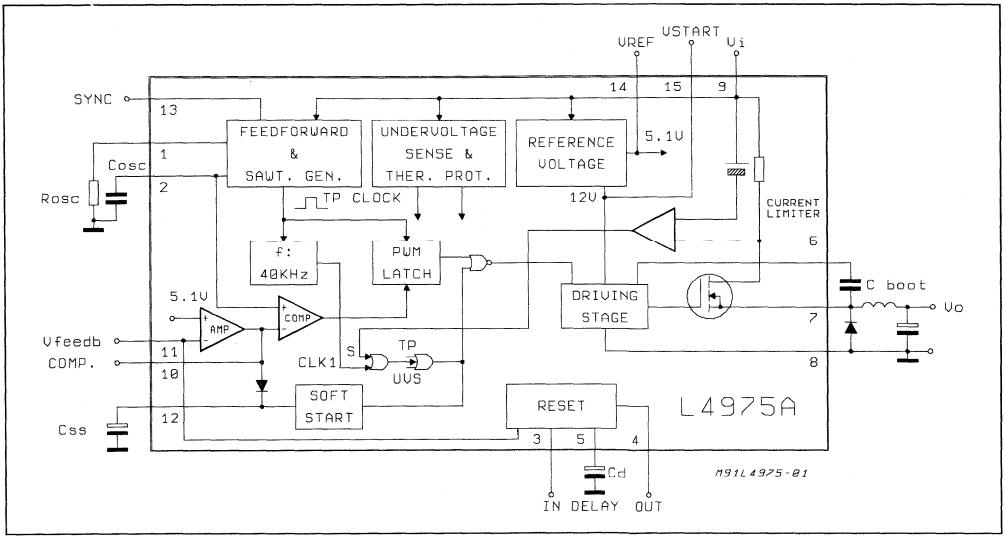
Multiwatt15V
ORDERING NUMBER: L4975A

DESCRIPTION

The L4975A is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

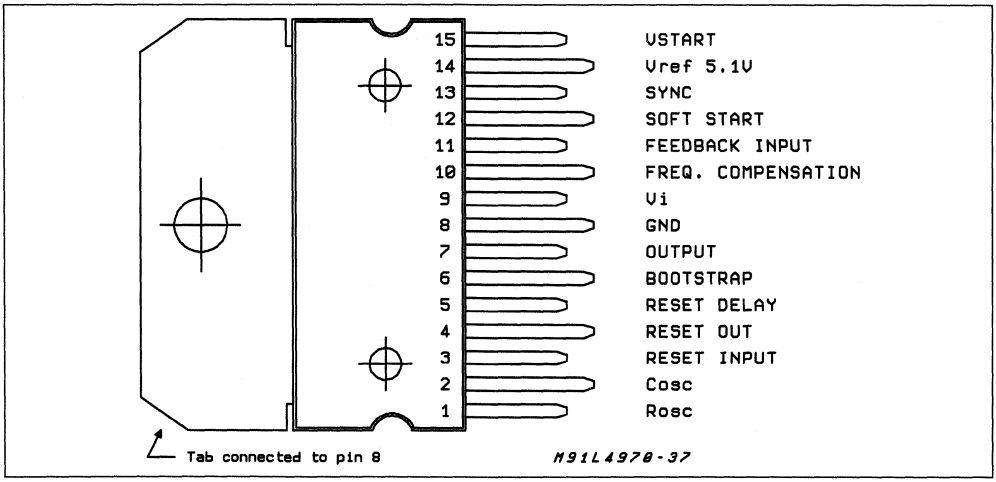
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4975A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4975A is a 5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 5A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

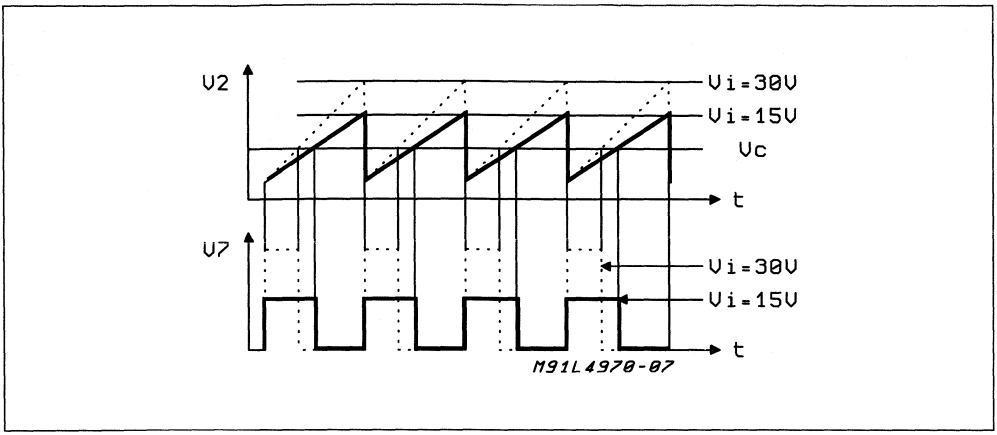


Figure 2: Soft Start Function

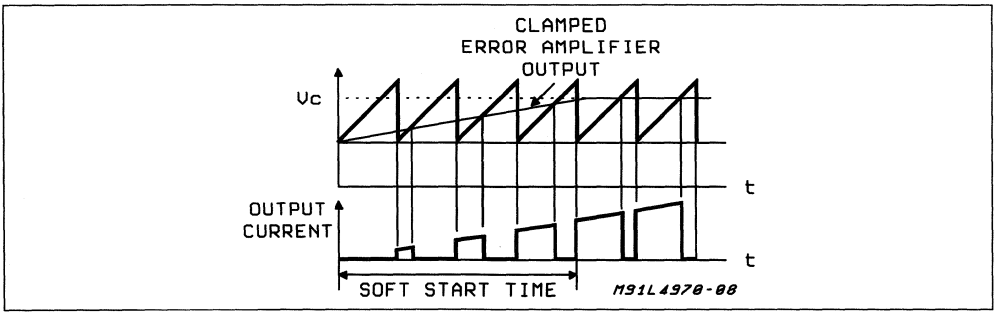
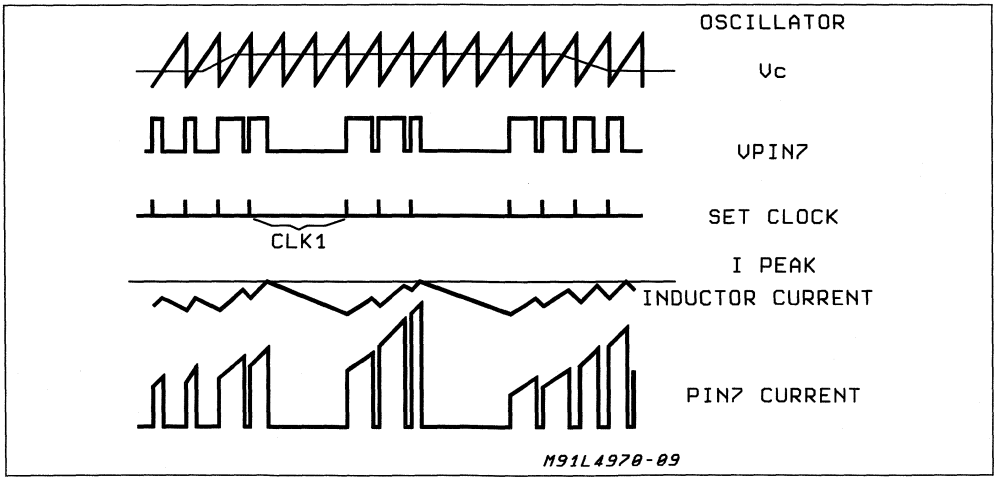


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

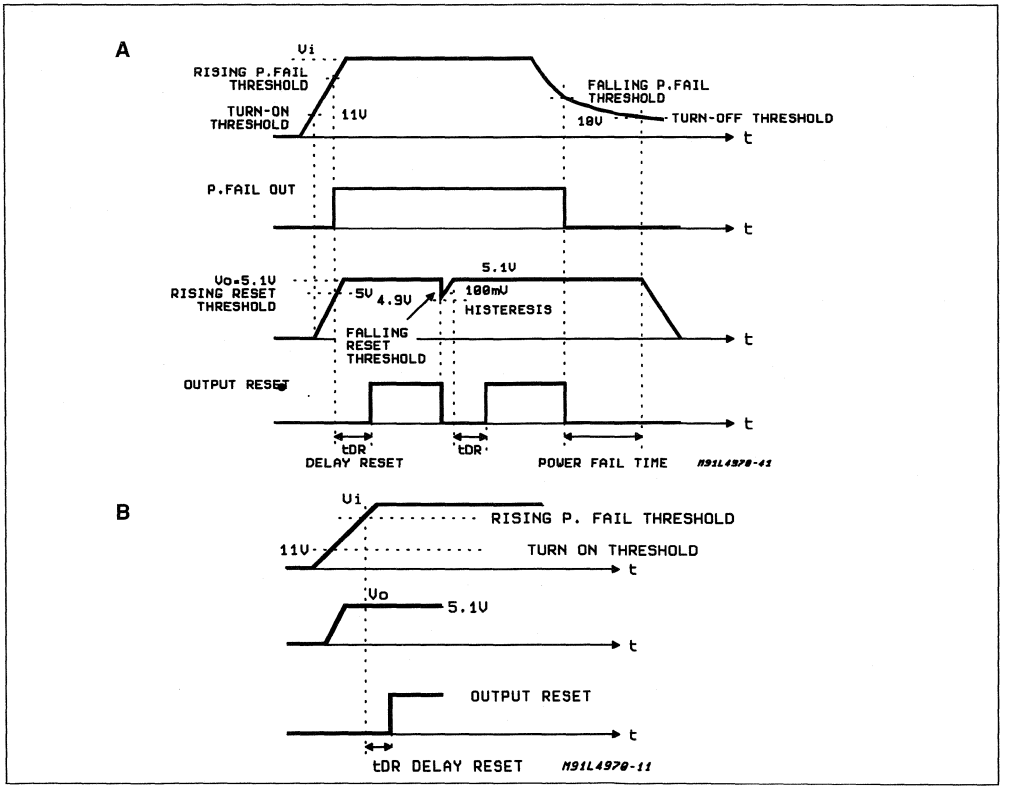
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 5A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 2A to 4A I_o = 1A to 5A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 3A I_o = 5A		0.4 0.55	0.6 0.8	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V V_o = V_{ref} to 40V	5.5	6.5	7.5	A	5
η	Efficiency	I_o = 3A V_o = V_{ref} V_o = 12V	 70	 75 80		 % %	5
		I_o = 5A V_o = V_{ref} V_o = 12V	 80	 85 92		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 5A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	V_i = 15V		2.5		V	7A
		S2 = B	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA		2.4	2.7		mA	7A

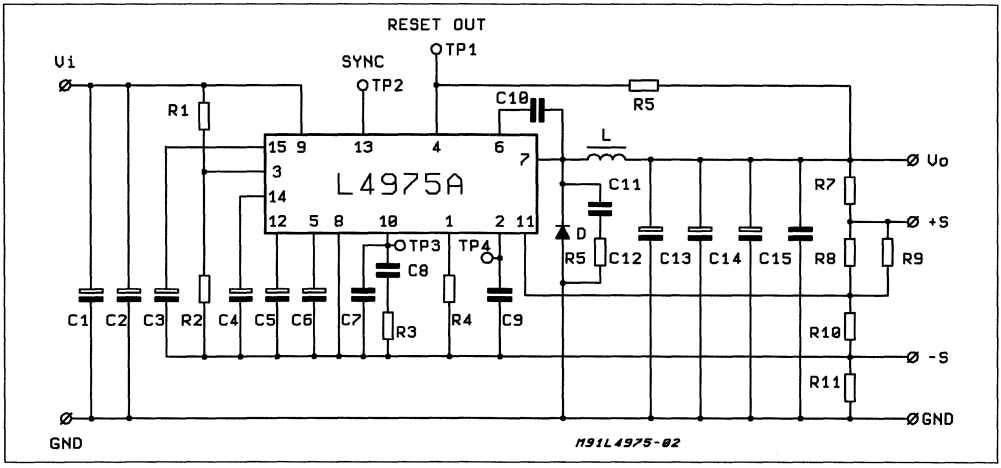
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_2 = V_{13} = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

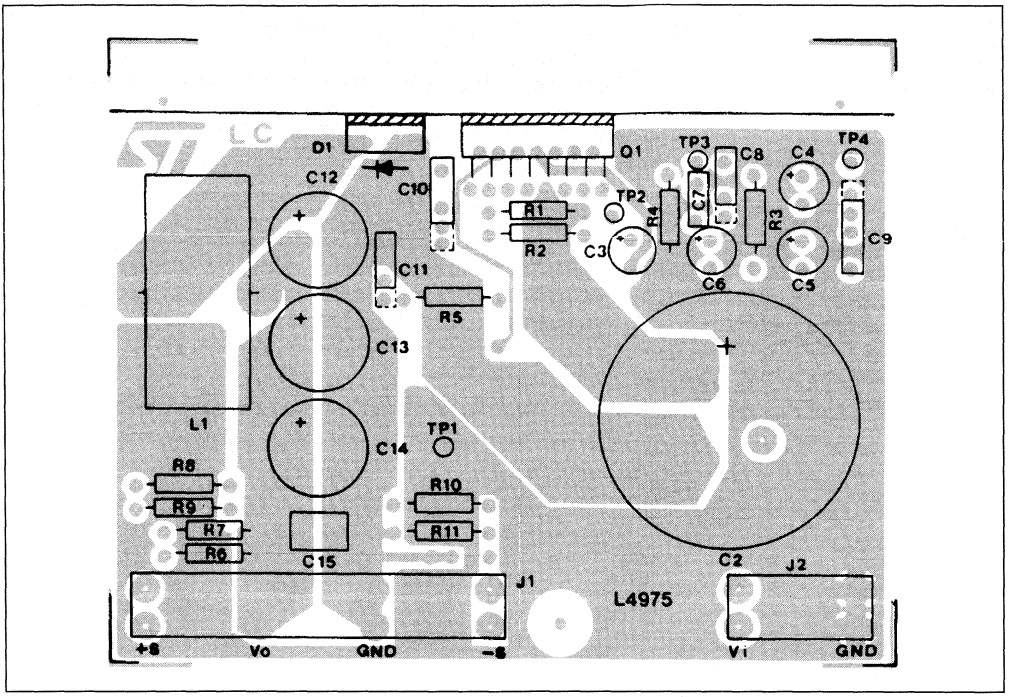
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 5A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 5A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 24 TURNS Ø 1.1mm (AWG 17) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

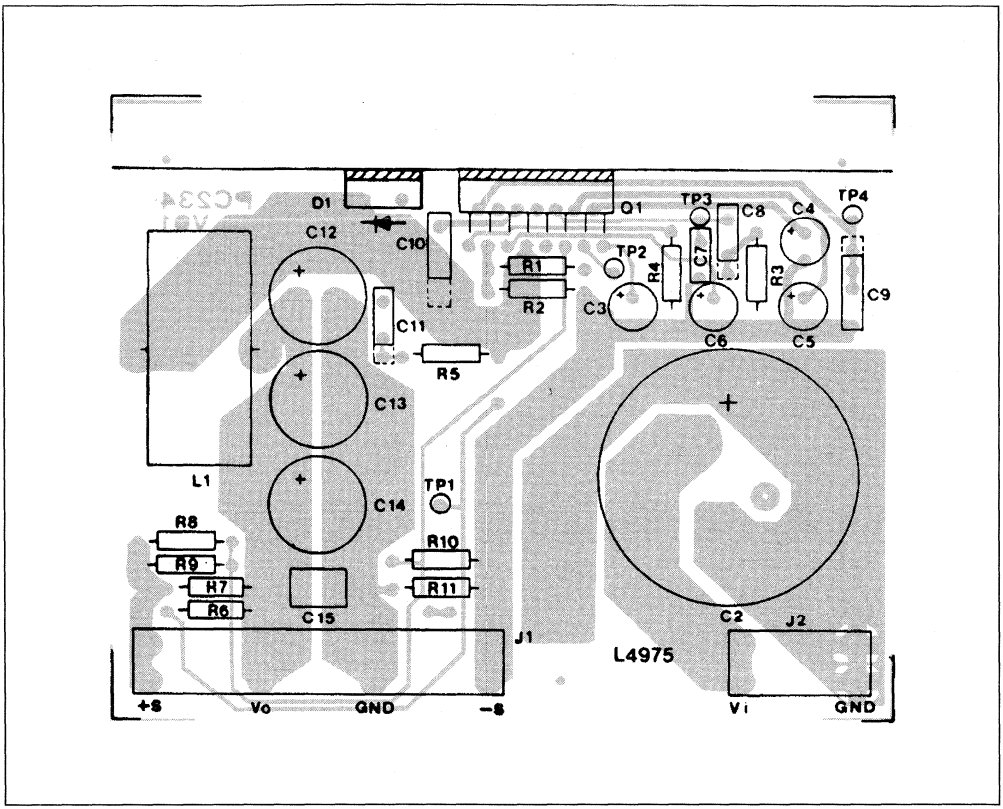


Figure 7: DC Test Circuits

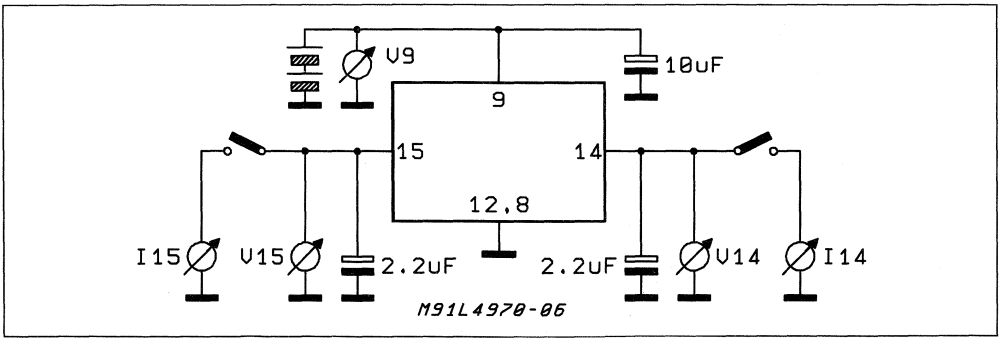


Figure 7A

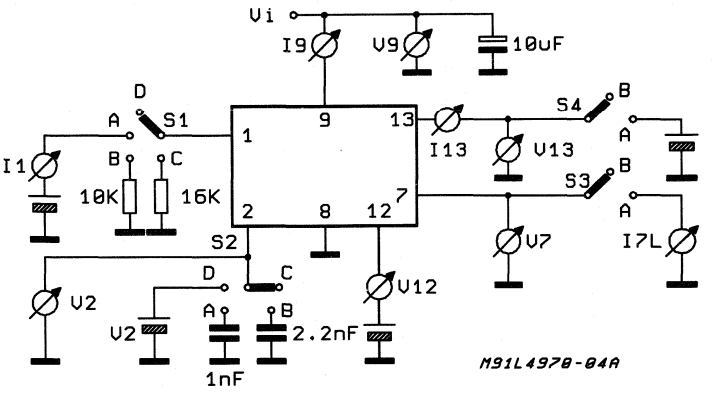


Figure 7B

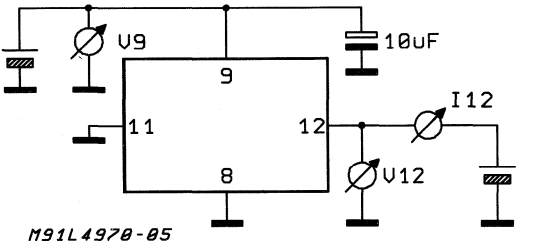


Figure 7D

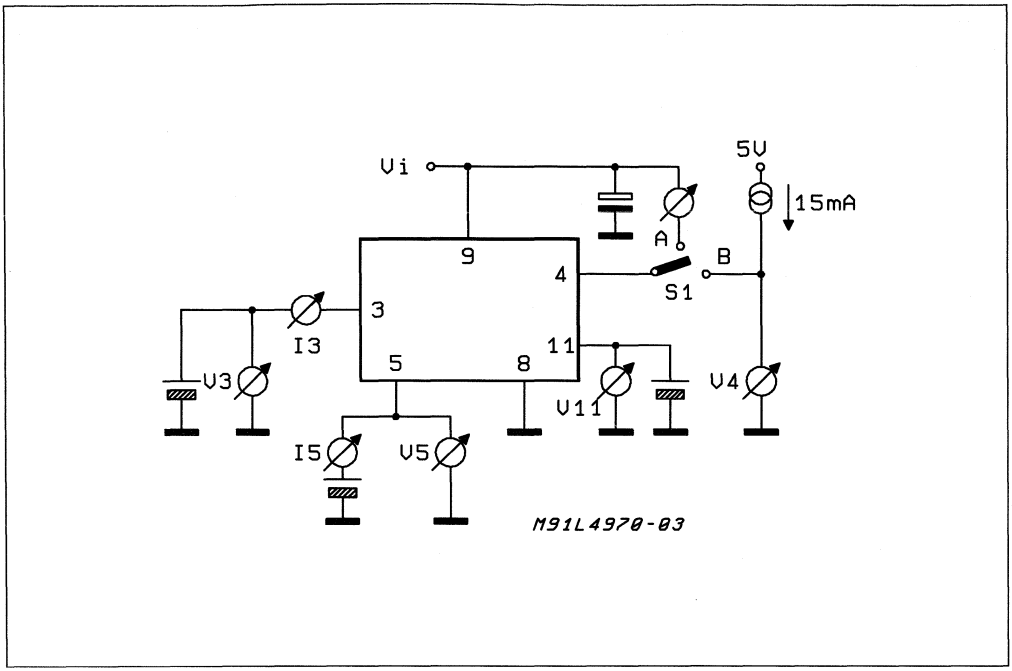


Figure 7C

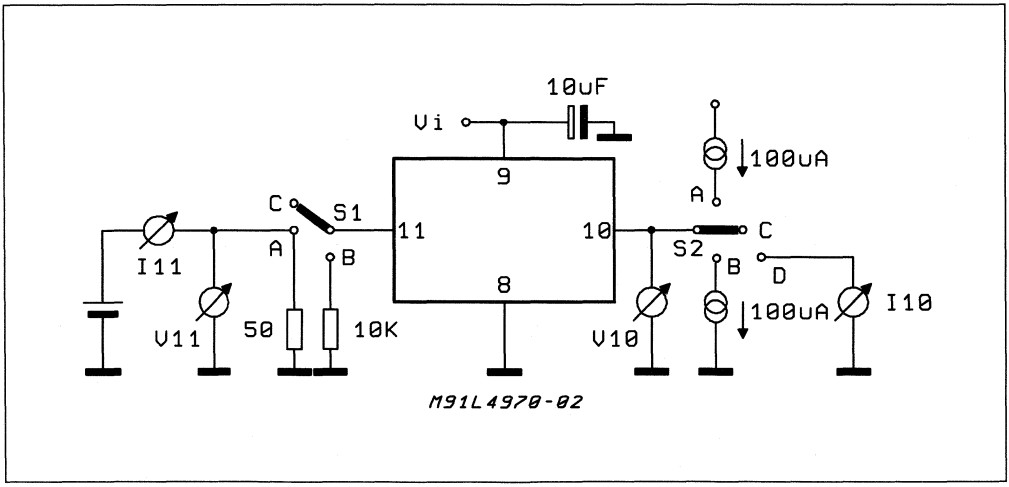


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

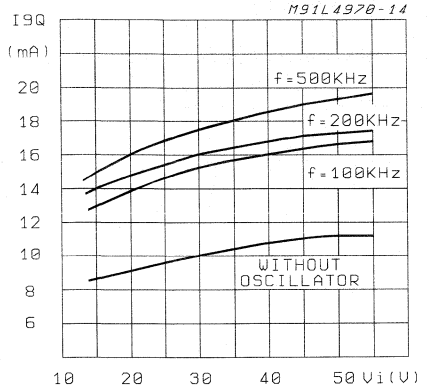


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

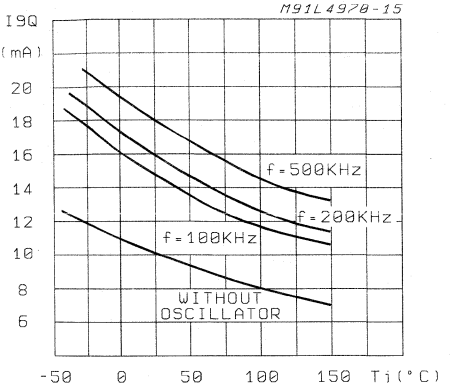


Figure 10: Quiescent Drain Current vs. Duty Cycle

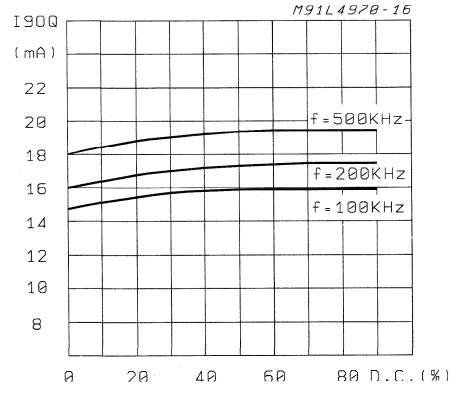


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

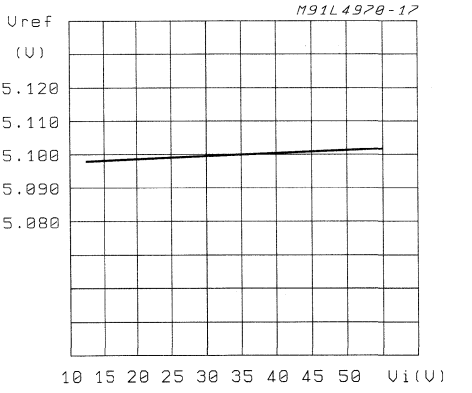


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

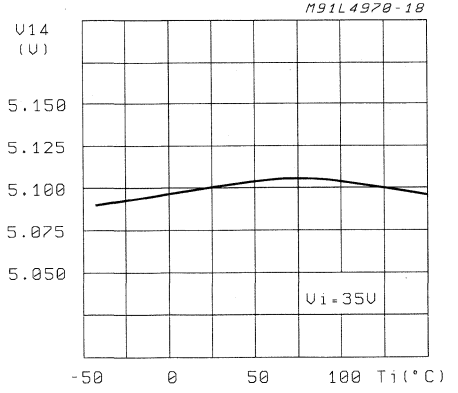


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

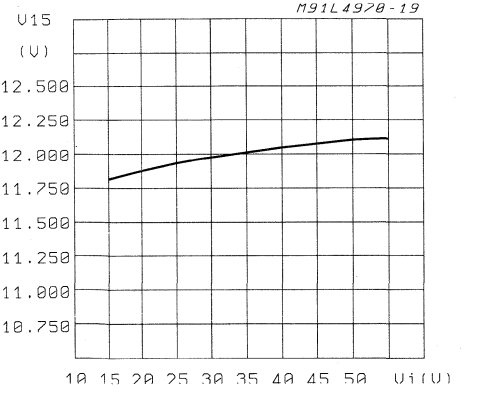


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

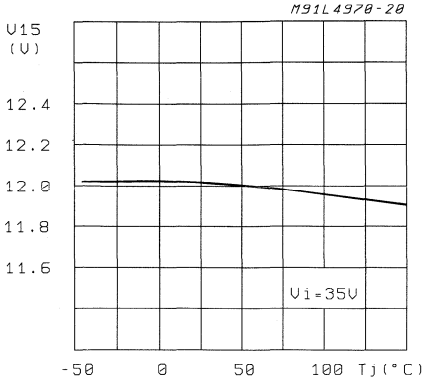


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

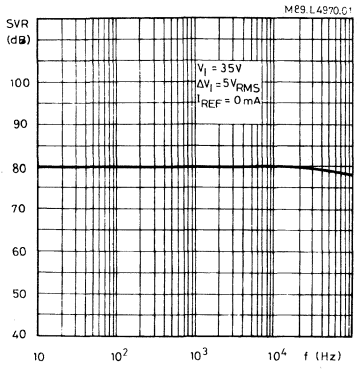


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

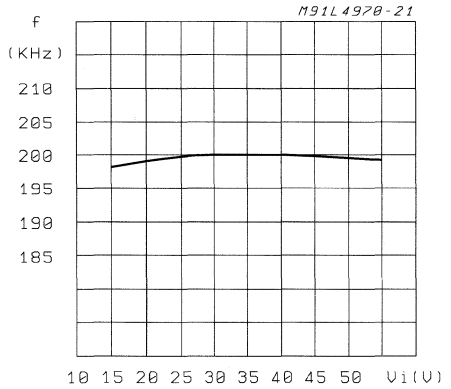


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

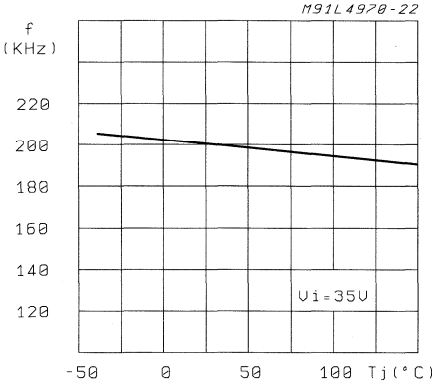


Figure 18: Switching Frequency vs. R4 (see fig. 5)

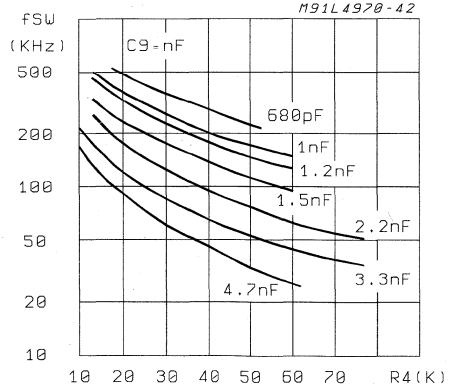


Figure 19: Max. Duty Cycle vs. Frequency

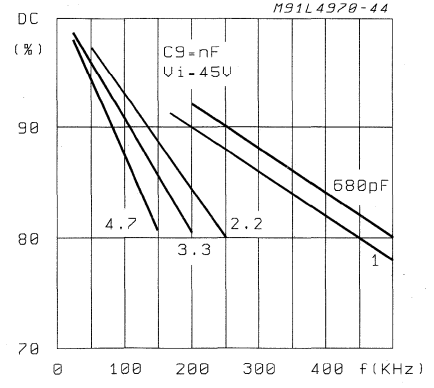


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

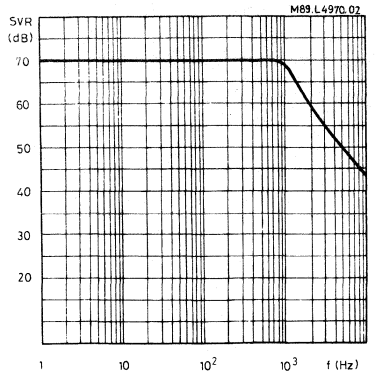


Figure 21: Line Transient Response (see fig. 5)

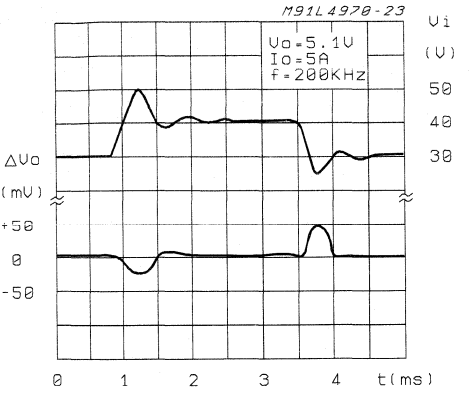


Figure 22: Load Transient Response (see fig. 5)

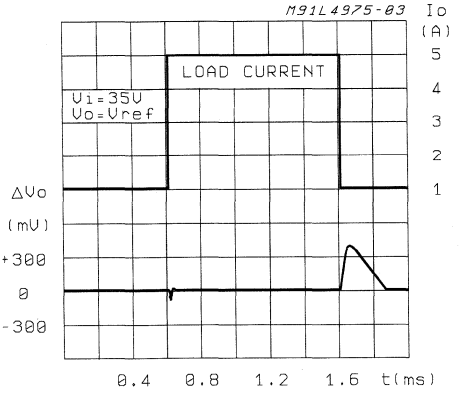


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

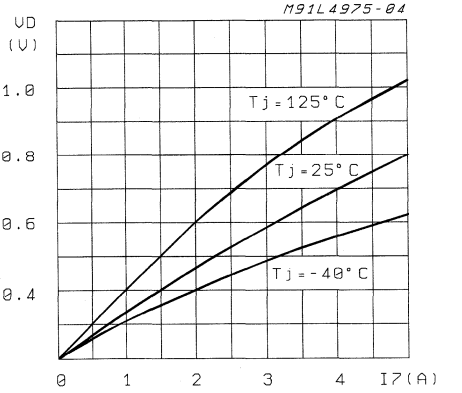


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

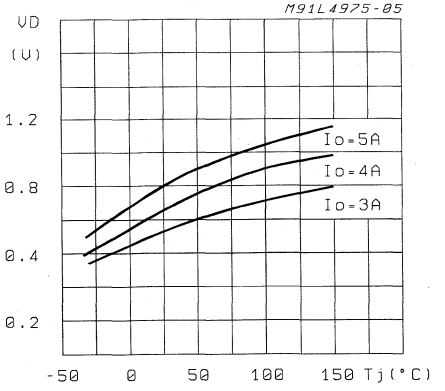


Figure 25: Power Dissipation (device only) vs. Input Voltage

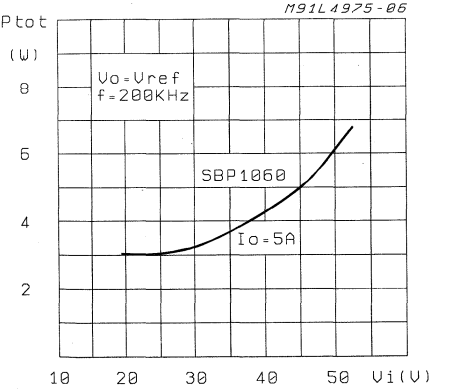


Figure 26: Power Dissipation (device only) vs. Output Voltage

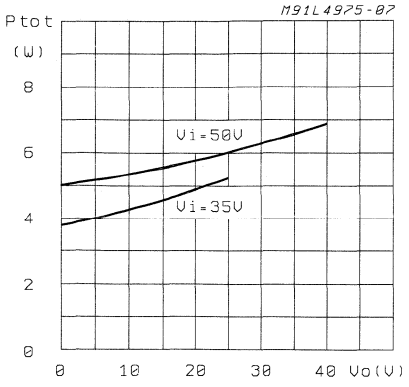


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

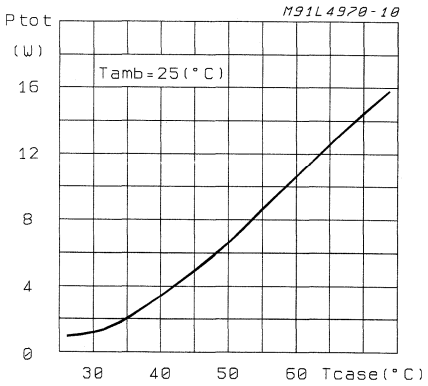


Figure 28: Efficiency vs. Output Current

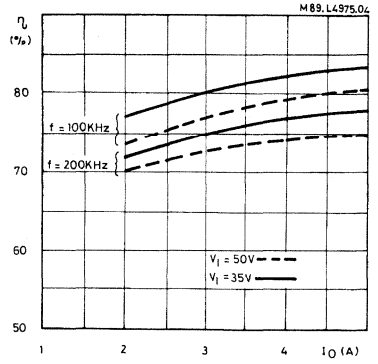


Figure 29: Efficiency vs. Output Voltage

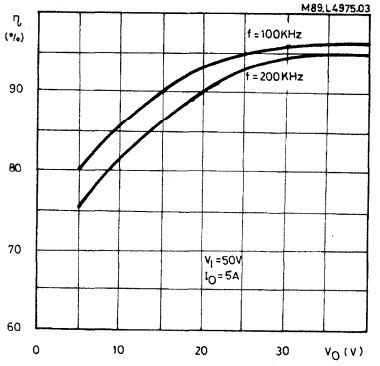


Figure 30: Efficiency vs. Output Voltage

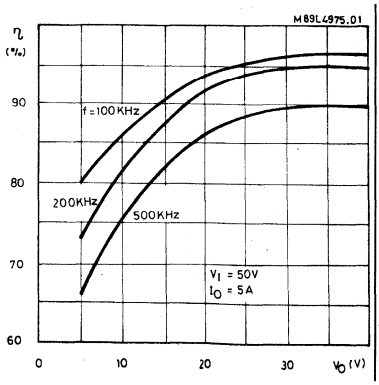


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

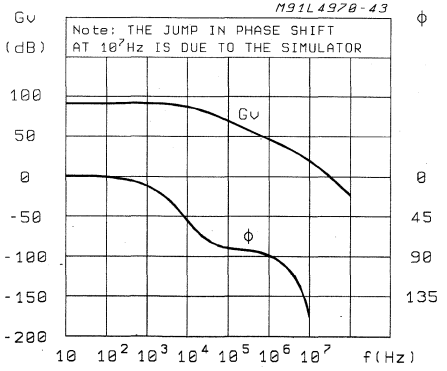


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Figure 32: Power Dissipation Derating Curve

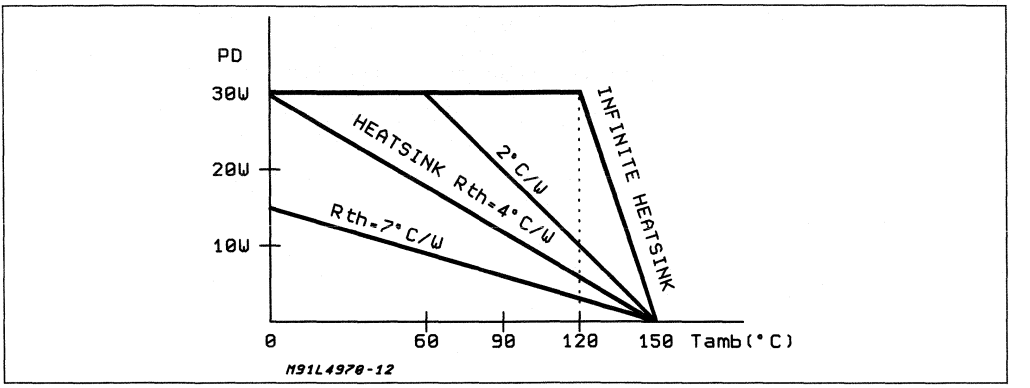


Figure 33: 5.1V/12V Multiple Supply. Note the Synchronization between the L4975A and the L4974A

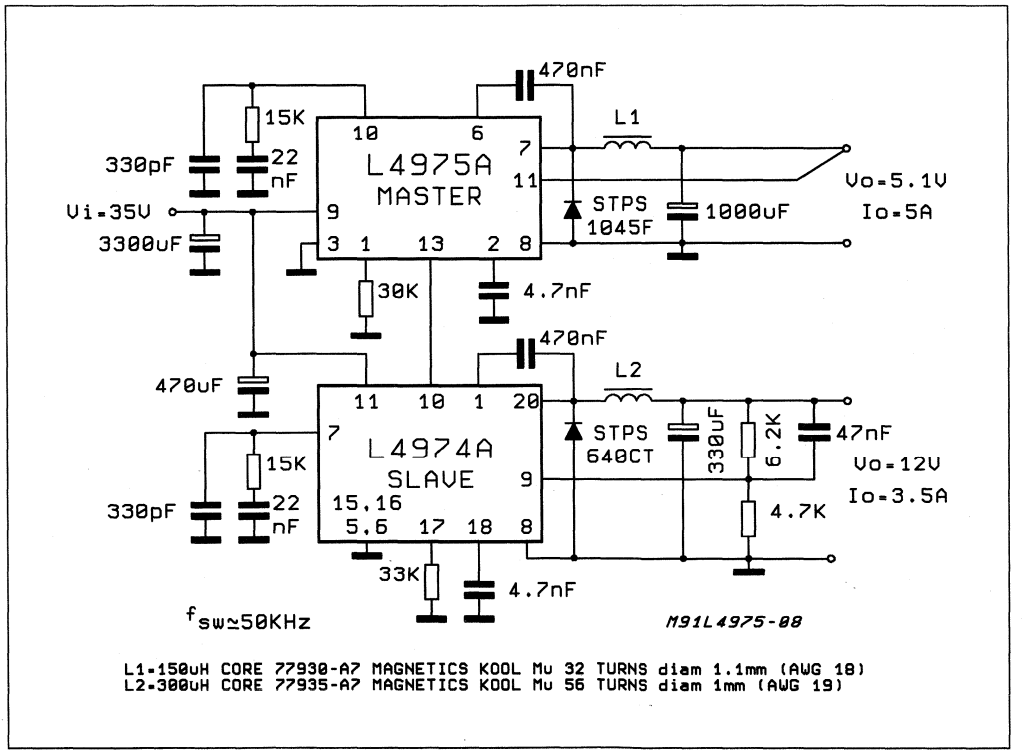


Figure 34: 5.1V / 5A Low Cost Application

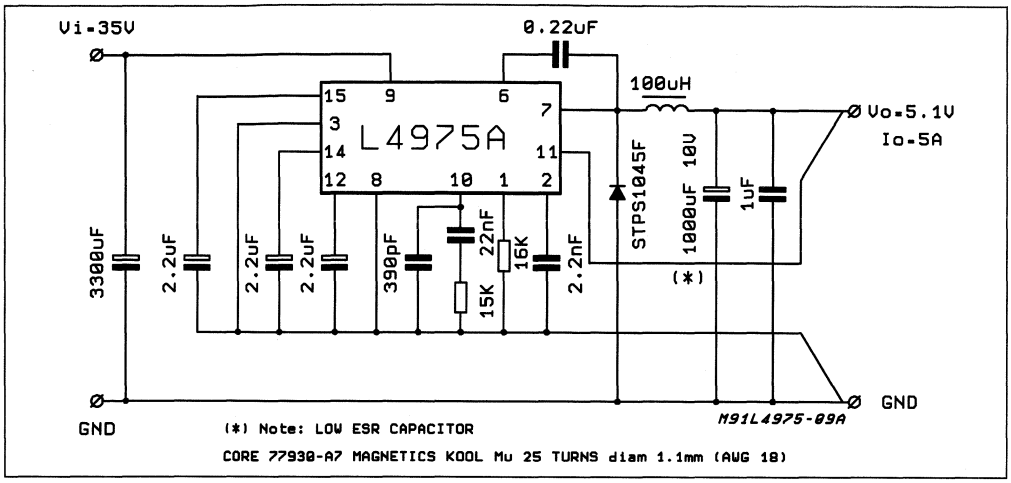


Figure 35: 5A Switching Regulator, Adjustable from 0V to 25V.

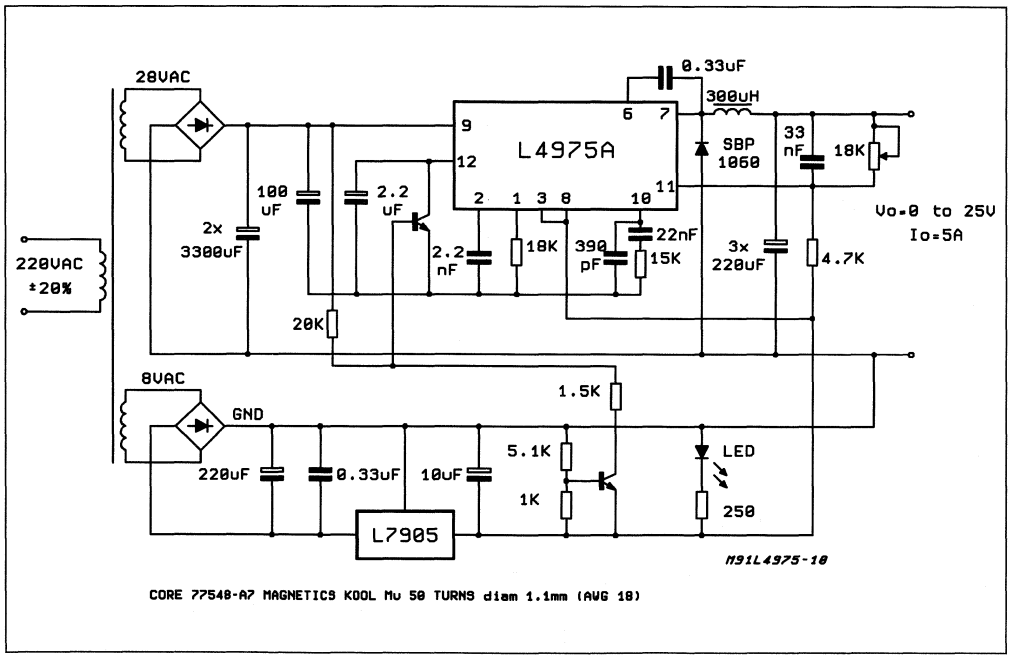
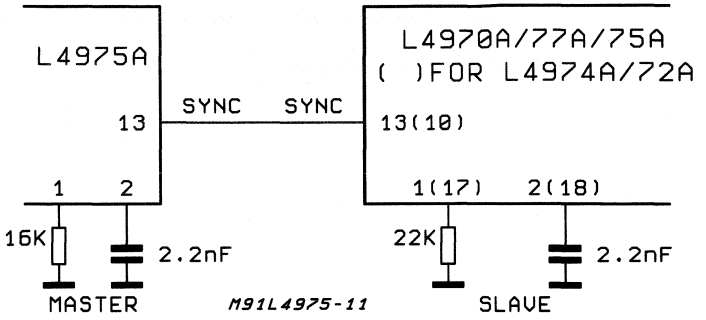


Figure 36: L4975A's Sync. Example



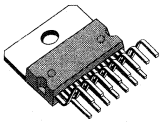
SGS-THOMSON MICROELECTRONICS

L4977A

7A SWITCHING REGULATOR

- 7A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



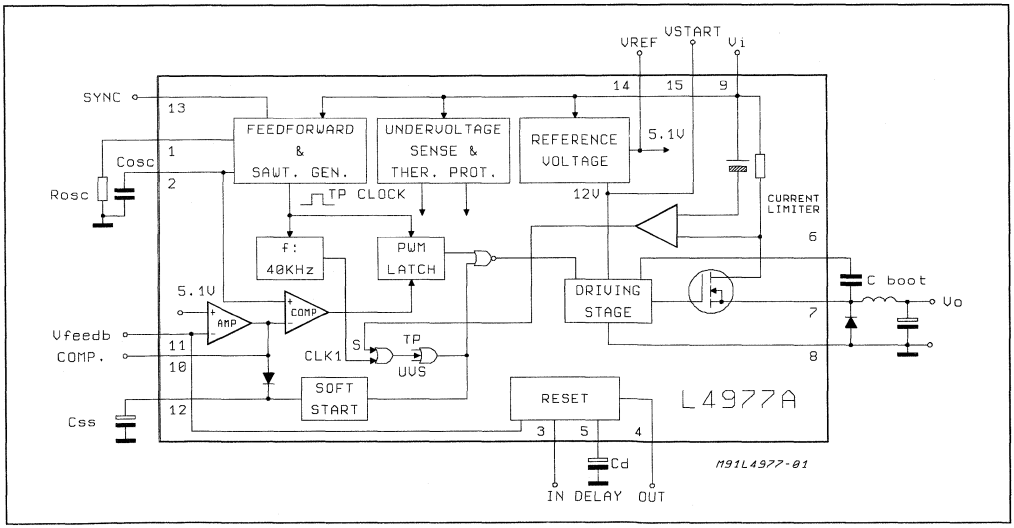
Multiwatt15V
ORDERING NUMBER: L4977A

DESCRIPTION

The L4977A is a stepdown monolithic power switching regulator delivering 7A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4977A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

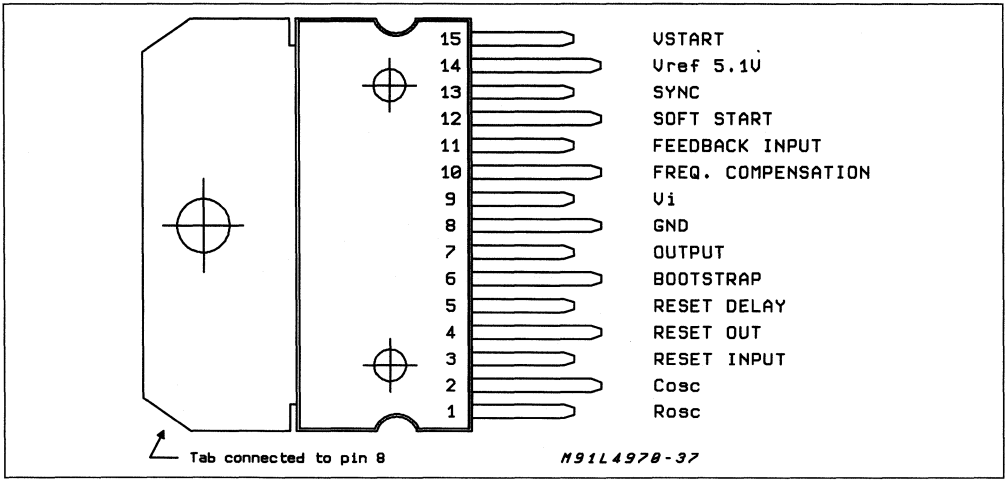
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4977A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4977A is a 7A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 7A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

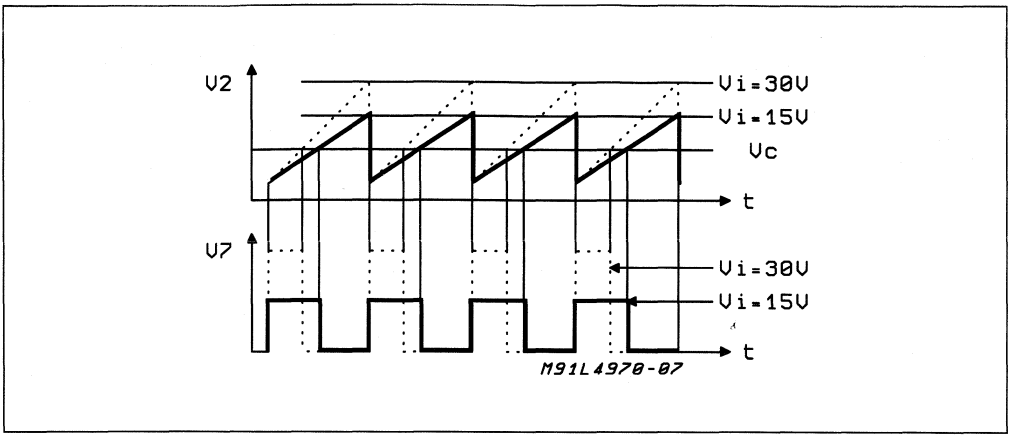


Figure 2: Soft Start Function

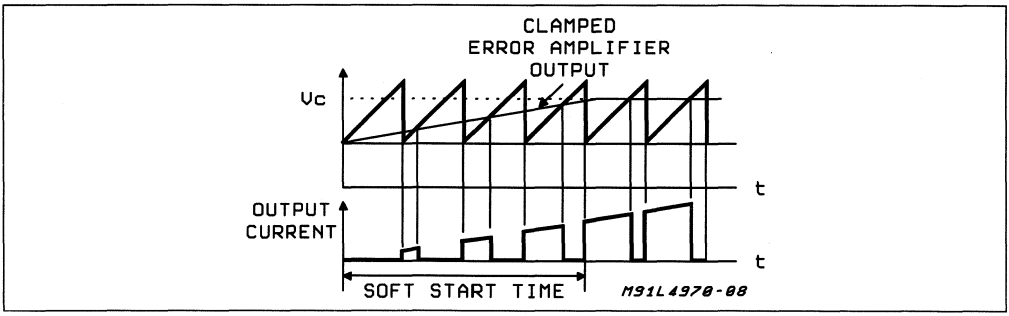
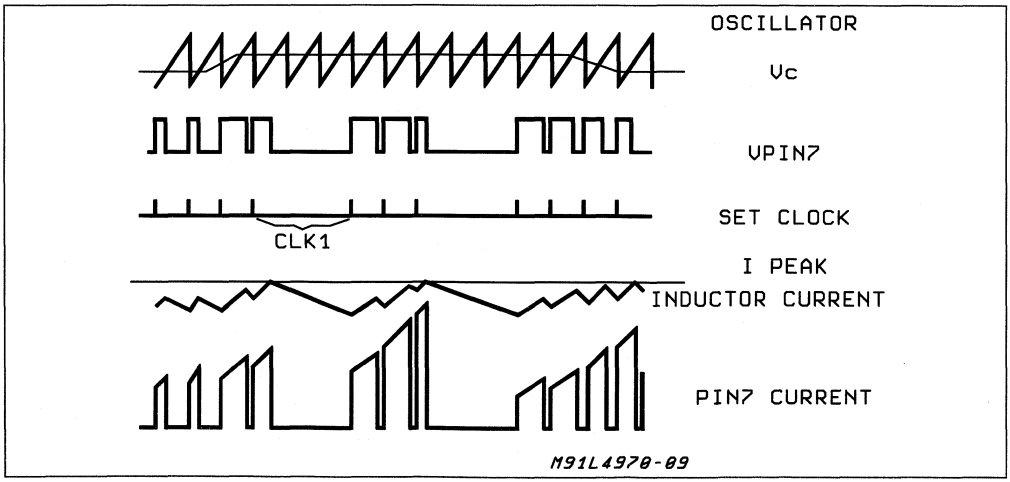


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

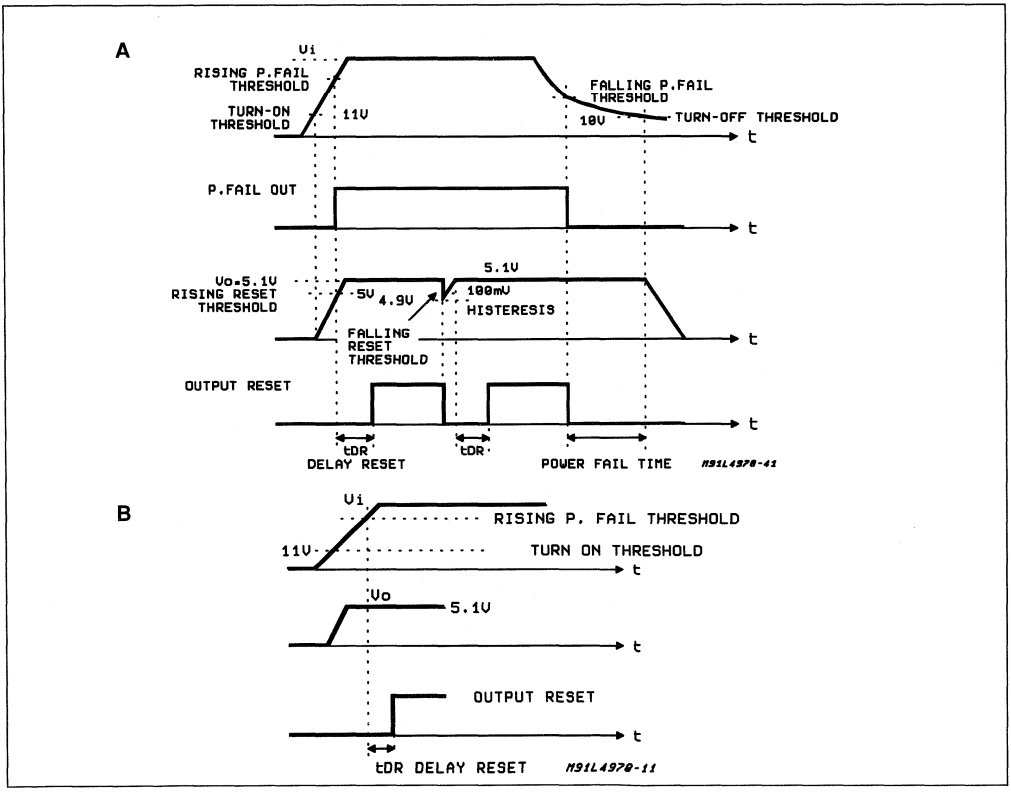
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 7A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 5A I_o = 2A to 7A		 10 20	 25 40	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 7A		0.4 0.8	0.6 1.1	V V	5
I_{7L}	Max. Limiting Current	V_o = V_{ref} to 40V V_i = 15 to 50V	8	9.5	11	A	5
η	Efficiency	I_o = 3A V_o = V_{ref} V_o = 12V	70	75 80		 % %	5
		I_o = 7A V_o = V_{ref} V_o = 12V	75	80 87		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 7A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	V_i = 15V		2.5		V	7A
		S2 = B	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I_1 = 1mA		2.4	2.7		mA	7A

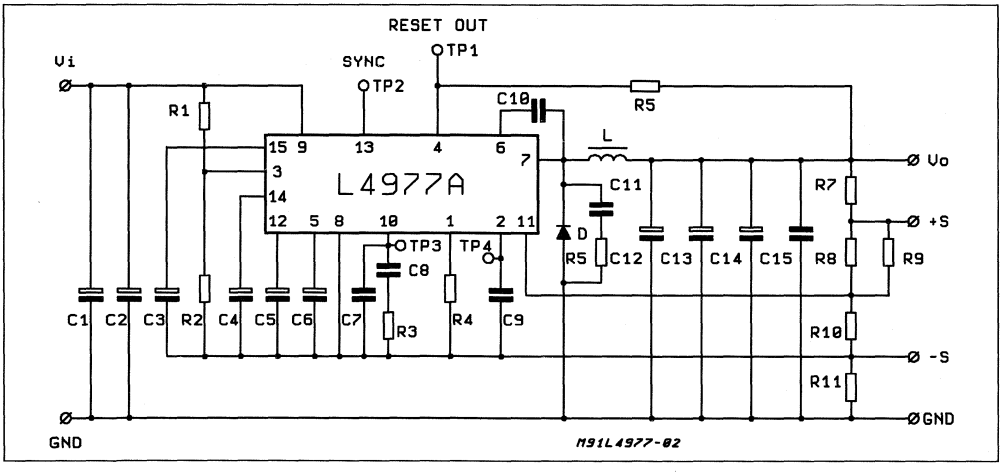
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_{13} = V_2 = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

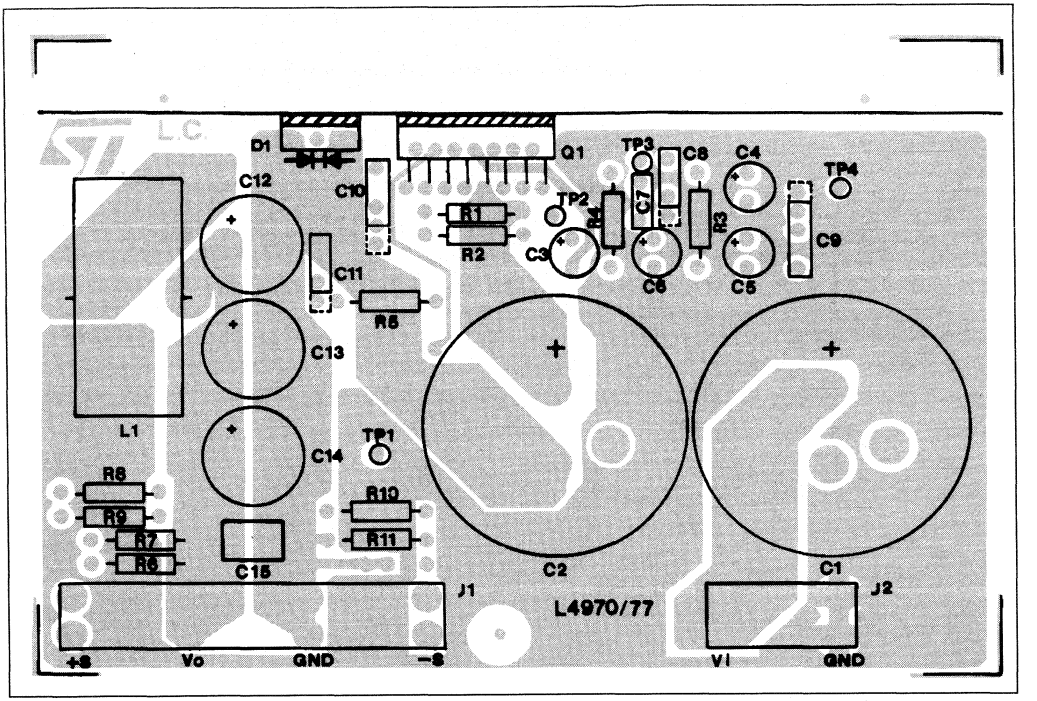
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 7A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 7A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 7A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

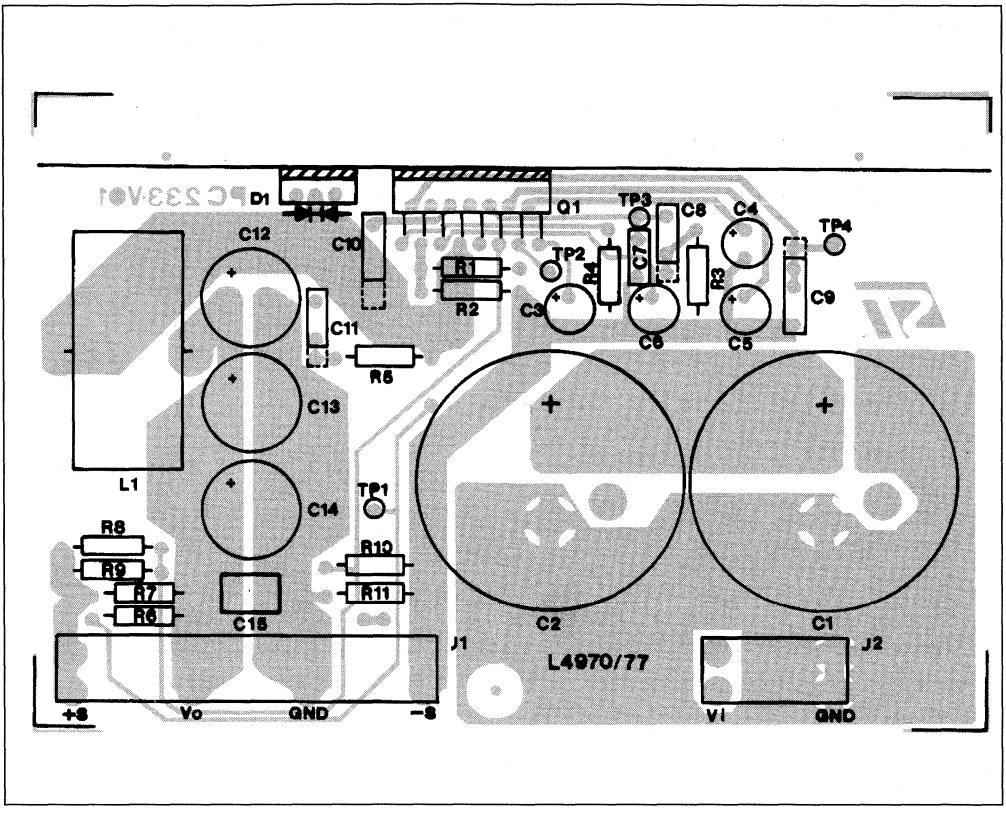


Figure 7: DC Test Circuits

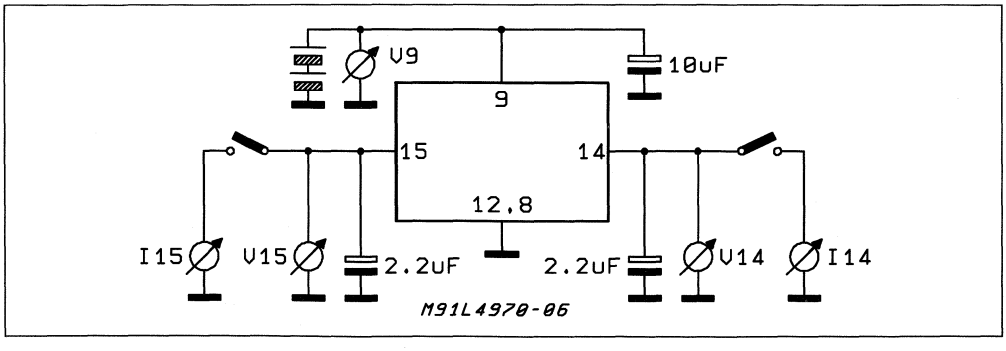


Figure 7A

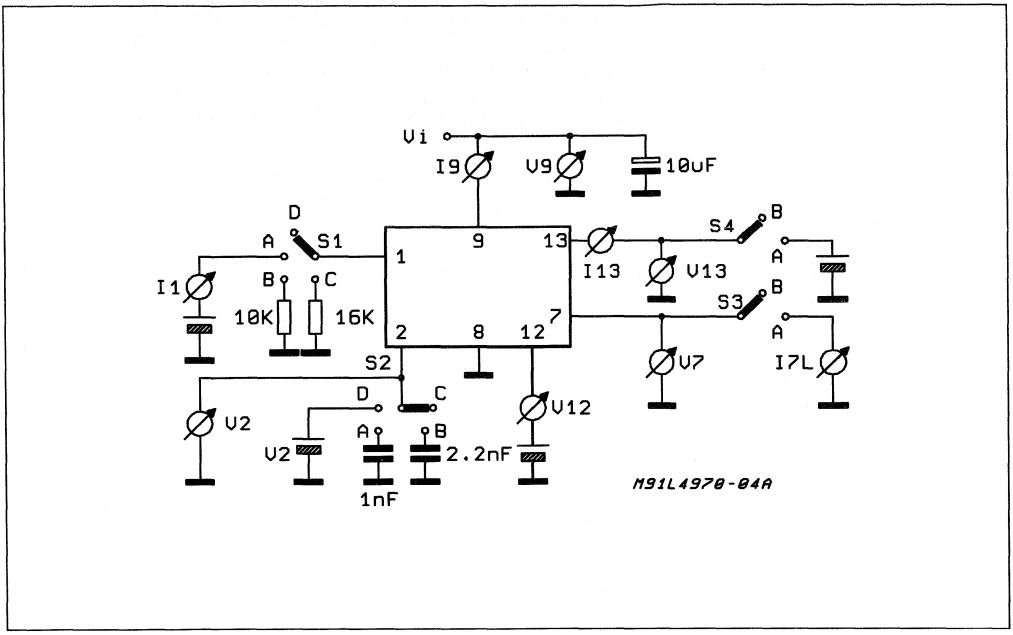


Figure 7B

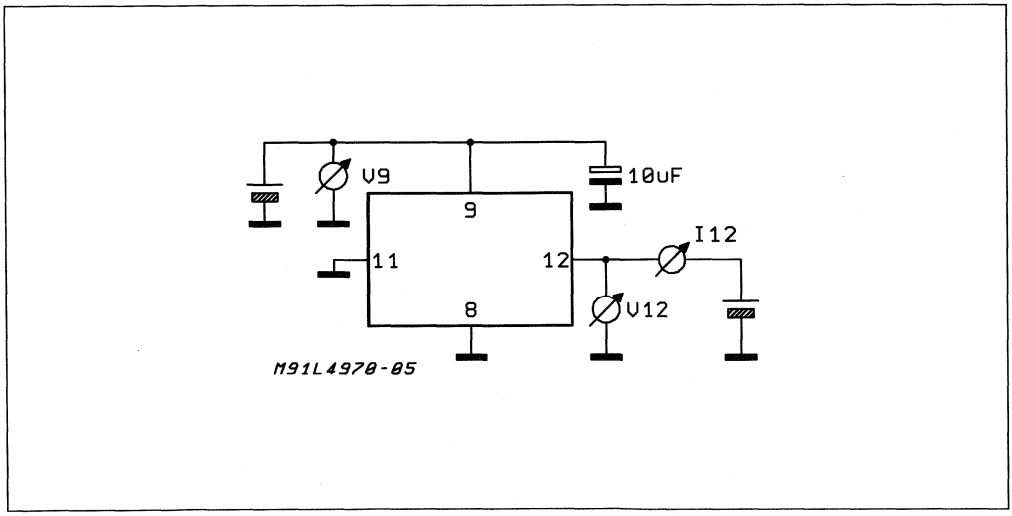


Figure 7D

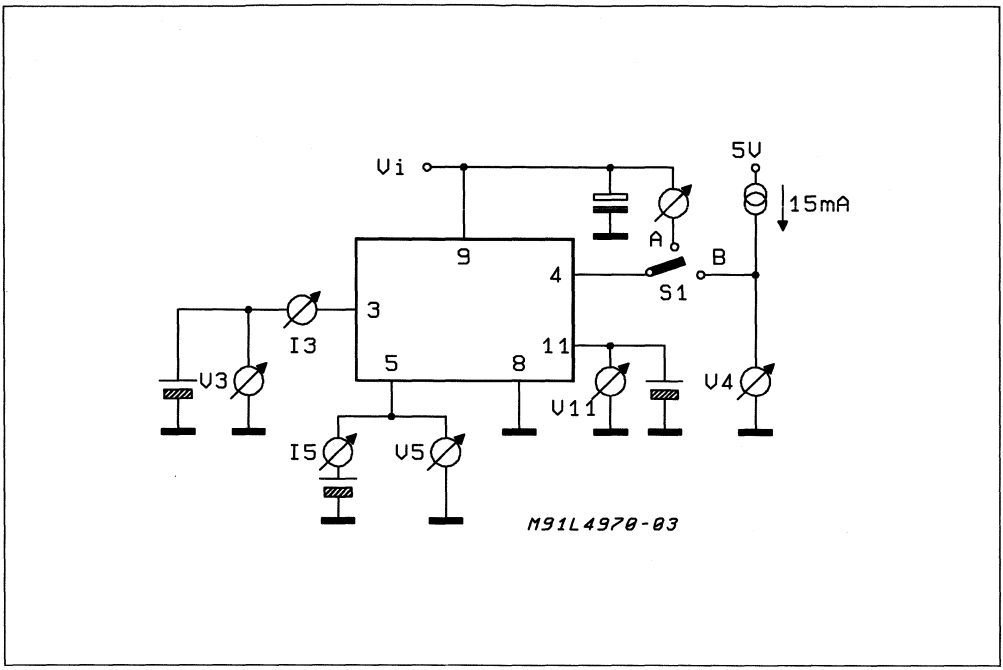
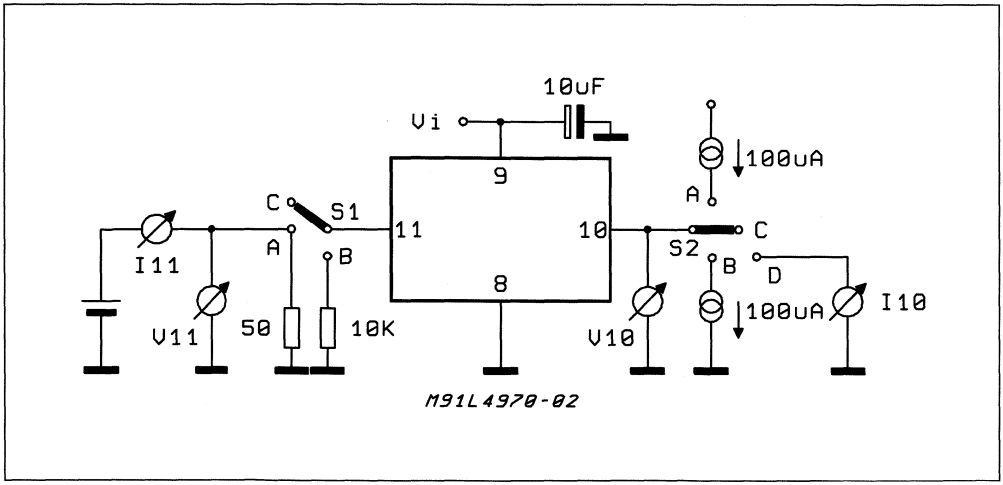


Figure 7C



SGS-THOMSON MICROELECTRONICS

Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

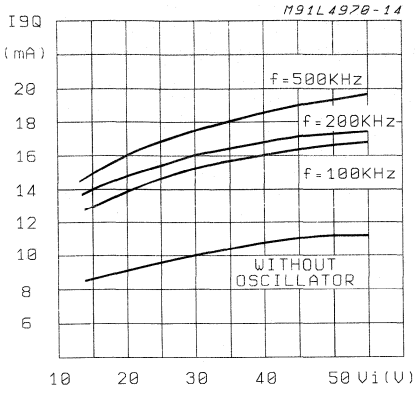


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

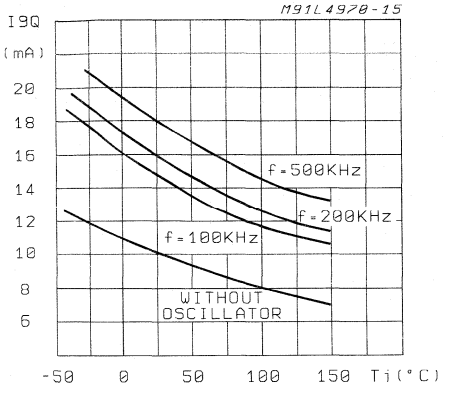


Figure 10: Quiescent Drain Current vs. Duty Cycle

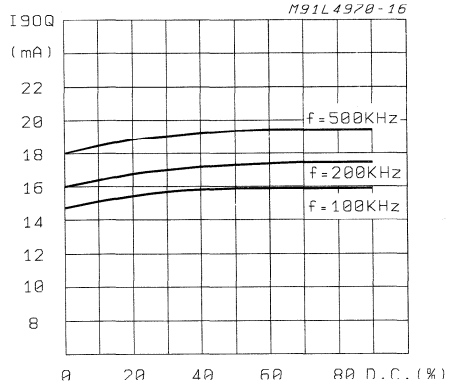


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

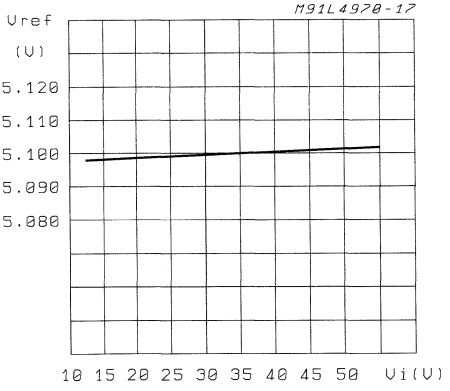


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

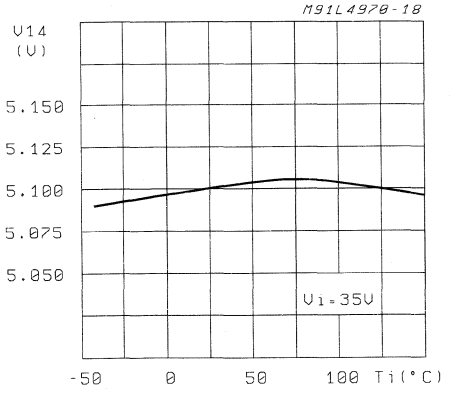


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

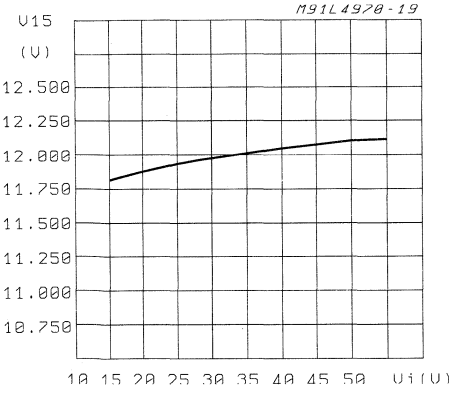


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

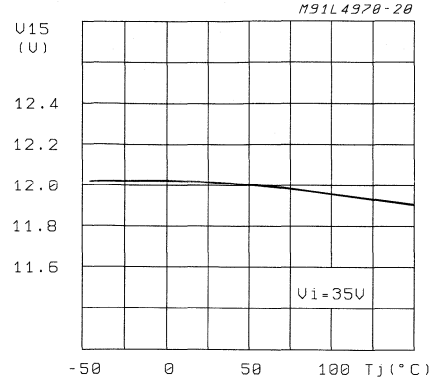


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

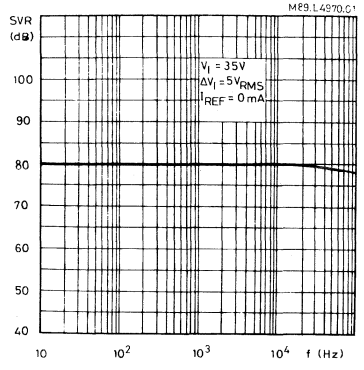


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

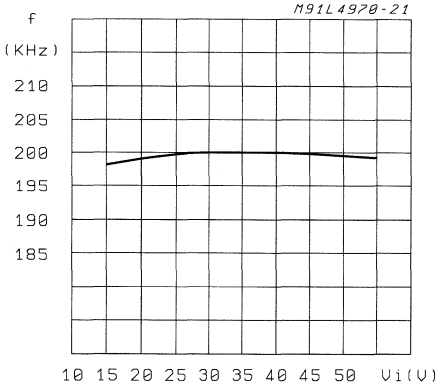


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

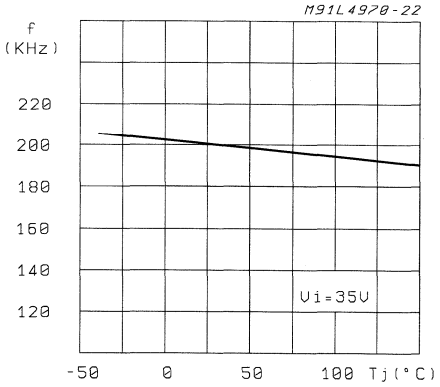


Figure 18: Switching Frequency vs. R4 (see fig. 5)

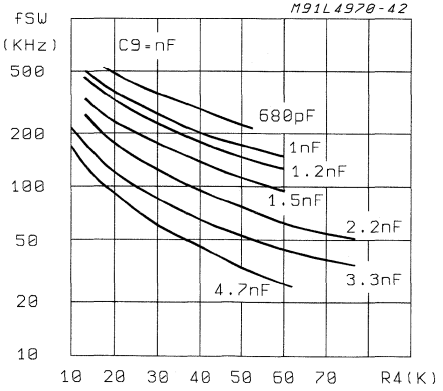


Figure 19: Max. Duty Cycle vs. Frequency

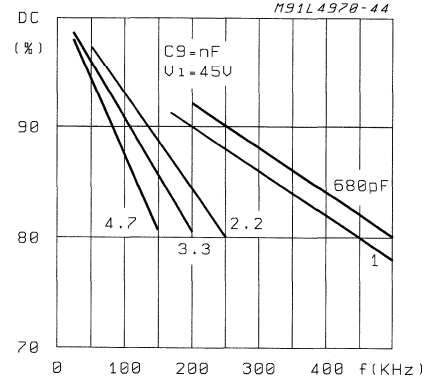


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

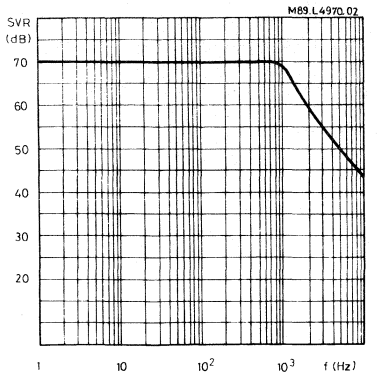


Figure 21: Line Transient Response (see fig. 5)

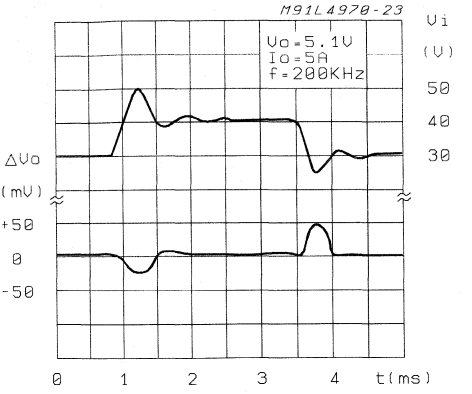


Figure 22: Load Transient Response (see fig. 5)

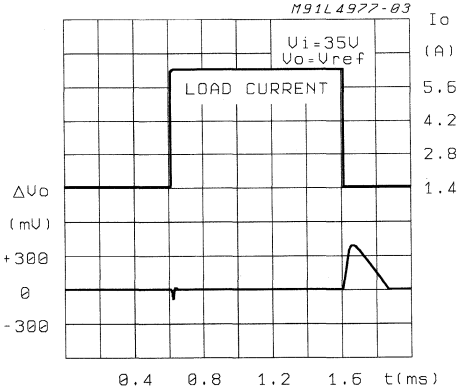


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

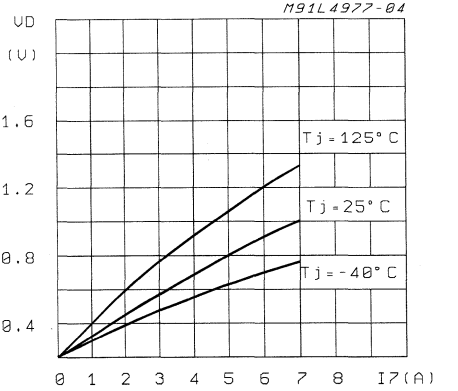


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

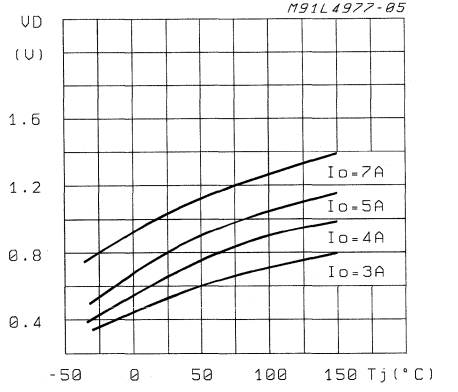


Figure 25: Power Dissipation (device only) vs. Input Voltage

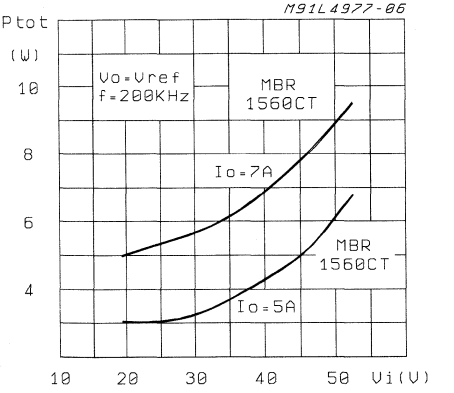


Figure 26: Power Dissipation (device only) vs. Output Voltage

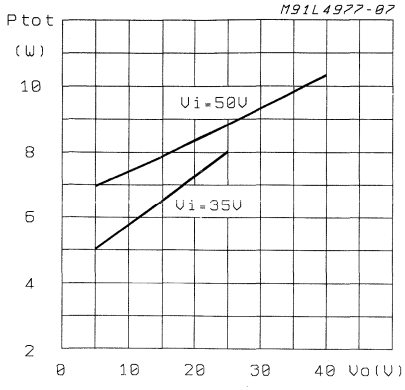


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

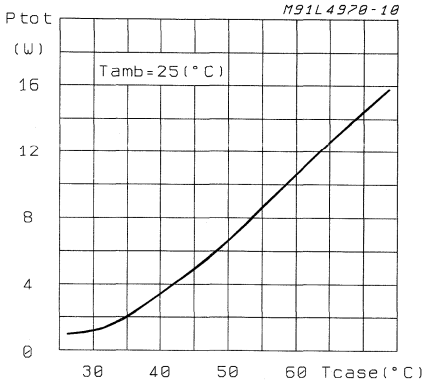


Figure 28: Efficiency vs. Output Current

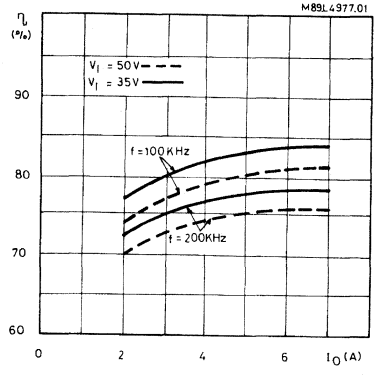


Figure 29: Efficiency vs. Output Voltage

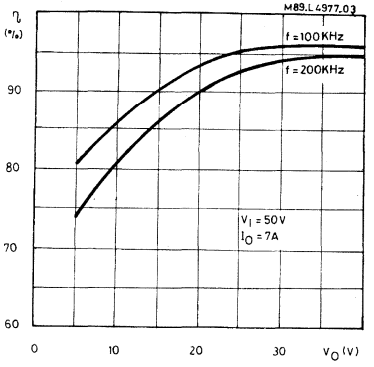


Figure 30: Efficiency vs. Output Voltage

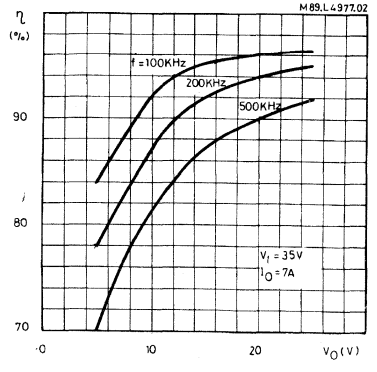


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

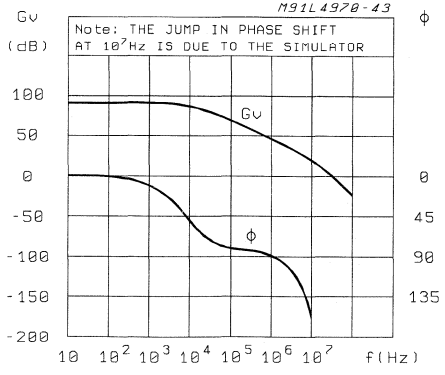


Figure 32: Power Dissipation Derating Curve

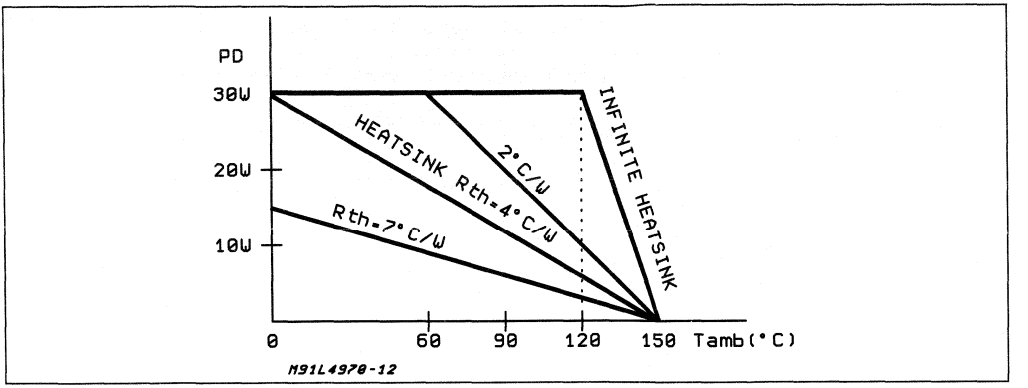


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4977A and the L4974A

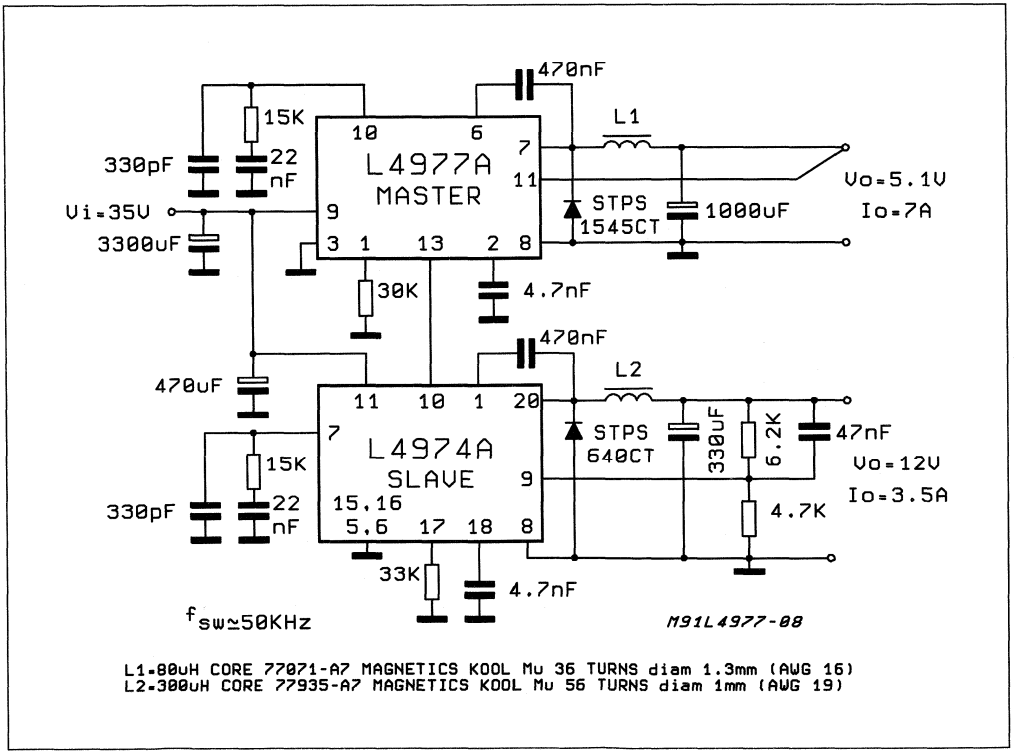


Figure 34: 5.1V / 7A Low Cost Application

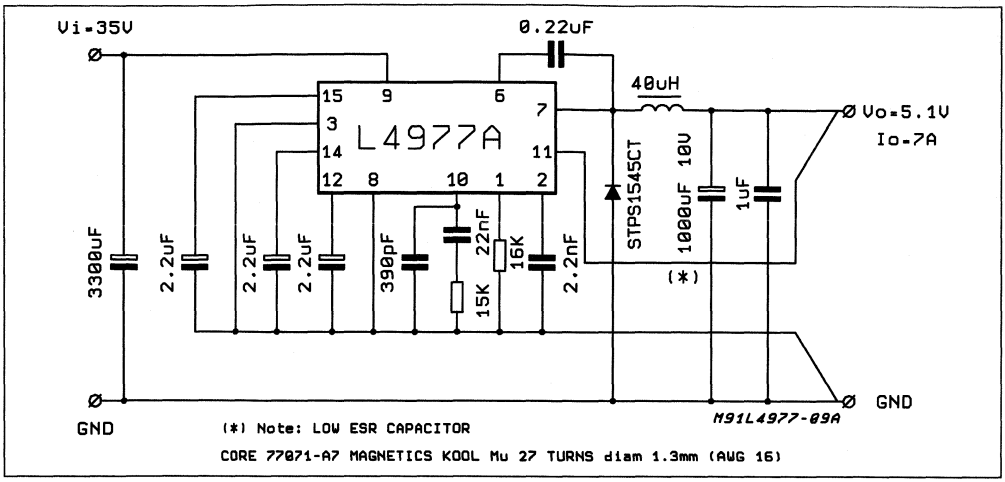


Figure 35: 7A Switching Regulator, Adjustable from 0V to 25V.

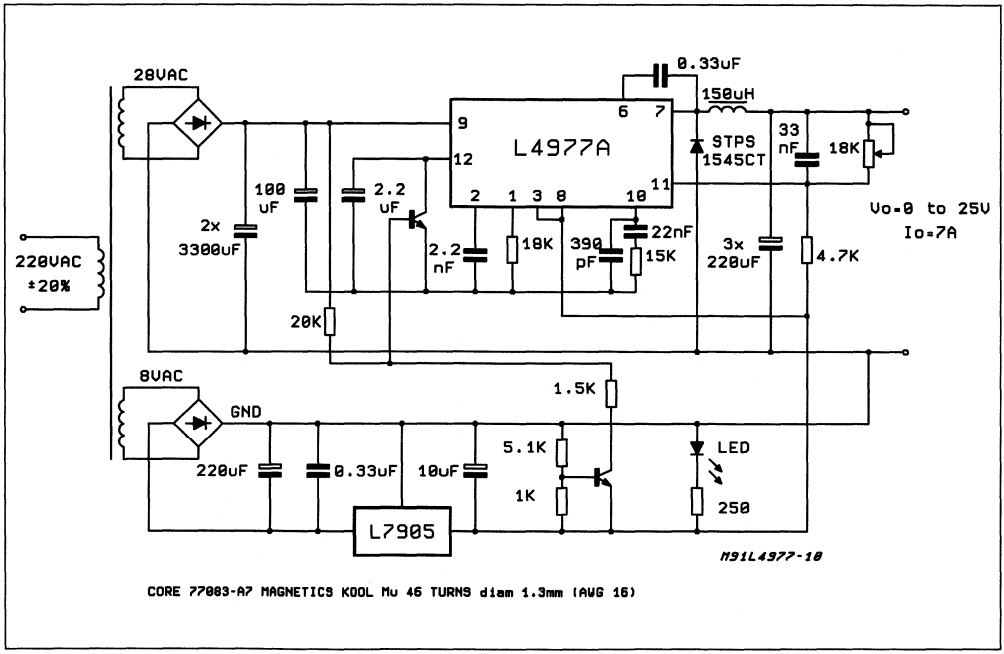
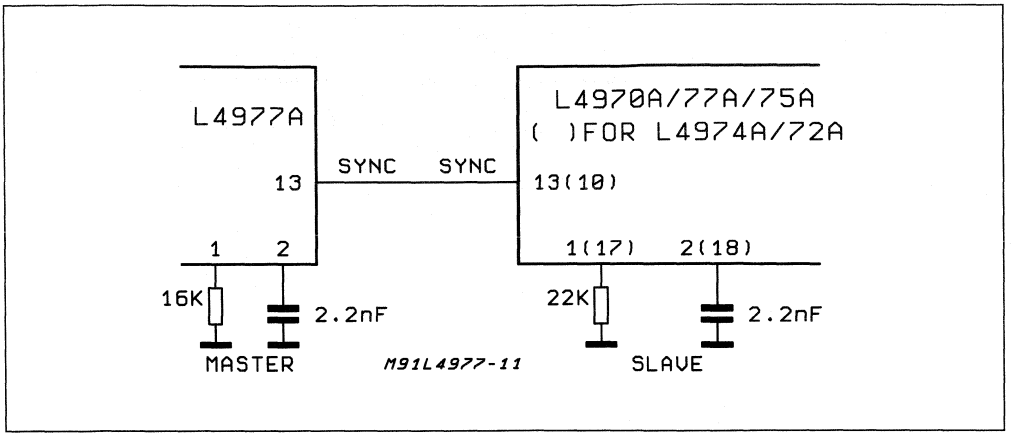


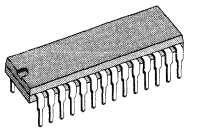
Figure 36: L4977A's Sync. Example

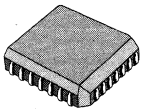


OCTAL LINE DRIVER

ADVANCE DATA

- OCTAL LINE DRIVER FOR:
  - EIA STD: RS232D; RS423A
  - CCIT: V.10; V.28
- NO EXTERNAL COMPONENTS
- OUTPUT FAIL SAFING CAPABILITY
- VERY LONG TRANSMISSION LINE (500Oft)
- 50V EOS OUTPUT PROTECTION





DIP28 **PLCC28**

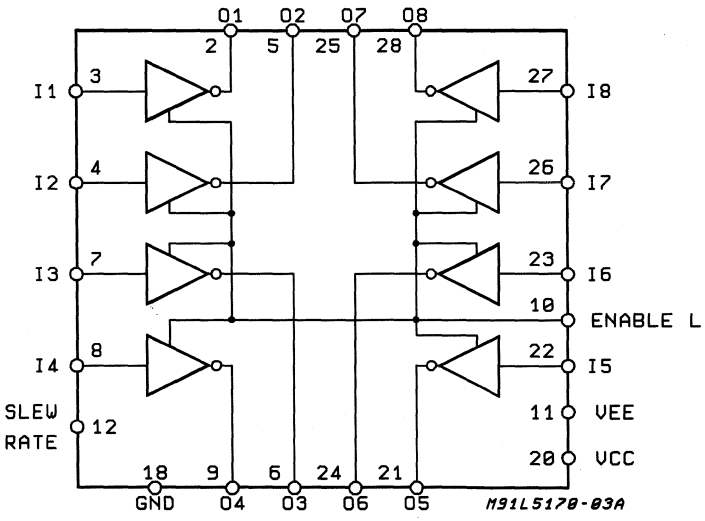
ORDERING NUMBERS:

L5170A L5170D

DESCRIPTION

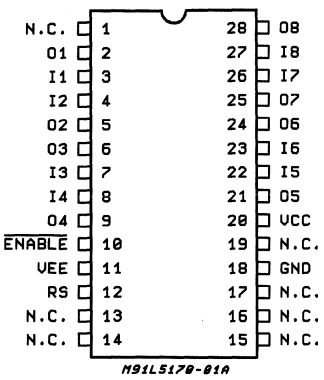
L5170 is an octal line driver unit in DIP28 and PLCC28 packages intended for use in the EIA std RS232D, RS423A and CCITT V.10 and V.28 applications.
With no external components L5170 is able to drive a line up to 5000ft assuming the capacitance is 35pF per ft and filter connectors/protection components add to the total capacitance load. The drivers typically run in short circuit current mode whenever the cable attached is over 500ft.

BLOCK DIAGRAM

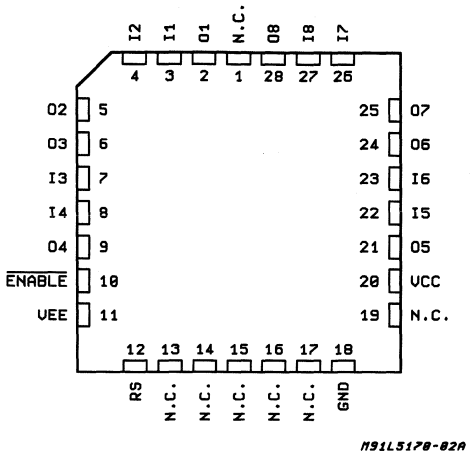


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS (Top views)



DIP28



PLCC28

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+15	V
V_{EE}	Supply Voltage	– 15	V
V_i	Input Voltage (Enable Data)	– 1.5 to 7	V
V_O	Output Voltage	±6	V
I_O	Output Current (**)	±150	mA
SR	Minimum Slew Resistor (***)	1.5	1KΩ
P_{tot}	Power Dissipation at T_{amb} = 70°C **(PLCC28)** (*) **(DIP28)** (*)	1.2 1.3	W W
T_{op}	Operating Free Air Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C

Notes:
(*) Mounted on board with minimized dissipating copper area.
(**) Minimum Current per driver. Do not exceed maximum power dissipation if more than one input is on.
(***) Minimum value of the resistor used to set the slew rate.

THERMAL DATA

Symbol	Description		PLCC28	DIP28	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max.	67	62	°C/W

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9 to 11V; V_{EE} = – 9 to – 11V T_{amb} =0 to 70°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OH}	High	V_{in} = 8V R_L = inf R_L = 3KΩ R_L = 450Ω (see note 1)	 5 5 4.5		 6 6 6	 V V V
V_{OL}	Low Level Outpu Voltage	V_{in} = 2.4V R_L = inf R_L = 3KΩ R_L = 450Ω (see note 1)	 – 6 – 6 – 6		 – 5 – 5 – 4.5	 V V V
V_{OI}	Output Voltage Balance	$\|V_{CC}\| = \|V_{EE}\|$; R_L = 450Ω			0.4	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IK}	Input Clamp Voltage	I_{IN} = – 15mA	– 1.5			V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	– 400			µA
I_{CC}	Positive Supply Current	V_{IN} = 2.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)			30	mA
I_{CC1}	Positive Supply Current	V_{IN} = 0.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)			40	mA
I_{EE}	Negative Supply Current	V_{IN} = 2.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)	– 30			mA
I_{EE1}	Negative Supply Current	V_{IN} = 0.4V; R_S = 2KΩ; R_L = 3KΩ C_L = 2.5nF; (See note 2)	– 40			mA
I_{sh}	Output Short Circuit Current	V_O = 0V; V_{IN} = 2.4V; (see fig.1)	25		100	mA
I_{sl}	Output Short Circuit Current	V_O = 0V; V_{IN} = 2.4V; (see fig.1)	– 100		– 25	mA
I_{bal}	Output Current Balance	Ish/Isl = Ibal	0.625		1.6	mA/mA
I_x	Output Leakage Current	See fig.2,3 and note 3 V_O = 6V V_O = – 6V	 – 70		 70	 µA µA
t_r	Rise time (see note 4 and 5; see figure 4A)	R_L = 450Ω; C_L = 50pF R_{slew} = 5.34KΩ ±1%	2		2.7	µs
t_{rc1}		R_L = 450Ω; C_L = 0.01µF R_{slew} = 10KΩ ±1%			10	µs
t_{rc2}		R_L = 450Ω; C_L = 0.1µF R_{slew} = 10KΩ ±1%			50	µs
t_{rc3}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 2KΩ ±1%	0.65		1.2	µs
t_{rc4}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 10KΩ ±1%	3.25		6	µs
t_f	Fall time (see note 4 and 5; see figure 4A)	R_L = 450Ω; C_L = 50pF R_{slew} = 5.34KΩ ±1%	2		2.7	µs
t_{fc1}		R_L = 450Ω; C_L = 0.01µF R_{slew} = 10KΩ ±1%			10	µs
t_{fc2}		R_L = 450Ω; C_L = 0.1µF R_{slew} = 10KΩ ±1%			50	µs
t_{fc3}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 2KΩ ±1%	0.65		1.2	µs
t_{fc4}		R_L = 450Ω; C_L = 2.5nF R_{slew} = 10KΩ ±1%	3.25		6	µs

Note 1: The Output under load must not drop below 90% of the open circuit drive level.

Note 2: This represents the static condition only. Applications can see 130mA normal current draw for clock and data lines with up to 500mA transients when all lines are transitioning at the same time. Over 500ft of cable slew rate is governed by the drivers ability to sink current. The currents are rougly equivalent to the short circuit current.

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{lz}	Output Enable to Output (see figure 4B)	R_L = 450Ω; C_L = 50pF R_{slew} = 10KΩ			5	µs
t_{nz}					5	µs
t_{zl}					150	µs
t_{zh}					150	µs
t_{plh}	Propagation (see figure 4C)	RL = 450Ω; C_L = 50pF R_{slew} = 2KΩ	0.3		0.9	µs
t_{ph1}			0.3		0.9	µs

LINE TRANSIENT IMMUNITY (Considering the following cases: Powered ON, Powered OFF-Low impedance power supply and Powered OFF-High impedance supply).

ESD	Elettrostatic Discharge	Tested per MIL-STD-883 (see note 6)	2			KV
EOS	Electrical Overstress	Transient pulse both polarities for 100µs (see note 7)	50			V

Note 3: The output leakage is measured under the following conditions:
a) The Driver tristated
b) Power supply OFF, and the power pins shorted to Ground
c) Power supply OFF. Impedances between power pins open and power pins shorted to Ground.

Note 4: The output waveform should not show any signs of oscillations under any load variation between o.1VVss and 0.9Vss. The oscillation allowed when V_{SS} < 0.1V_{SS} and V_{ss} >0.9V_{ss} shall be 10% of V_{ss}.

Note 5: t_{fc1} thru t_{rc4} shall be within ±20% of t_{rc1} thru t_{rc4} respectively.

Note 6: All pins are required to withstand parameter.

Note 7: Output pins are required to withstand fig.5 without any degradation to the circuit.

TEST CIRCUIT

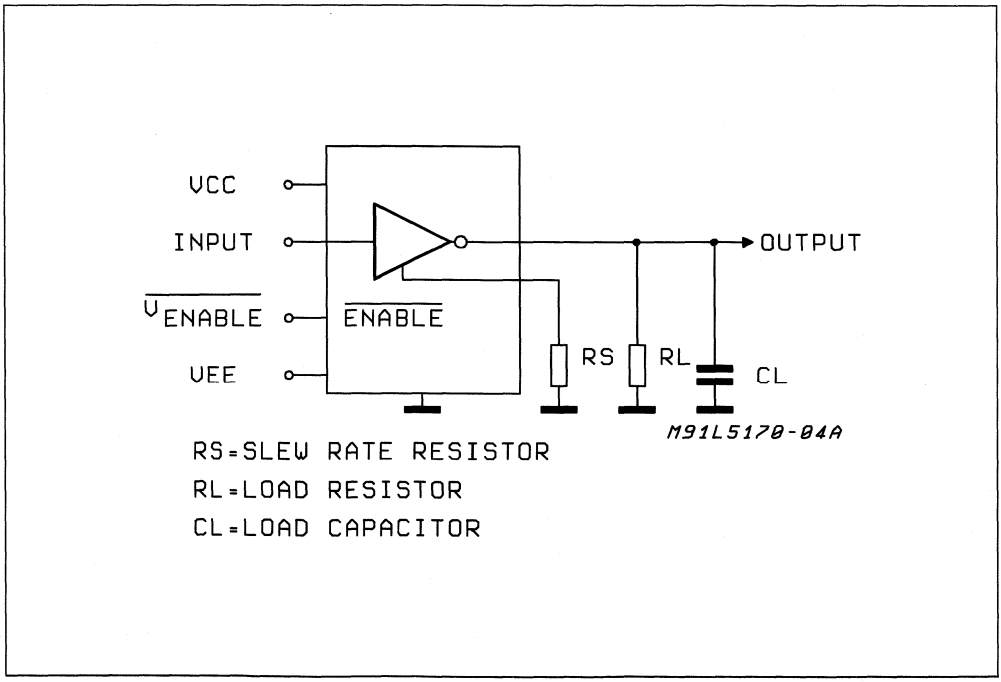


Figure 1: Typical Short Circuit Current

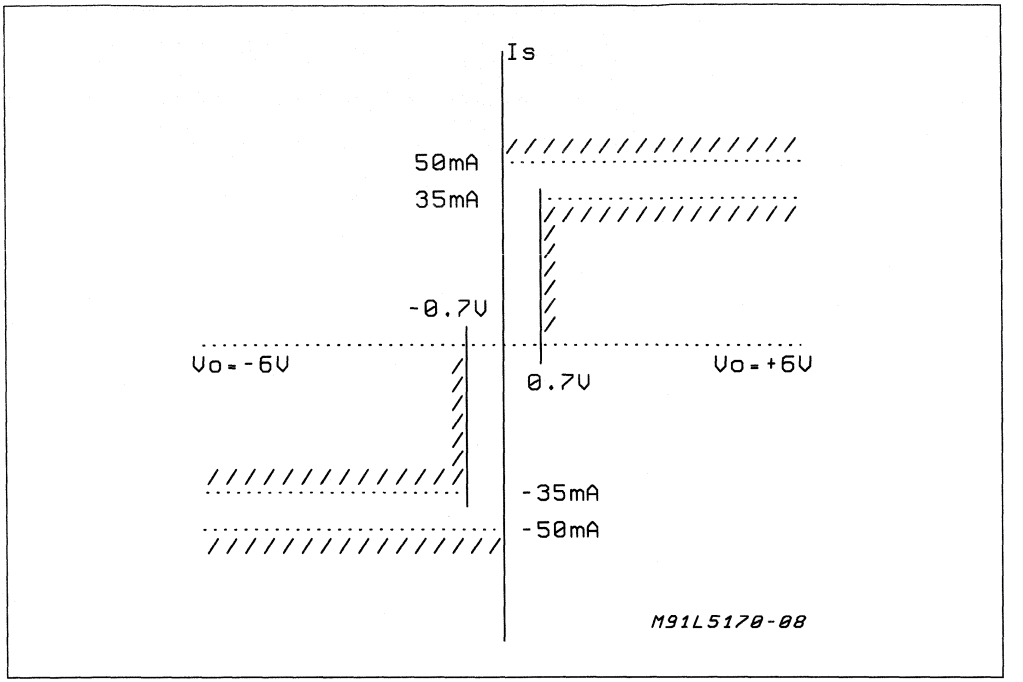


Figure 2: Output Leakage Test Circuit

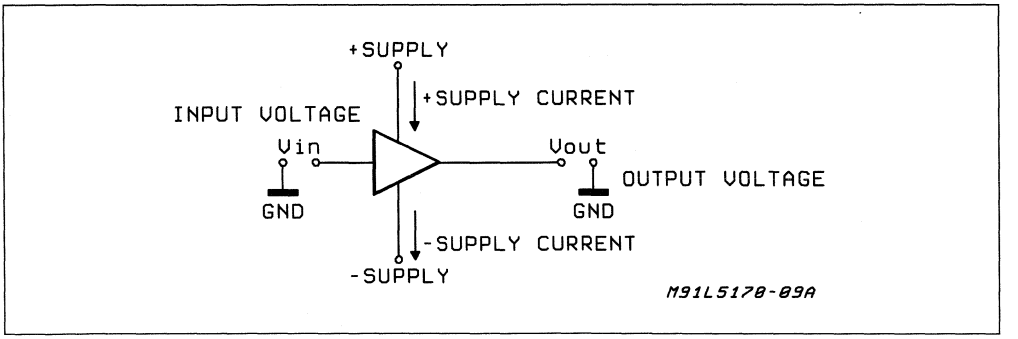


Figure 3: Output Voltage Rise Time

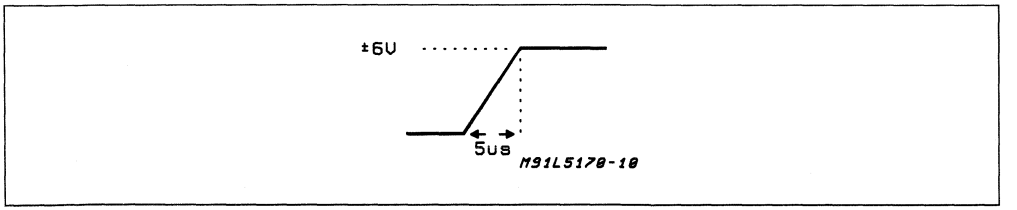


Figure 4: Waveforms

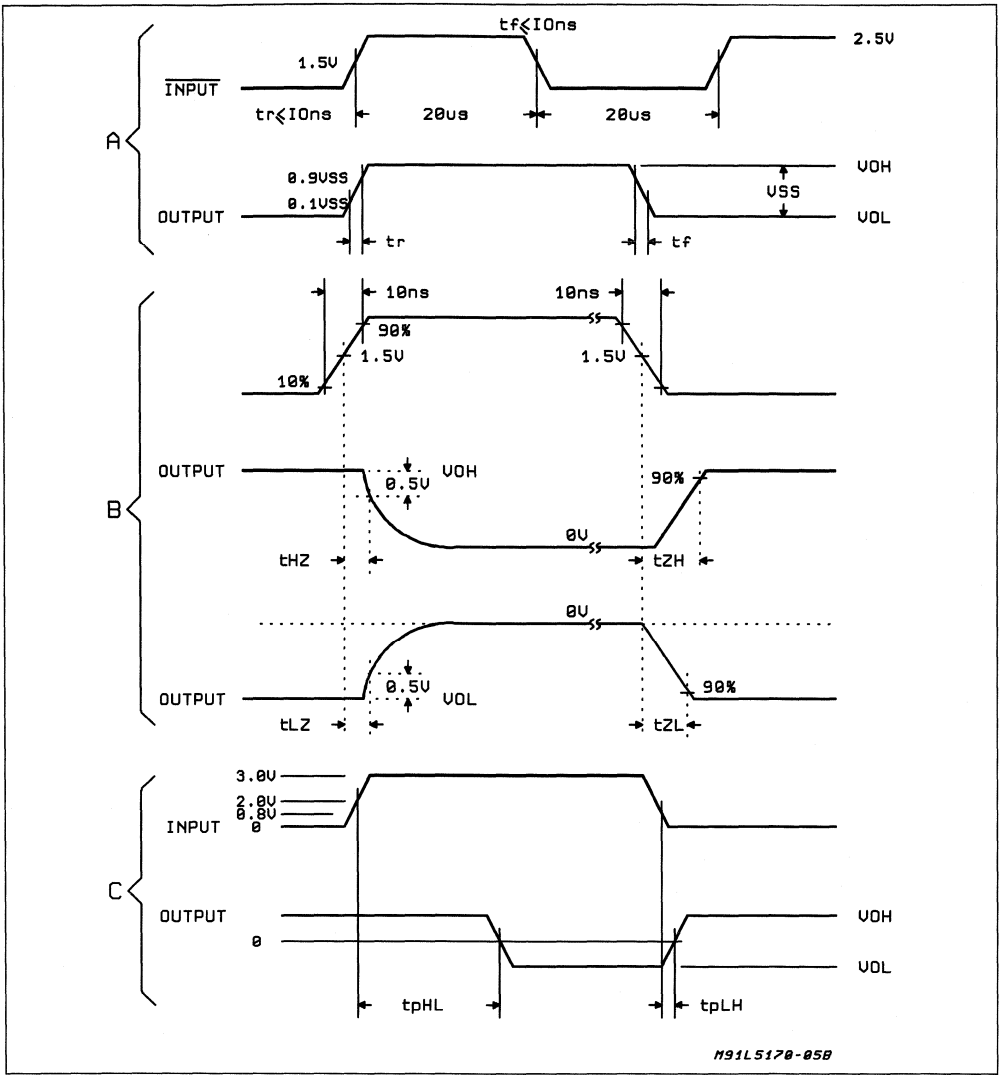
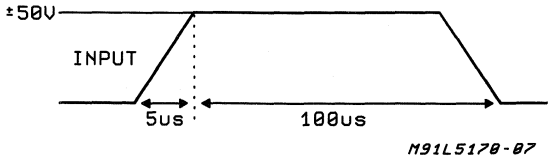


Figure 5: EOS Requirements



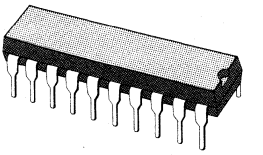
SGS-THOMSON MICROELECTRONICS

L6114
L6115

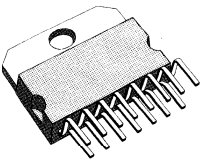
QUAD 100 V, DMOS SWITCH

- OUTPUT VOLTAGE TO 100 V
- 0.7 Ω $R_{DS(ON)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

MultiPower BCD Technology



Powerdip 14 + 3 + 3



Multiwatt-15

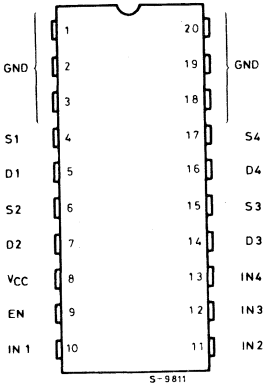
ORDER CODES : L6114 (Powerdip)
L6115 (Multiwatt-15)

DESCRIPTION

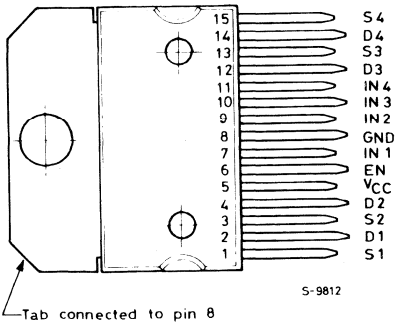
Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6114/15 monolithic quad DMOS switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6114 mounted in a Powerdip 14+3+3 package and the L6115 in a 15-lead Multiwatt package.

CONNECTION DIAGRAMS (top view)



L6114 (Powerdip)



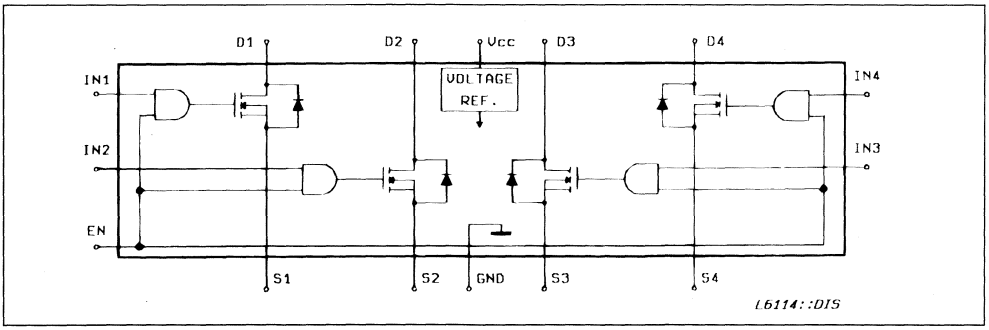
L6115 (Multiwatt-15)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
V_{DS}	Drain-source Voltage			100	V
V_{CC}	Supply Voltage			60	V
I_D	Continuous Drain Current	@ T_{pins} = 90 °C	Powerdip	1.5	A
		@ T_{case} = 90 °C	Multiwatt –15	3	A
I_{DM} (*)	Pulsed Drain Current		Powerdip	5	A
			Multiwatt –15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ T_{pins} = 90 °C	Powerdip	1.5	A
		@ T_{case} = 90 °C	Multiwatt –15	3	A
I_{SDM}	Pulsed Source Drain Diode Current		Powerdip	5	A
			Multiwatt –15	8	A
V_{IN}	Input Voltage			7	V
V_{EN}	Enable Voltage			7	V
V_S	Source Voltage			– 1 to + 4	V
P_{tot}	Total Power Dissipation	@ T_{pins} = 90 °C	Powerdip	4.3	W
		@ T_{case} = 90 °C	Multiwatt –15	20	W
		@ T_{amb} = 70 °C	Powerdip	1.3	W
		@ T_{amb} = 70 °C	Multiwatt –15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range			– 40 to + 150	°C

(*) Pulse width ≤ 300 µs, duty cycle ≤ 10 %.
Note : I_D, I_{DM}, I_{SD}, I_{SDM} are given per channel.

BLOCK DIAGRAM



THERMAL DATA

			Powerdip	Multiwatt–15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			14		48	V
I_{CC}	Supply Current	All V_{IN} = H V_{EN} = Square Wave (200 KHz, 50 % DC)			9		mA
I_Q	Quiescent Current	V_{EN} = L			2	3	mA
BV_{DSS}	Drain Source Breakdown Voltage	I_D = 1 mA V_{EN} = L		100			V
I_{DSS}	Output Leakage Current	V_{EN} = L	V_{DS} = 100 V			1	mA
			V_{DS} = 80 V T_j = 125 °C		1		mA
$R_{DS\ (on)}$ (*)	Static Drain-source on Resistance	$V_{CC} \geq$ 14 V V_{EN}, V_{IN} = H	I_D = 1.5 A		0.7		Ω
$V_{IN\,L}$, $V_{EN\,L}$	Input Low Voltage			− 0.3		0.8	V
$V_{IN\,H}$, $V_{EN\,H}$	Input High Voltage			2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low Current	V_{IN}, V_{EN} = L				− 100	µA
$I_{IN\,H}$, $I_{EN\,H}$	Input High Current	V_{IN}, V_{EN} = H				10	µA
$t_{d\ (on)}$	Turn on Delay Time	I_D = 1.5 A See Test Circuit and Waveforms			300		ns
t_r	Rise Time				100		ns
$t_{d\ (off)}$	Turn off Delay Time				400		ns
t_f	Fall Time				100		ns
V_{SD} (*)	Source Drain Diode Forward Voltage	I_{SD} = 1.5 A	V_{EN} = L			1.5	V
$V_{SD\ (on)}$ (*)	Source Drain Forward Voltage	I_{SD} = 1.5 A V_{IN}, V_{EN} = H				1.2	V

(*) Pulse test : pulse width = 300 µs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit
(Pins x = Powerdip ; Pins (x) = Multiwatt).

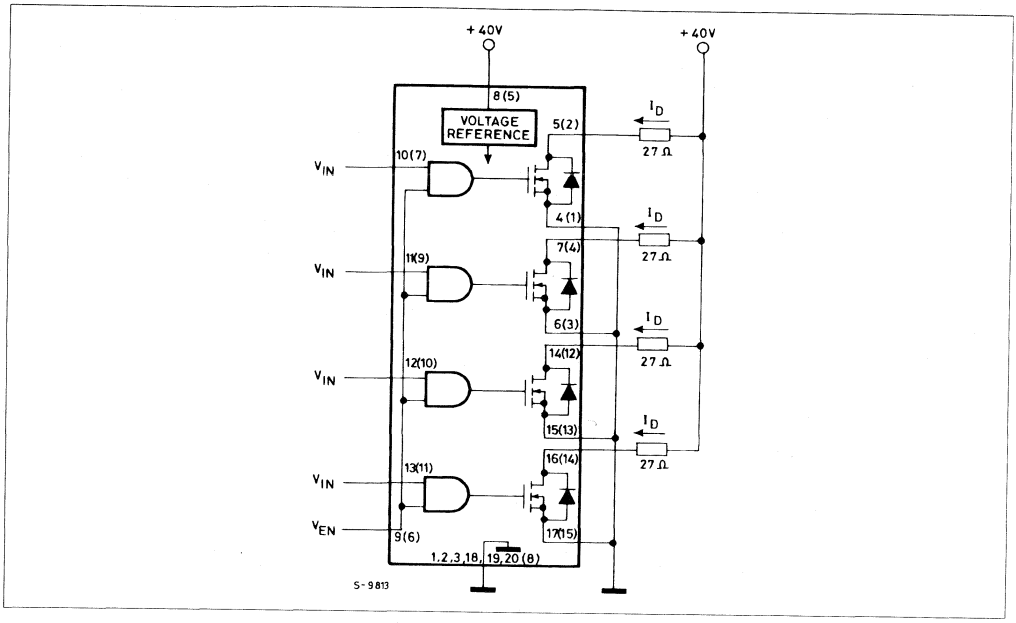
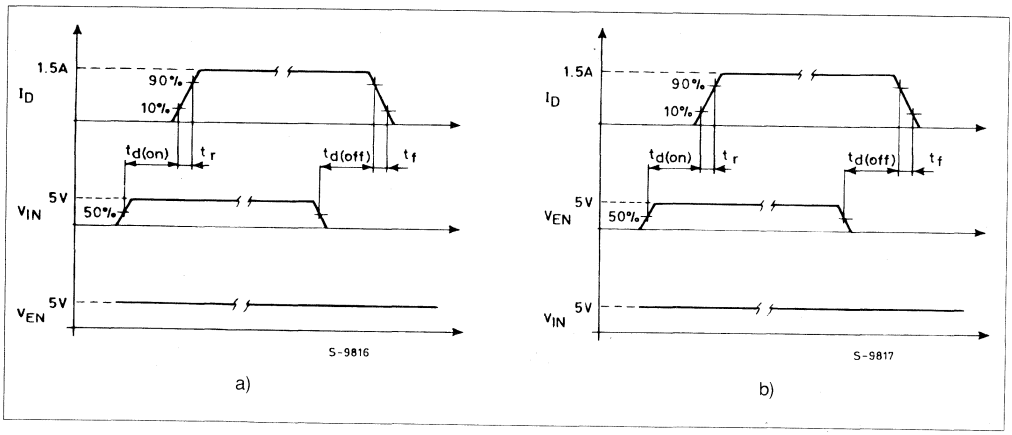
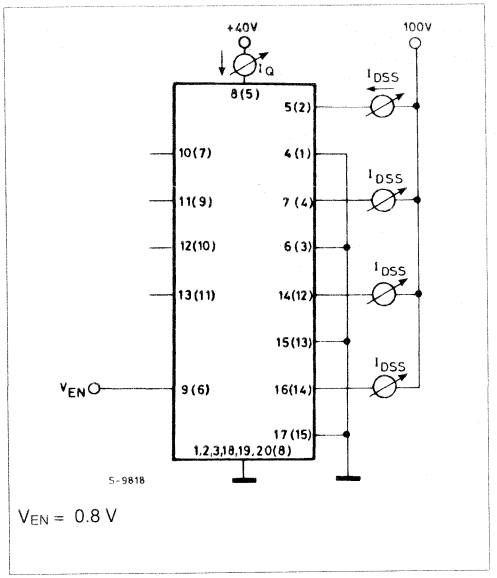


Figure 2 : Waveforms.



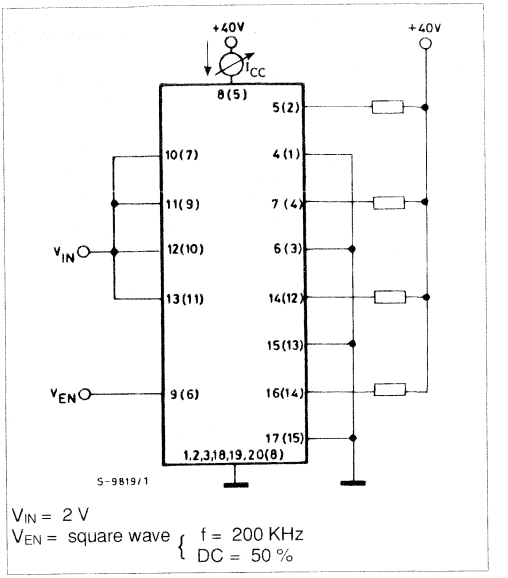
TEST CIRCUIT (Pins x = Powerdip ; Pins (x) = Multiwatt)

Figure 3 : Quiescent Current and Output Leakage Current..



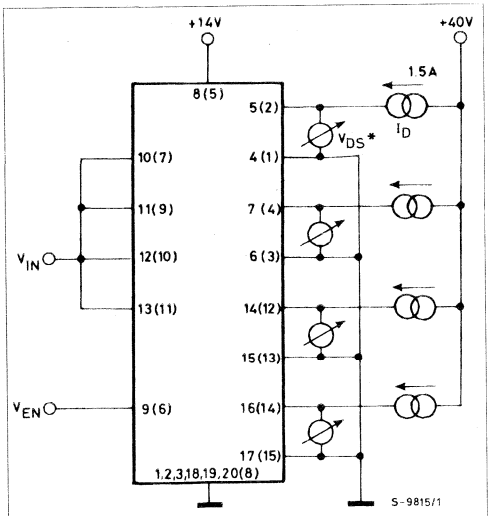
V_{EN} = 0.8 V

Figure 4 : Supply Current.



V_{IN} = 2 V
V_{EN} = square wave { f = 200 KHz, DC = 50 %

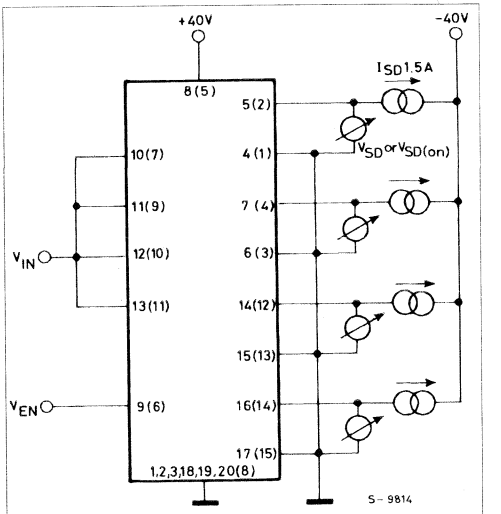
Figure 5 : $R_{DS\ (on)}$.



V_{CC} = 14 V, V_{IN} = 2 V, V_{EN} = 2V
I_D = square wave, f = 3 KHz DC = 2 %
(*) V_{DS} is taken during the time in which the I_D = 1.5 A

$$R_{DS} = \frac{V_{DS}}{1.5}$$

Figure 6 : Source-drain Diode Forward Voltage.



V_{IN} = 2 V, I_{SD} square wave, f = 3 KHz DC = 2 %
- Set V_{EN} = 0.8 V for V_{SD} (taken during the time in which I_{SD} = 1.5 A)
- Set V_{EN} = 2 V for $V_{SD\ (on)}$ (taken during the time in which I_{SD} = 1.5 A)

Figure 7 : Input Logic Levels

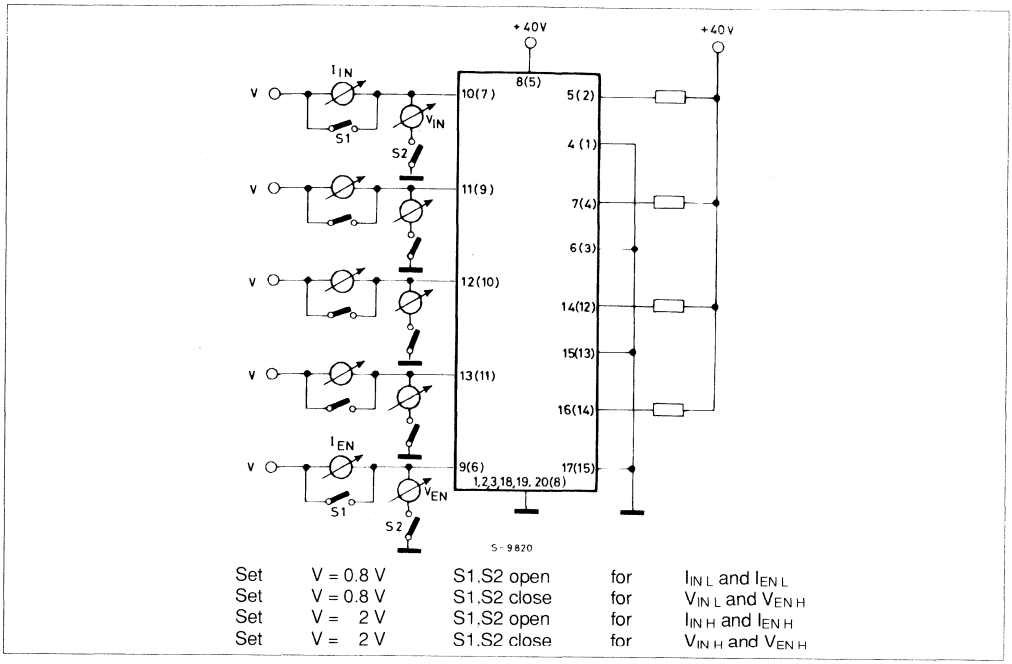


Figure 8 : Static Drain-source on Resistance.

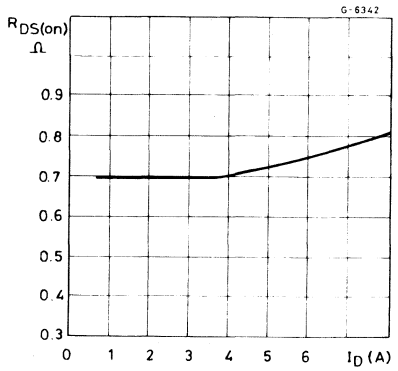


Figure 9 : Normalized Break-down Voltage vs. Temperature.

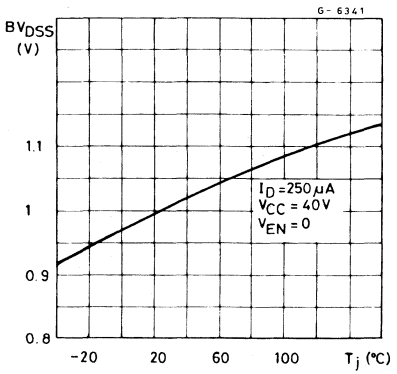


Figure 10 : Normalized on Resistance vs. Temperature.

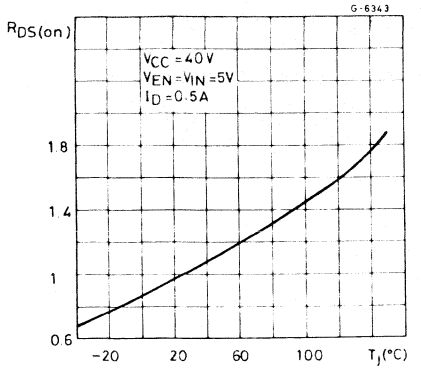


Figure 11 : Typical Source-drain Diode Forward Voltage.

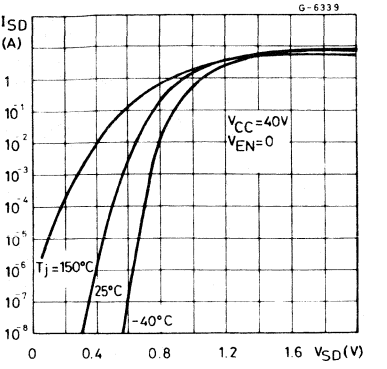
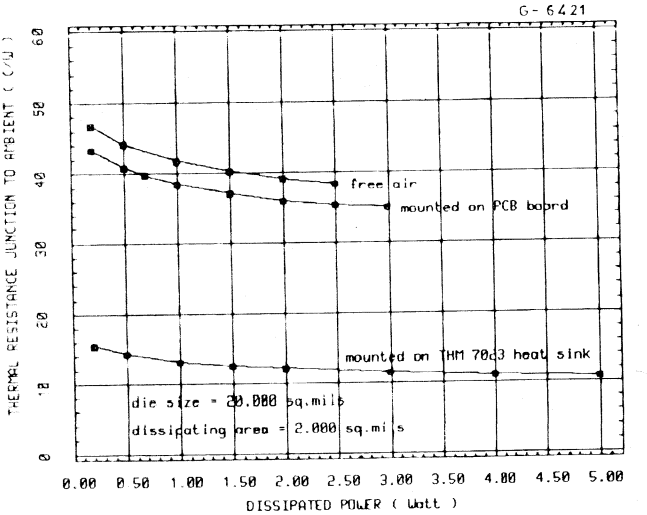


Figure 12 : $R_{th\ j\text{-}amb}$ vs. Dissipated Power(Multiwatt).



(*) R_{th} = 9 °C/W.

Figure 13 : Transient Thermal Resistance for Single Pulses (Multiwatt).

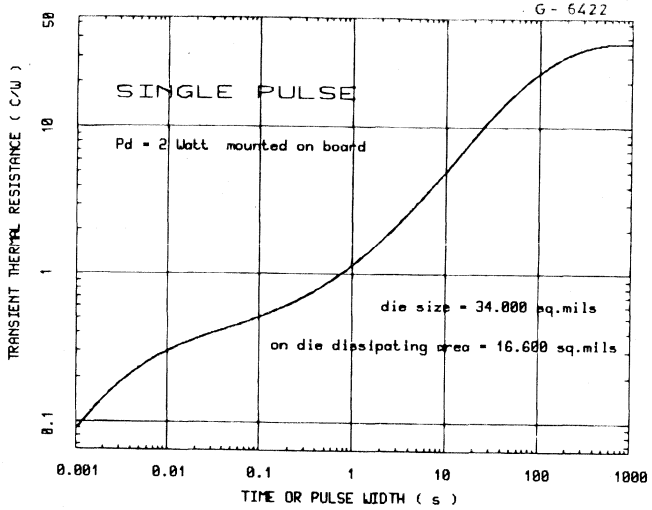
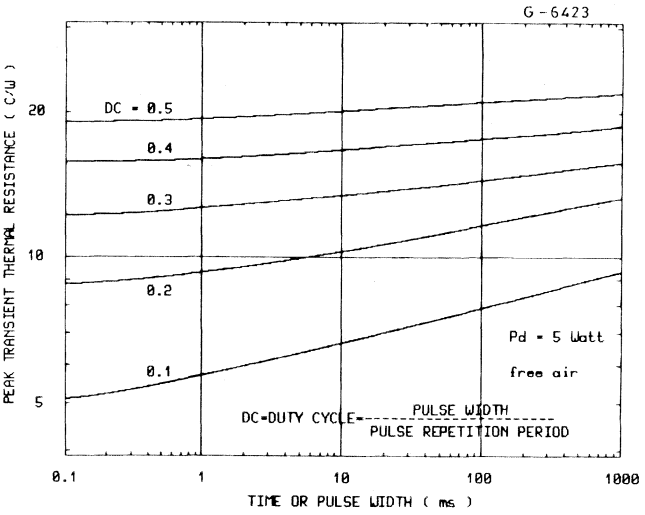


Figure 14 : Peak Transient Thermal Resistance vs.Pulse width and duty cycle (Multiwatt).



SGS-THOMSON MICROELECTRONICS

SGS-THOMSON MICROELECTRONICS

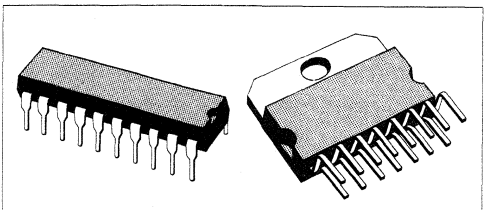
L6122
L6123

100 V DMOS SWITCHES

ADVANCE DATA

- OUTPUT VOLTAGE TO 100 V
- 0,5 Ω $R_{DS\ (on)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

MultiPower BCD Technology



Powerdip 14+3+3 — **Multiwatt-15**

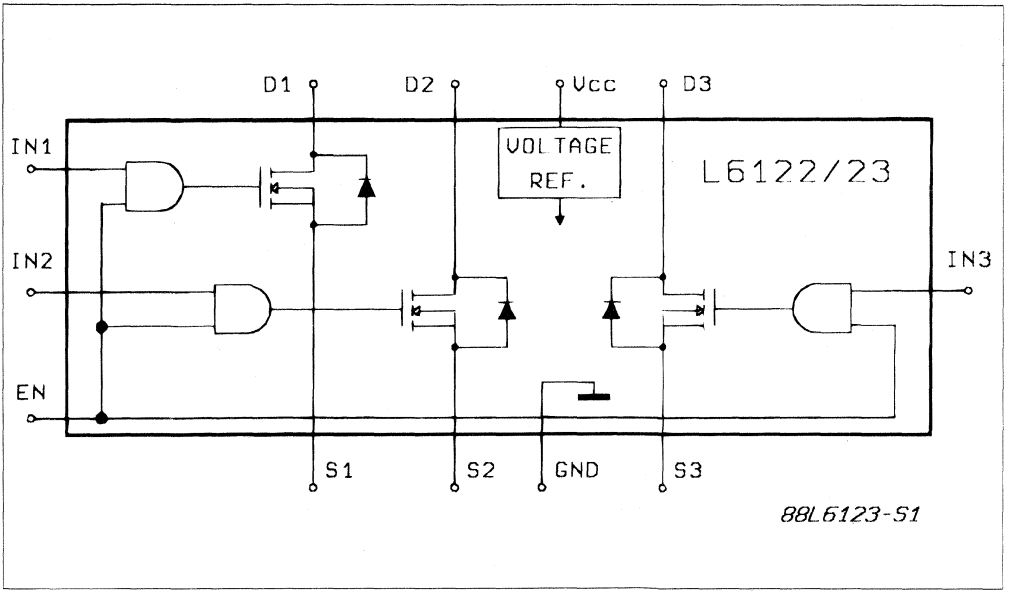
ORDER CODES : L6122, L6123

DESCRIPTION

Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6122/23 monolithic three DMOS switch is designed for high current, high voltage switching applications. Each of the three switches is controlled by a logic input and all three are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6122 mounted in a Powerdip 14 + 3 + 3 package and the L6123 in a 15-lead Multiwatt package.

BLOCK DIAGRAM



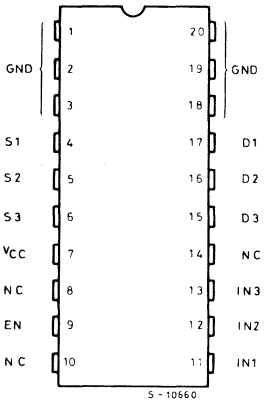
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

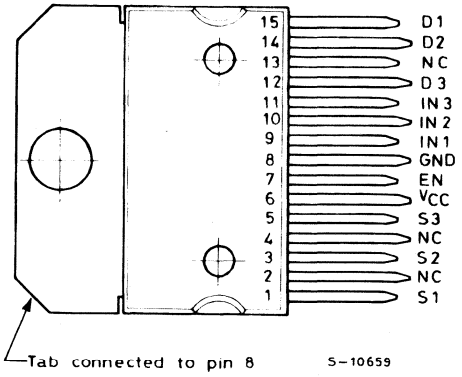
Symbol	Parameter		Value	Unit
V_{DS}	Drain-source Voltage		100	V
V_{CC}	Supply Voltage		60	V
I_D	Continuous Drain Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{DM} (*)	Pulsed Drain Current	Powerdip	5	A
		Multiwatt –15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{SDM}	Pulsed Source Drain Diode Current	Powerdip	5	A
		Multiwatt –15	8	A
V_{IN}	Input Voltage		7	V
V_{EN}	Enable Voltage		7	V
V_S	Source Voltage		– 1 to + 4	V
P_{tot}	Total Power Dissipation	@ T_{pins} = 90 °C Powerdip	4.3	W
		@ T_{case} = 90 °C Multiwatt –15	20	W
		@ T_{amb} = 70 °C Powerdip	1.3	W
		@ T_{amb} = 70 °C Multiwatt –15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range		– 40 to + 150	°C

(*) Pulse width ≤ 300 µs, duty cycle ≤ 10 %.
NOTE : I_D, I_{DM}, I_{SD}, I_{SDM} are given per channel.

CONNECTION DIAGRAMS (top view)



L6122 (Powerdip)



L6123 (Multiw. 15)

THERMAL DATA

			Powerdip	Multiwatt –15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	-
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	-	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			14		48	V
I_{CC}	Supply Current	All V_{IN} = H V_{EN} = Square Wave (200 KHz, 50 % DC)			9		mA
I_Q	Quiescent Current	V_{EN} = L			2	3	mA
BV_{DSS}	Drain Source Breakdown Voltage	I_D = 1 mA V_{EN} = L		100			V
I_{DSS}	Output Leakage Current	V_{EN} = L	V_{DS} = 100 V			1	mA
			V_{DS} = 80 V T_j = 125 °C		1		mA
$R_{DS\ (on)}$ (*)	Static Drain-source on Resistance	$V_{CC} \geq$ 14 V V_{EN}, V_{IN} = H	I_D = 1.5 A		0.7		Ω
V_{INL}, V_{ENL}	Input Low Voltage			– 0.3		0.8	V
V_{INH}, V_{ENH}	Input High Voltage			2		7	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN}, V_{EN} = L				– 100	µA
I_{INH}, I_{ENH}	Input High Current	V_{IN}, V_{EN} = H				10	µA
$t_{d\ (on)}$	Turn on Delay Time	I_D = 1.5 A See Test Circuit and Waveforms			300		ns
t_r	Rise Time				100		ns
$t_{d\ (off)}$	Turn off Delay Time				400		ns
t_f	Fall Time				100		ns
V_{SD} (*)	Source Drain Diode Forward Voltage	I_{SD} = 1.5 A	V_{EN} = L			1.5	V
$V_{SD\ (on)}$ (*)	Source Drain Forward Voltage	I_{SD} = 1.5 A V_{IN}, V_{EN} = H				1.2	V

(*) Pulse test : pulse width = 300 µs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit.

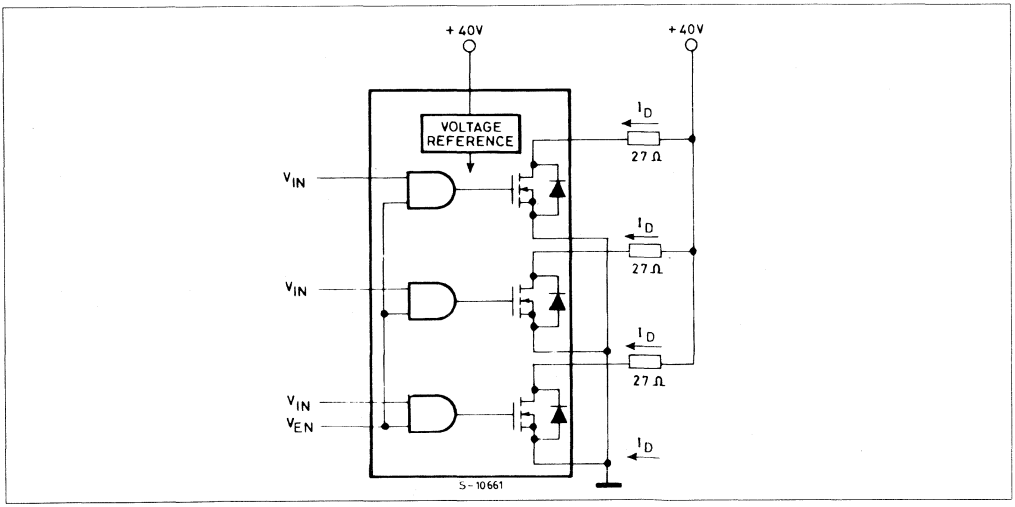


Figure 2 : Waveforms.

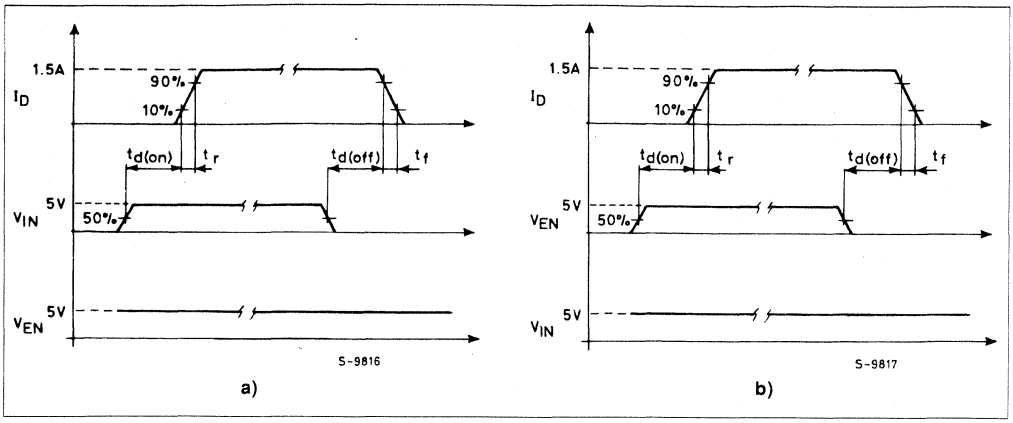


Figure 3 : Static Drain-source on Resistance.

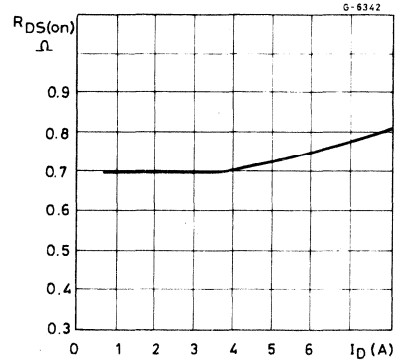


Figure 4 : Normalized Breakdown Voltage vs. Temperature.

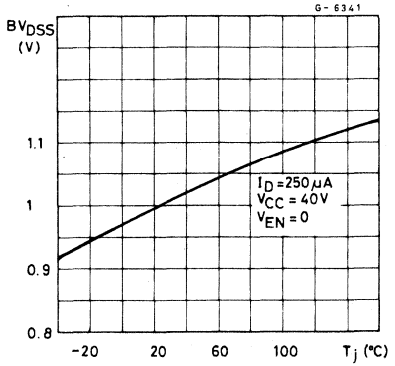


Figure 5 : Normalized on Resistance vs. Temperature.

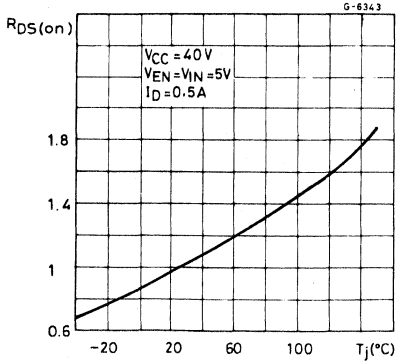


Figure 6 : Typical Source-drain Diode Forward Voltage.

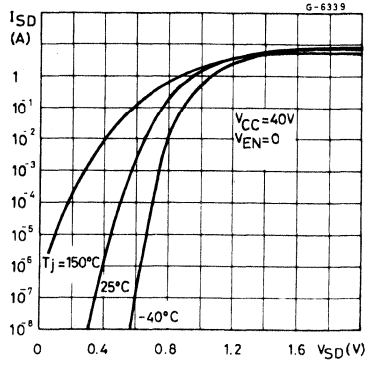
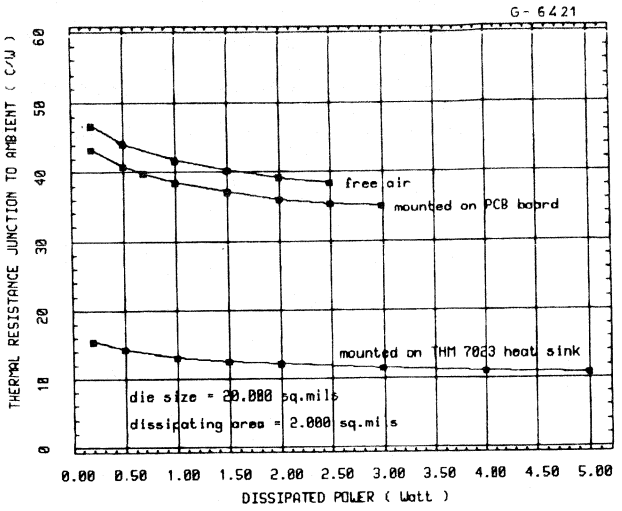


Figure 7 : $R_{th\ j\text{-}amb}$ vs. Dissipated Power (Multiwatt).



(*) Rth ≈ 9°C/W

Figure 8 : Transient Thermal Resistance for Single Pulses (Multiwatt).

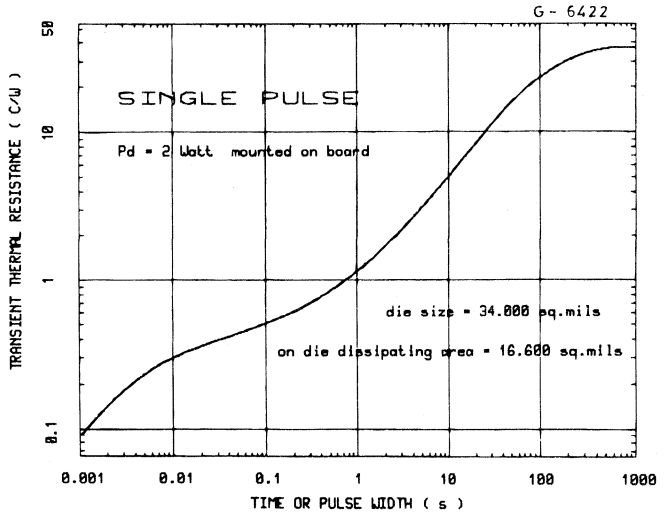
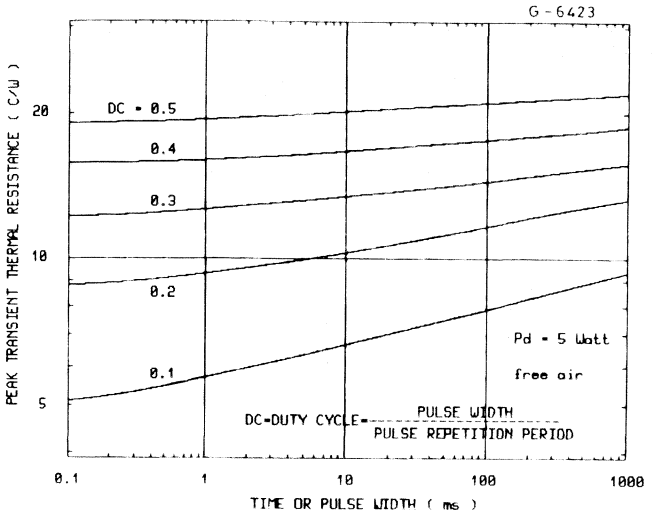


Figure 9 : Peak Transient Thermal Resistance vs. Pulse Width and Duty Cycle (Multiwatt).



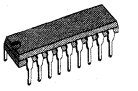
L6201
L6202-L6203

DMOS FULL BRIDGE DRIVER

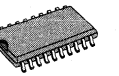
PRELIMINARY DATA

- SUPPLY VOLTAGE UP TO 48 V
- 5A MAX PEAK CURRENT (2A max. for L6201)
- TOTAL RMS CURRENT UP TO L6201: 1A; L6202: 1.5A; L6203: 4A
- $R_{DS\ (ON)}$ 0.3 Ω (typical value at 25 °C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100 KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY

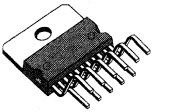
MULTIPOWER BCD TECHNOLOGY



Powerdip 12+3+3



SO20 (12+4+4)



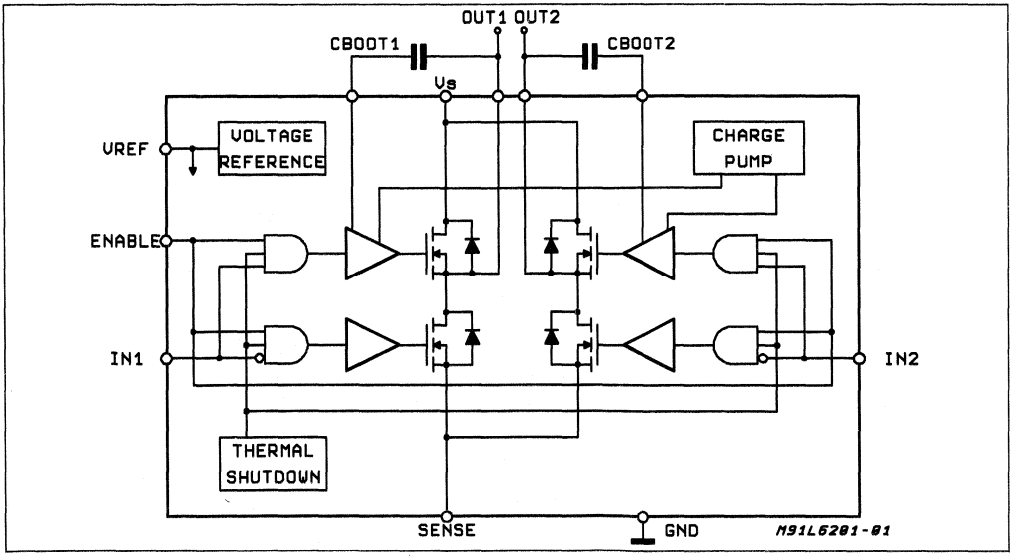
Multiwatt11

ORDERING NUMBERS:
L6201 (SO)
L6202 (Powerdip)
L6203 (Multiwatt)

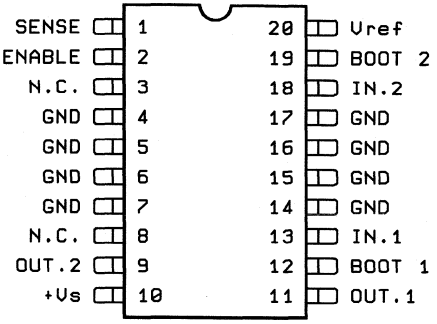
DESCRIPTION

The I.C. is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can operate at supply voltages up to 48 V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The I.C. is mounted in three different packages.

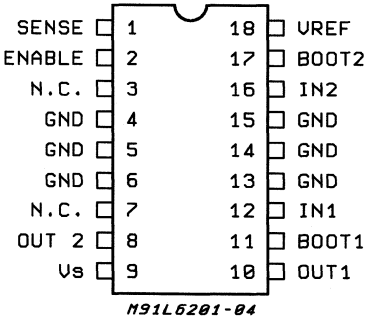
BLOCK DIAGRAM



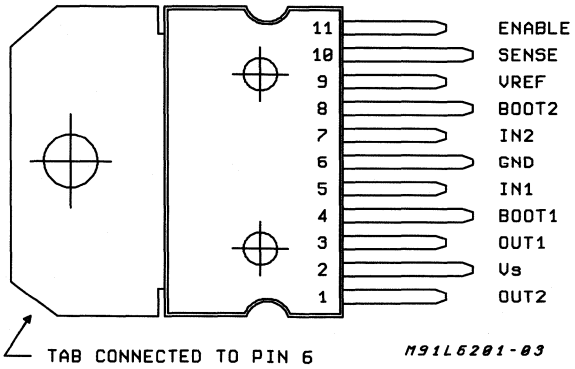
PIN CONNECTIONS (Top view)



SO20



POWERDIP



MULTIWATT11

PINS FUNCTIONS

Device			Name	Function
L6201	L6202	L6203		
1	1	10	SENSE	A resistor R_{sense} connected to this pin provides feedback for motor current control.
2	2	11	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	3		N.C.	Not Connected
4,5	4	6	GND	Common Ground Terminal
–	5		GND	Common Ground Terminal
6,7	6		GND	Common Ground Terminal
8	7		N.C.	Not Connected
9	8	1	OUT2	Ouput of 2nd Half Bridge
10	9	2	V_S	Supply Voltage
11	10	3	OUT1	Output of first Half Bridge
12	11	4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
13	12	5	IN1	Digital Input from the Motor Controller
14,15	13	6	GND	Common Ground Terminal
–	14		GND	Common Ground Terminal
16,17	15		GND	Common Ground Terminal
18	16	7	IN2	Digital Input from the Motor Controller
19	17	8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
20	18	9	V_{ref}	Internal voltage reference. A capacitor from this pin to GND is recommended. The internal Ref. Voltage can source out a current of 2mA max.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	52	V
V_{OD}	Differential Output Voltage (between Out1 and Out2)	60	V
V_{IN}, V_{EN}	Input or Enable Voltage	– 0.3 to + 7	V
I_o	Pulsed Output Current for L6202/03 (Note 1) – Non Repetitive (< 1 ms) for L6201 for L6202/03 DC Output Current for L6201 (Note 1)	5 5 10 1	A A A A
V_{sense}	Sensing Voltage	– 1 to + 4	V
V_b	Boostrap Peak Voltage	60	V
P_{tot}	Total Power Dissipation: T_{pins} = 90°C for L6201 for L6202 T_{case} = 90°C for L6203 T_{amb} = 70°C for L6201 (Note 2) for L6202 (Note 2) for L6203 (Note 2)	 4 5 20 0.9 1.3 2.3	 W W W W W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

Note 1: Pulse width limited only by junction temperature and transient thermal impedance (see thermal characteristics)
Note 2: Mounted on board with minimized dissipating copper area.

THERMAL DATA

Symbol	Parameter		Value			Unit
			L6201	L6202	L6203	
$Rth_{j\text{-}pins}$	Thermal Resistance Junction-pins	max	15	12	–	°C/W
$Rth_{j\text{-}case}$	Thermal Resistance Junction Case	max.	–	–	3	°C/W
$Rth_{j\text{-}amb}$	Thermal Resistance Junction-ambient	max.	85	60	35	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the Test Circuits; T_j = 25°C, V_S = 42V, V_{sens} = 0, unless otherwise specified).

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			12	36	48	V
V_{ref}	Reference Voltage	I_{REF} = 2mA			13.5		V
I_{REF}	Output Current					2	mA
I_s	Quiescent Supply Current	EN = H V_{IN} = L EN = H V_{IN} = H EN = L (Fig. 1,2,3)	I_L = 0		10 10 8	15 15 15	mA mA mA
f_c	Commutation Frequency (*)				30	100	KHz
T_j	Thermal Shutdown				150		°C
T_d	Dead Time Protection				100		ns

TRANSISTORS

OFF							
I_{DSS}	Leakage Current	Fig. 11 V_s = 52 V				1	mA
ON							
R_{DS}	On Resistance	Fig. 4,5			0.3	0.55	Ω
$V_{DS(ON)}$	Drain Source Voltage	Fig. 9 I_{DS} = 1A I_{DS} = 1.2A I_{DS} = 3A	**L6201** **L6202** **L6203**		0.3 0.36 0.9		V V V
V_{sens}	Sensing Voltage			– 1		4	V

SOURCE DRAIN DIODE

V_{sd}	Forward ON Voltage	Fig. 6a and b I_{SD} = 1A **L6201** EN = L I_{SD} = 1.2A **L6202** EN = L I_{SD} = 3A **L6203** EN = L			0.9 (**) 0.9 (**) 1.35(**)		V V V
t_{rr}	Reverse Recovery Time	$\frac{dif}{dt}$ = 25 A/µs I_F = 1A I_F = 1.2A I_F = 3A	L6201 L6202 L6203		300		ns
t_{fr}	Forward Recovery Time				200		ns

LOGIC LEVELS

$V_{IN\ L}$, $V_{EN\ L}$	Input Low Voltage		– 0.3		0.8	V
$V_{IN\ H}$, $V_{EN\ H}$	Input High Voltage		2		7	V
$I_{IN\ L}$, $I_{EN\ L}$	Input Low Current	V_{IN}, V_{EN} = L			–10	µA
$I_{IN\ H}$, $I_{EN\ H}$	Input High Current	V_{IN}, V_{EN} = H		30		µA

ELECTRICAL CHARACTERISTICS (Continued)
LOGIC CONTROL TO POWER DRIVE TIMING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_1 (V_i)	Source Current Turn-off Delay	Fig. 12		300		ns
t_2 (V_i)	Source Current Fall Time	Fig. 12		200		ns
t_3 (V_i)	Source Current Turn-on Delay	Fig. 12		400		ns
t_4 (V_i)	Source Current Rise Time	Fig. 12		200		ns
t_5 (V_i)	Sink Current Turn-off Delay	Fig. 13		300		ns
t_6 (V_i)	Sink Current Fall Time	Fig. 13		200		ns
t_7 (V_i)	Sink Current Turn-on Delay	Fig. 13		400		ns
t_8 (V_i)	Sink Current Rise Time	Fig. 13		200		ns

(*) Limited by power dissipation
(**) In synchronous rectification the drain-source voltage drop VDS is shown in fig. 4 (L6202/03); typical value for the L6201 is of 0.3V.

Figure 1: Typical Normalized I_S vs. T_j

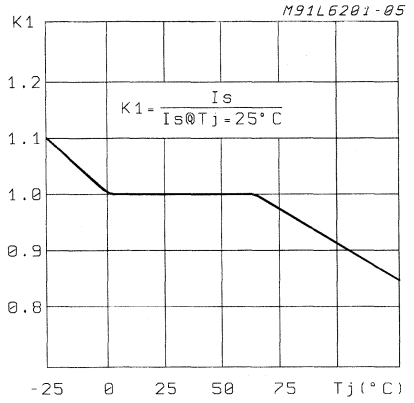


Figure 2: Typical Normalized Quiescent Current vs. Frequency

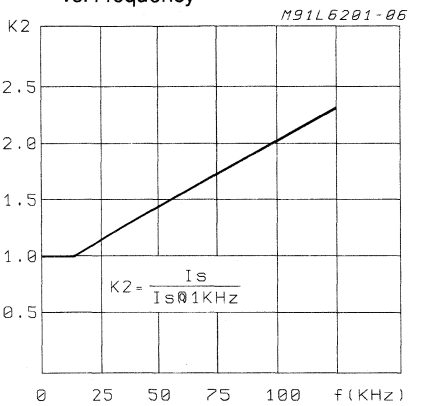


Figure 3: Typical Normalized I_S vs. V_S

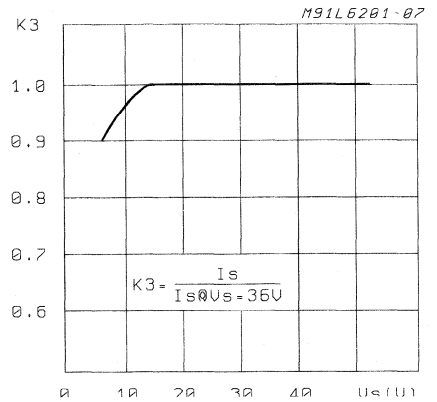


Figure 4: Typical $R_{DS\ (ON)}$ vs. V_S ~ V_{ref}

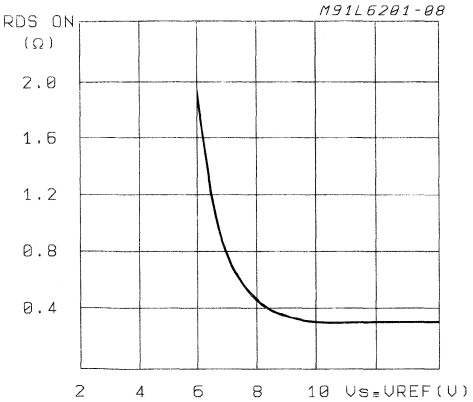


Figure 5: Normalized $R_{DS\ (ON)}$ at 25°C vs. Temperature Typical Values

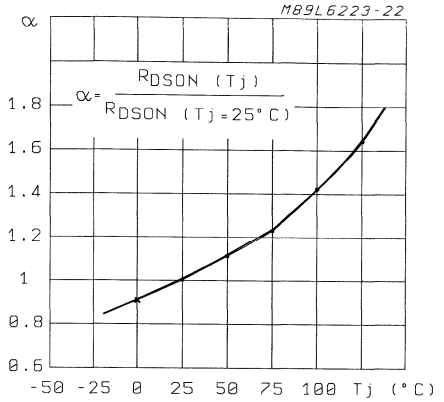


Figure 6a: Typical Diode Behaviour in Synchronous Rectification (L6201)

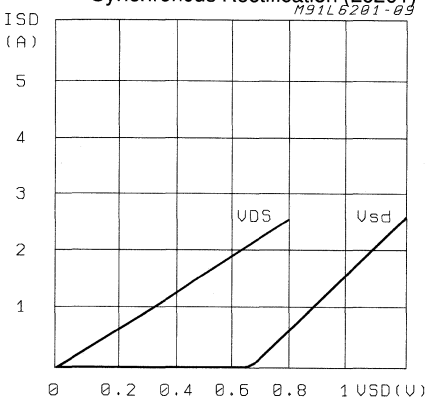


Figure 6b: Typical Diode Behaviour in Synchronous Rectification

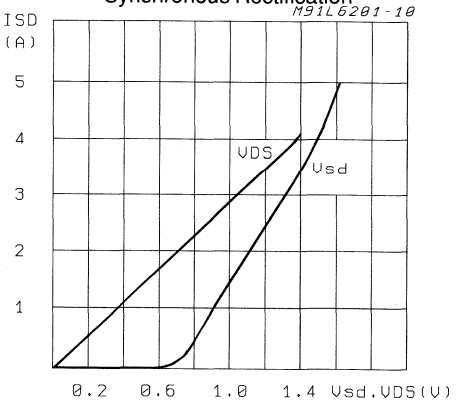


Figure 7a: Typical Power Dissipation vs I_L (L6201)

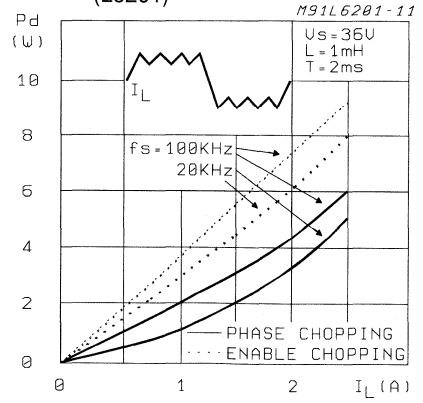


Figure 7b: Typical Power Dissipation vs I_L (L6202,L6203))

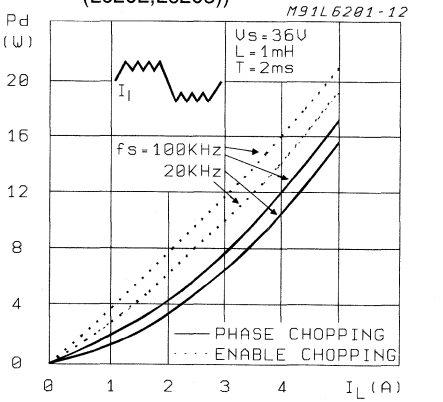


Figure 8a: Two Phase Chopping

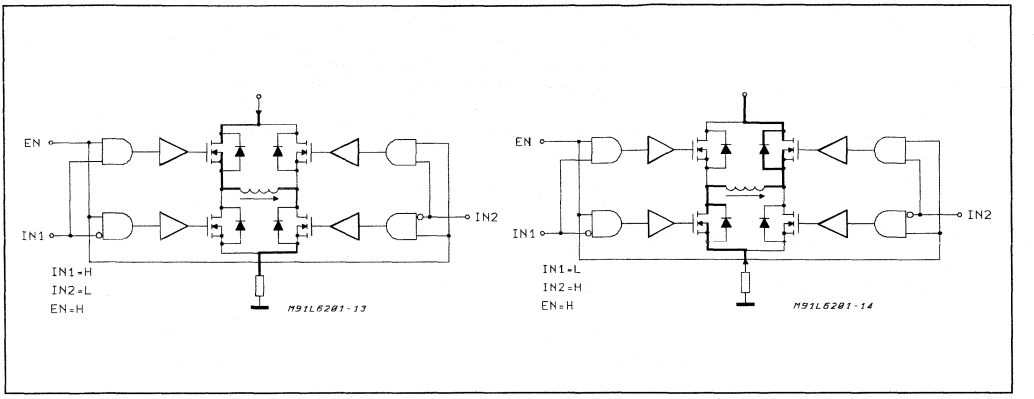


Figure 8b: One Phase Chopping

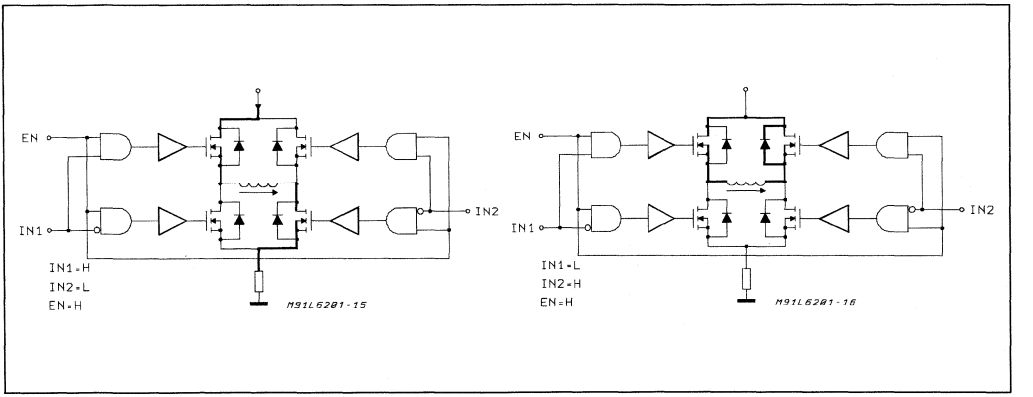
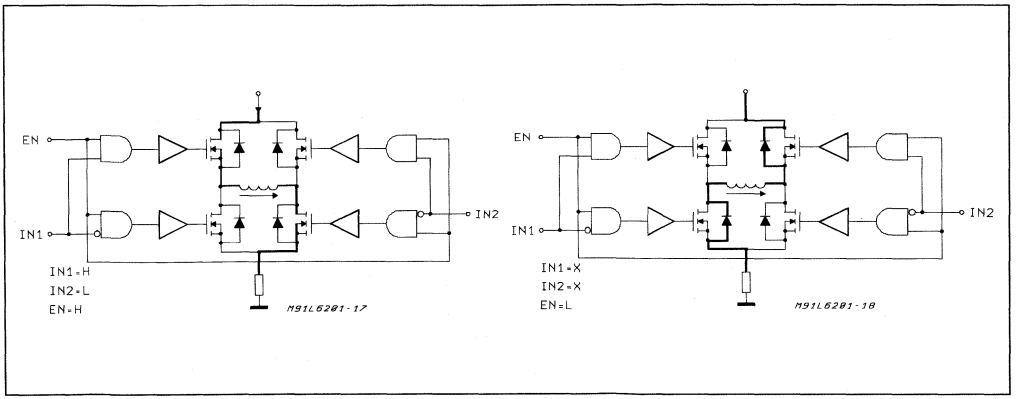


Figure 8c: Enable Chopping



TEST CIRCUITS

Figure 9: Saturation Voltage

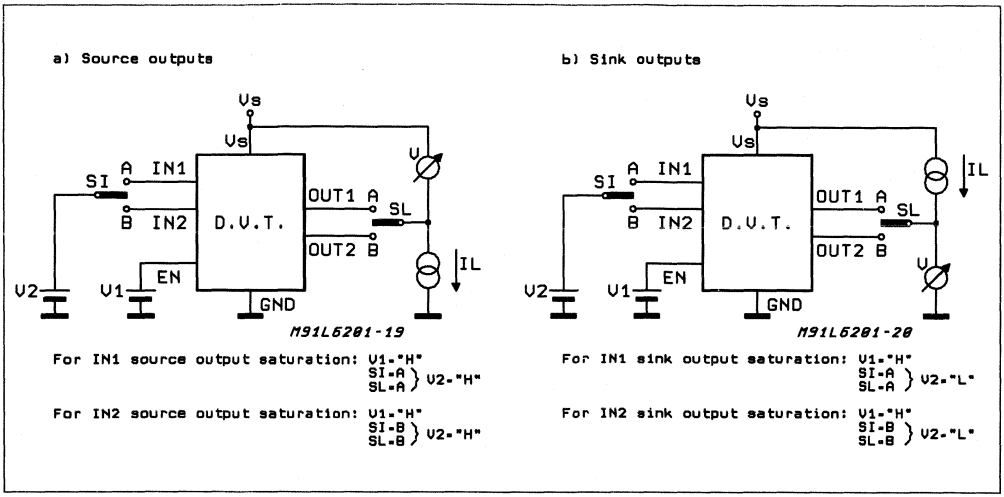


Figure 10: Quiescent Current

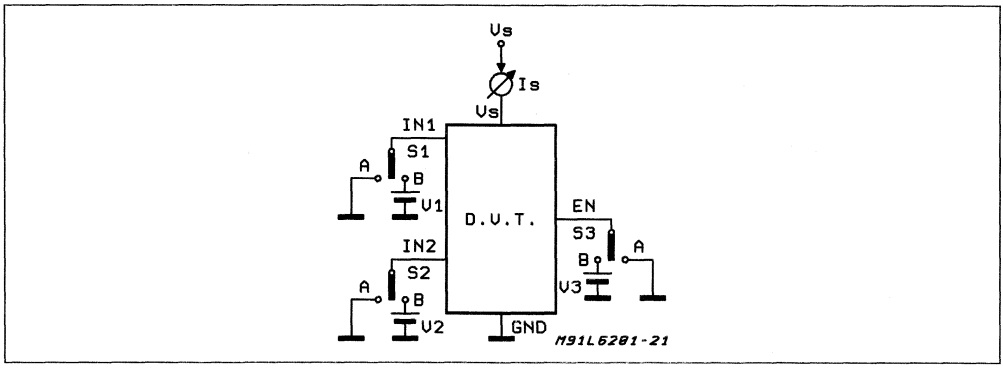


Figure 11: Leakage Current

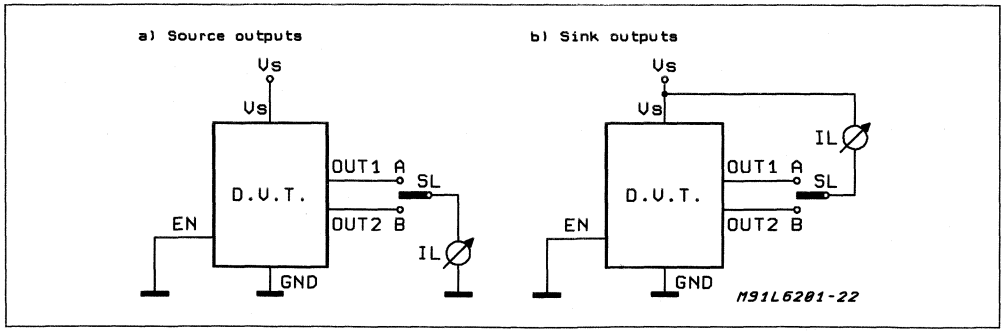


Figure 12: Source Current Delay Times vs. Input Chopper

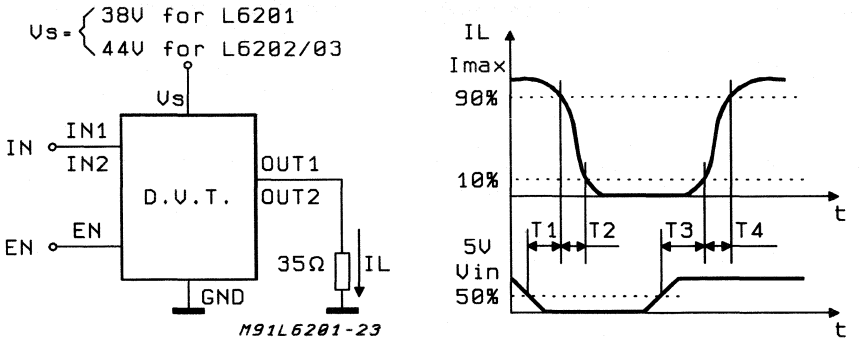
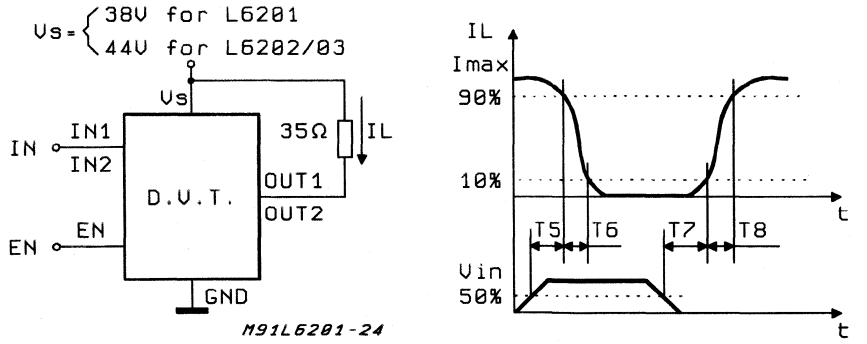


Figure 13: Sink Current Delay Times vs. Input Chopper



CIRCUIT DESCRIPTION

The L6201/2/3 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and µC compatible and eliminate the necessity of external MOS drive components. The Logic Drive is shown in table 1.

Table 1

Inputs			Output Mosfets (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned oFF

L = Low H = High X = DON't care
(*) Numbers referred to INPUT1 or INPUT2 controlled output stages

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (fig. 15).

Figure 14: Intrinsic Structures in the POWER DMOS Transistors

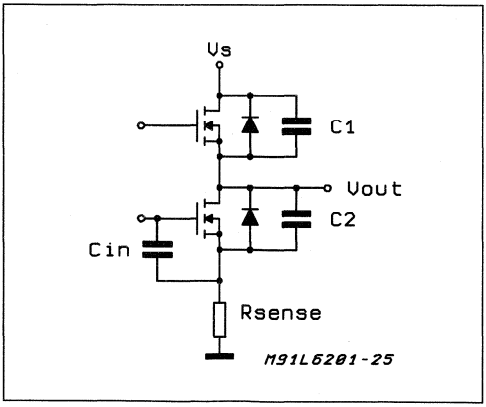
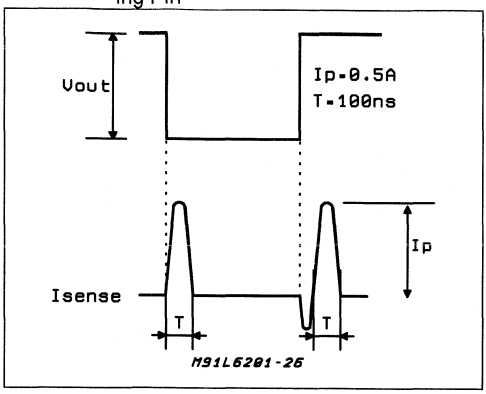


Figure 15: Current Typical Spikes on the Sensing Pin



TRANSISTOR OPERATION

ON State

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS\ (ON)}$ throughout the recommended operating range. In this condition the dissipated power is given by :

$$P_{ON} = R_{DS\ (ON)} \cdot I_{DS}^2\ (RMS)$$

The low $R_{DS\ (ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF State

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by :

$$P_{OFF} = V_S \cdot I_{DSS}$$

The power dissipation is very low and is negligible in comparison to that dissipated in the ON STATE.

Transitions

As already seen above the transistors have an intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)} \cdot I_D$ and when it reaches the diode forward voltage it is clamped. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage-current waveforms and in the driving mode. (see Fig. 7ab and Fig. 8abc).

$$P_{trans.} = I_{DS}\ (t) \cdot V_{DS}\ (t)$$

Boostrap Capacitors

To ensure that the POWER DMOS transistors are driven correctly gate to source voltage of typ. 10 V must be guaranteed for all of the N-channel DMOS transistors. This is easy to be provided for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. This is achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1 nF. It is recommended that a capacitance of at least 10 nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher RDS (ON). On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

Reference Voltage

To by-pass the internal Ref. Volt. circuit it is recommended that a capacitor be placed between its pin and ground. A value of 0.22 µF should be sufficient for most applications. This pin is also protected against a short circuit to ground: a max. current of 2mA max. can be sinked out.

Dead Time

To protect the device against simultaneous conduction in both arms of the bridge resulting in a rail to rail short circuit, the integrated logic control provides a dead time greater than 40 ns.

Thermal Protection

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the temperature has fallen to a safe level the device restarts the input and enable signals under control.

APPLICATION INFORMATION

Recirculation

During recirculation with the ENABLE input high, the voltage drop across the transistor is RDS (ON)· IL, clamped at a voltage depending on the characteristics of the source-drain diode. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problem because the voltage spike generated on the sense resistor is masked by the current controller circuit.

Rise Time T_r (See Fig. 16)

When a diagonal of the bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case :

$$E_{OFF/ON} = [R_{DS\ (ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

Load Time T_{LD} (See Fig.16)

During this time the energy dissipated is due to the ON resistance of the transistors (E_{LD}) and due to commutation (E_{COM}). As two of the POWER DMOS transistors are ON, E_{ON} is given by :

$$E_{LD} = I_L^2 \cdot R_{DS\ (ON)} \cdot 2 \cdot T_{LD}$$

In the commutation the energy dissipated is :

$$E_{COM} = V_S \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{LD}$$

Where :

$T_{COM} = T_{TURN\text{-}ON} = T_{TURN\text{-}OFF}$

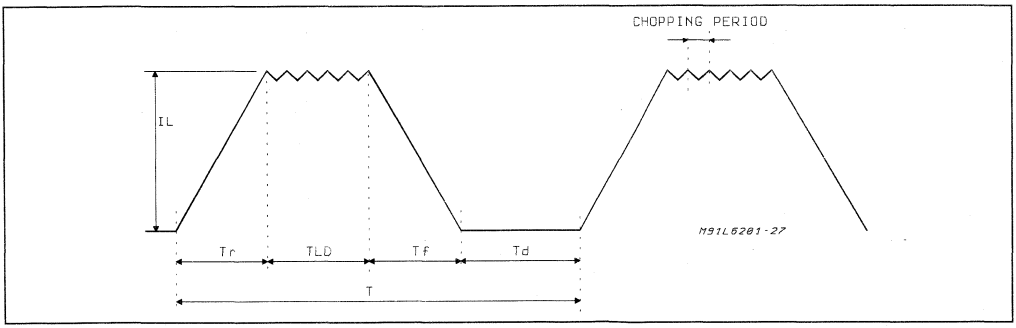
f_{SWITCH} = Chopping frequency.

Fall Time T_f (See Fig. 16)

It is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time :

$$E_{ON/OFF} = [R_{DS\ (ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

Figure 16.



Quiescent Energy

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

Total Energy Per Cycle

$$E_{TOT} = E_{OFF/ON} + E_{LD} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

The Total Power Dissipation P_{DIS} is simply :

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time

T_{LD} = Load drive time

T_f = Fall time

T_d = Dead time

T = Period

$T = T_r + T_{LD} + T_f + T_d$

DC Motor Speed Control

Since the I.C. integrates a full H-Bridge in a single package it is idealy suited for controlling DC motors. When used for DC motor control it performs the power stage required for both speed and direction control. The device can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17. In this particular configuration only half of the L6506 is used and the other half of the device may be used to control a second motor.

The L6506 senses the voltage across the sense resistor R_S to monitor the motor current: it compares the sensed voltage both to control the speed and during the brake of the motor.

Between the sense resistor and each sense input of the L6506 a resistor is recommended; if the connections between the outputs of the L6506 and the inputs of the L6203 need a long path, a resistor must be added between each input of the L6203 and ground.

A snubber network made by the series of R and C must be foreseen very near to the output pins of the I.C.; one diode (BYW98) is connected between each power output pin and ground as well.

The following formulas can be used to calculate the snubber values:

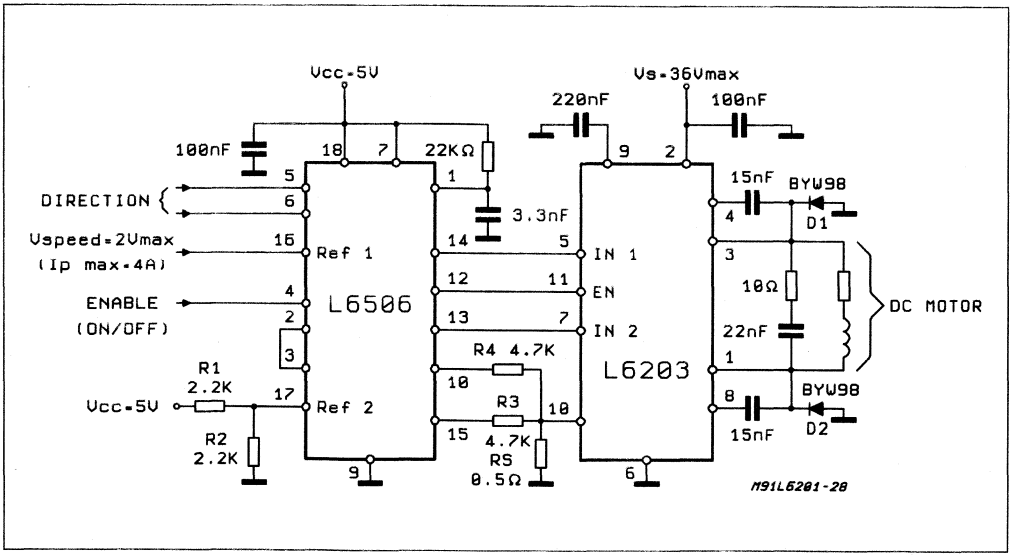
$R \cong V_S/I_p$

$C = I_p/(dV/dt)$ where:

V_S is the maximum Supply Voltage foreseen on the application;
I_p is the peak of the load current;
dv/dt is the limited rise time of the output voltage (200V/µs is generally used).

If the Power Supply Cannot Sink Current, a suitable large capacitor must be used and connected near the supply pin of the L6203. Sometimes a capacitor at pin 17 of the L6506 let the application better work. For motor current up to 2A max., the L6202 can be used in a similar circuit configuration for which a typical Supply Voltage of 24V is recommended.

Figure 17: Bidirectional DC Motor Control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with one L6506 or L297, two full bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface is realized.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component are minimalized: an R.C. network to set the chopper frequency, a resistive divider (R1; R2) to establish the comparator reference voltage and a snubber network made by R and C in series (See DC Motor Speed Control).

Figure 18: Two Phase Bipolar Stepper Motor Control Circuit with Chopper Current Control

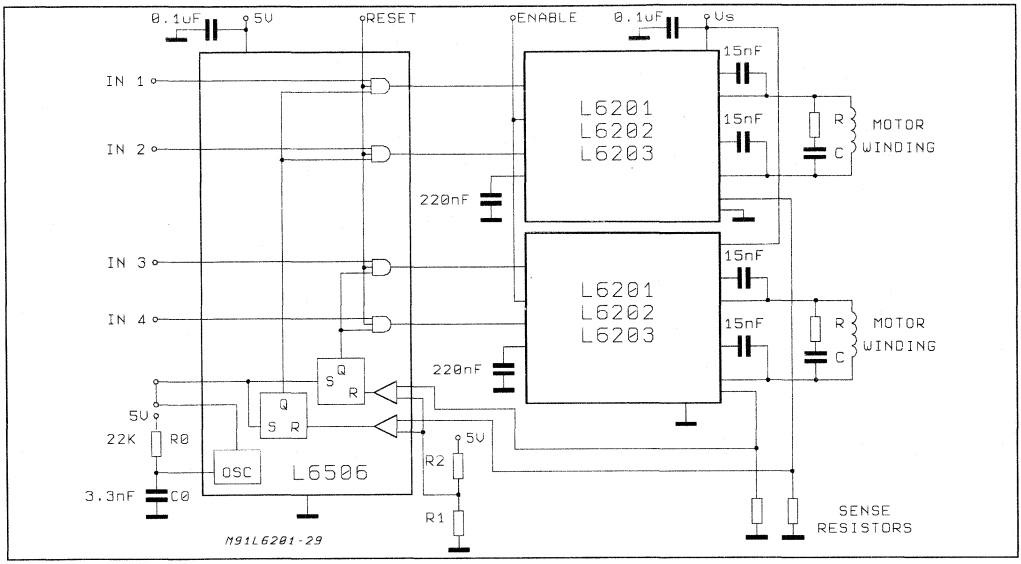
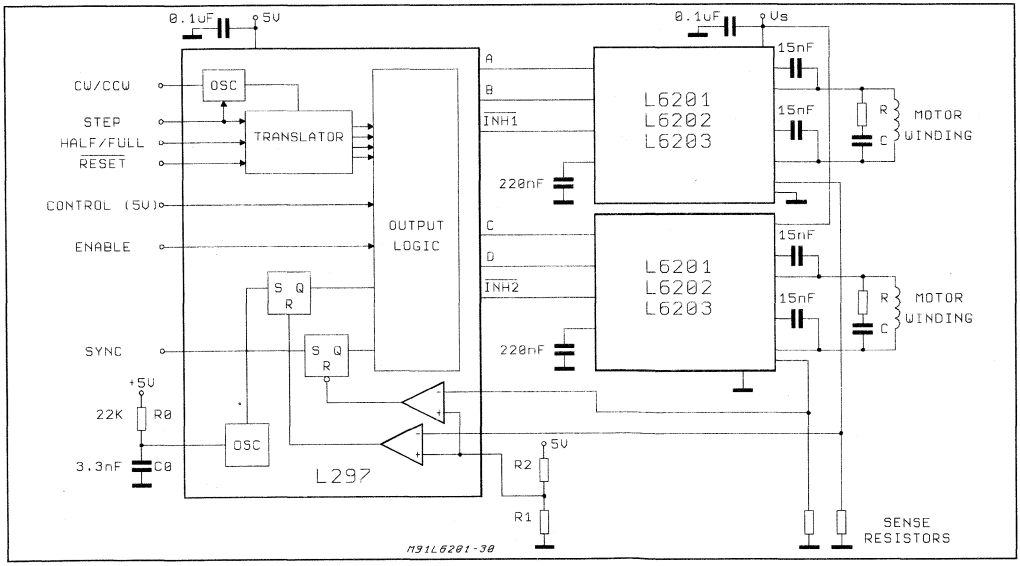
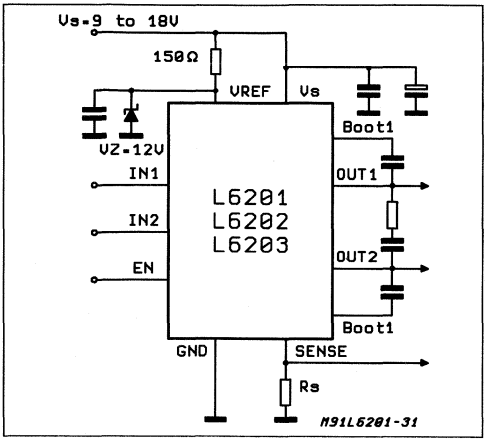


Figure 19: Two Phase Bipolar Stepper Motor Control Circuit with Chopper Current Control and Translator



It could be requested to drive a motor at V_S lower than the minimum recommended one of 12V (See Electrical Characteristics); in this case, by accepting a possible small increas in the $R_{DS\ (ON)}$ resistance of the power output transistors at the lowest Supply Voltage value, may be a good solution the one shown in Fig. 20.

Figure 20: L6201/2/3 Used at a Supply Voltage Range Between 9 and 18V



THERMAL CHARACTERISTICS

Thanks to the high efficiency of this device, often a true heatsink is not needed or it is simply obtained by means of a copper side on the P.C.B. (L6201/2).
Under heavy conditions, the L6203 needs a suitable cooling.
By using two square copper sides in a similar way as it shown in Fig. 23, Fig. 21 indicates how to choose the on board heatsink area when the L6201 total power dissipation is known since:

$$R_{Th\ j\text{-}amb} = (T_{j\ max.} - T_{amb\ max}) / P_{tot}$$

Figure 22 shows the Transient Thermal Resistance vs. a single pulse time width.
Figure 23 and 24 refer to the L6202.
For the Multiwatt L6203 addition information is given by Figure 25 (Thermal Resistance Junction-Ambient vs. Total Power Dissipation) and Figure 26 (Peak Transient Thermal Resistance vs. Repetitive Pulse Width) while Figure 27 refers to the single pulse Transient Thermal Resistance.

Figure 21: Typical $R_{Th\ J\text{-}amb}$ vs. "On Board" Heatsink Area (L6201)

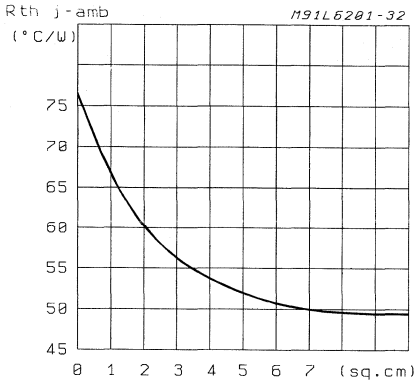
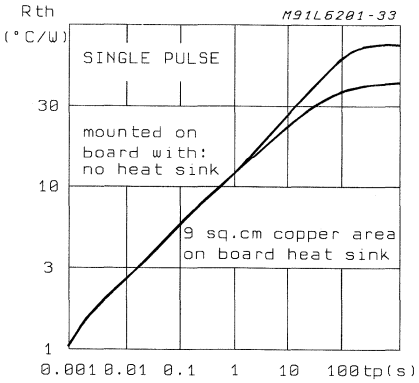


Figure 22: Typical Transient R_{TH} in Single Pulse Condition (L6201)



Figurre 23: Typical $R_{Th\ J\text{-}amb}$ vs. Two "On Board" Square Heatsink (L6202)

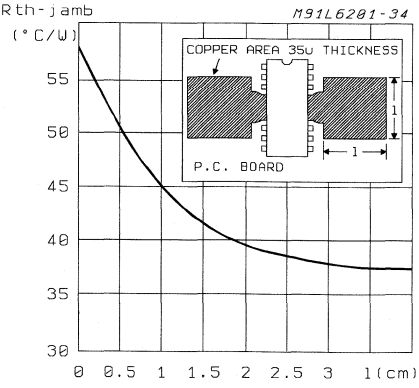


Figure 24: Typical Transient Thermal Resistance for Single Pulses (L6202)

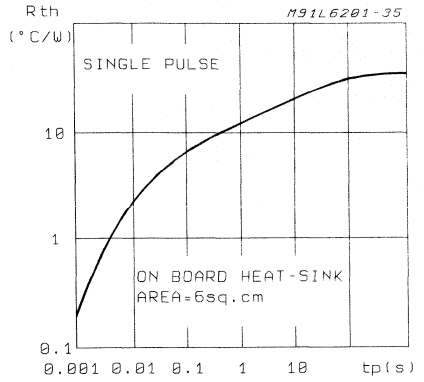


Figure 25: Typical $R_{Th\ J\text{-}amb}$ of Multiwatt Package vs. Total Power Dissipation

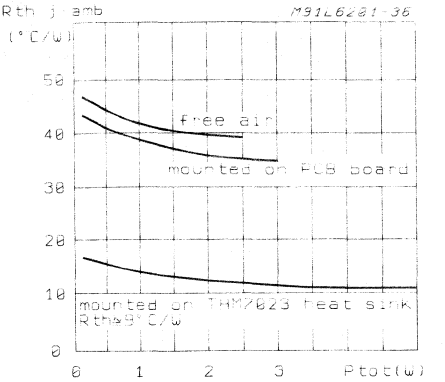


Figure 26: Typical Transient Thermal Resistance for Single Pulses with and without Heatsink (L6203)

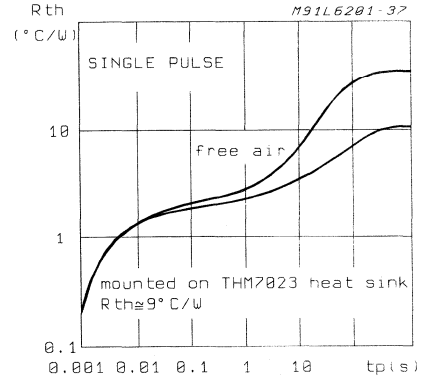
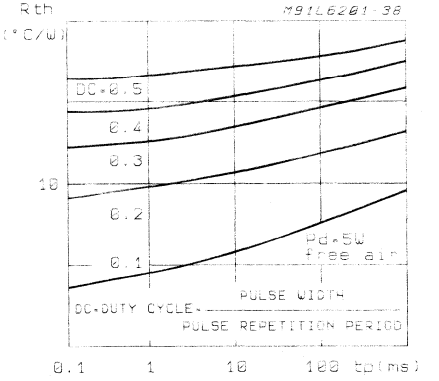


Figure 27: Typical Transient Thermal Resistance versus Pulse Width and Duty Cycle (L6203)

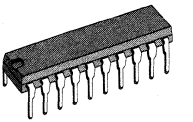


DMOS DUAL FULL BRIDGE DRIVER

ADVANCE DATA

- SUPPLY VOLTAGE UP TO 48V
- $R_{DS(ON)}$ 1.2Ω (25°C)
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- 0.5A DC CURRENT
- TTL/CMOS COMPATIBLE DRIVER
- HIGH EFFICIENCY CHOPPING

MULTIPOWER BCD TECHNOLOGY



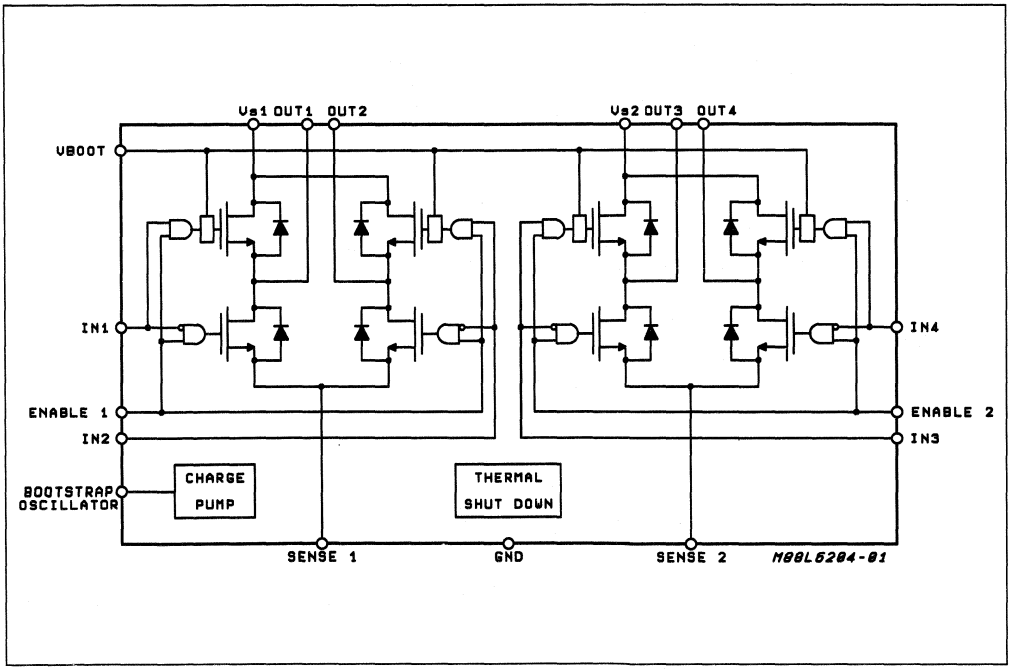
Powerdip 16+2+2

ORDERING NUMBER: L6204

DESCRIPTION

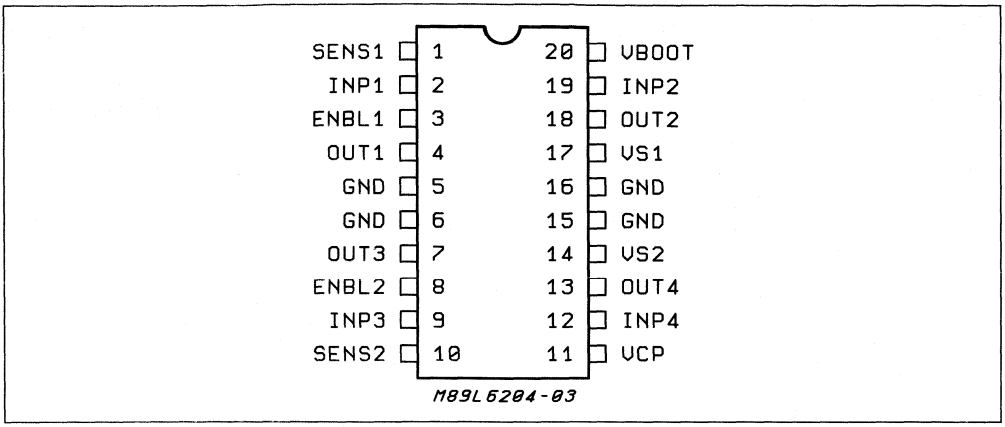
The L6204 is a dual full bridge driver for motor control applications realized in BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance.
The logic inputs are TTL/CMOS compatible. Both channels are controlled by a separate Enable.
Each bridge has a sense resistor to control the currenrt level.
The L6204 is mounted in an 20-lead Powerdip package and the four center pins are used to conduct heat to the PCB. At normal operating temperatures no external heatsink is required.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



PIN FUNCTIONS

Pin	Symbols	Functions
1	SENSE 1	Sense resistor to provide the feedback for motor current control of the bridge A
2	IN1	Digital input from the motor controller (bridge A)
3	ENABLE 1	A logic level low on this pin disable the bridge A
4	OUT 1	Output of one half bridge of the bridge A
5	GND	Common Power Ground
6	GND	Common Power Ground
7	OUT 3	Ouput of one half bridge of the bridge B
8	ENABLE 2	A logic level low on this pin disable the bridge B
9	IN 3	Digital input from the motor controller (bridge B)
10	SENSE 2	Sense resistor to provide the feedback for motor current control of the bridge B
11	BOOSTRAP OSC. VCP	Oscillator output for the external charge pump
12	IN 4	Digital input from the motor controller (bridge B)
13	OUT 4	Output of one half bridge of the bridge B
14	V_S2	Supply voltage bridge B
15	GND	Common Power Ground
16	GND	Common Power Ground
17	V_S1	Supply Voltage bridge A
18	OUT 2	Output of one half bridge of the bridge A
19	IN 2	Digital input from the motor controller (bridge A)
20	VBOOT	Overvoltage input for driving of the upper DMOS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	50	V
V_{IN}, V_{EN}	Input or Enable Voltage Range	-0.3 to +7	V
I_o	Pulsed Output Current	3	A
V_{SENSE}	Sensing Voltage	-1 to 4	V
V_{BOOT}	Bootstrap Supply	60	V
P_{tot}	Total power dissipation: (T_{pins} = 80°C) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C 8cm^2 copper area on PCB)	5 1.23 2	W W W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 42V, T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		12		48	V
I_S	Total Quiescent Current	EN1=EN2=H; IN1=IN2=IN3=IN4=L EN1 = EN2 = L			10 10	mA mA
f_C	Commutation Frequency			20		KHz
T_J	Thermal Shutdown			150		°C
T_d	Dead Time Protection			500		ns

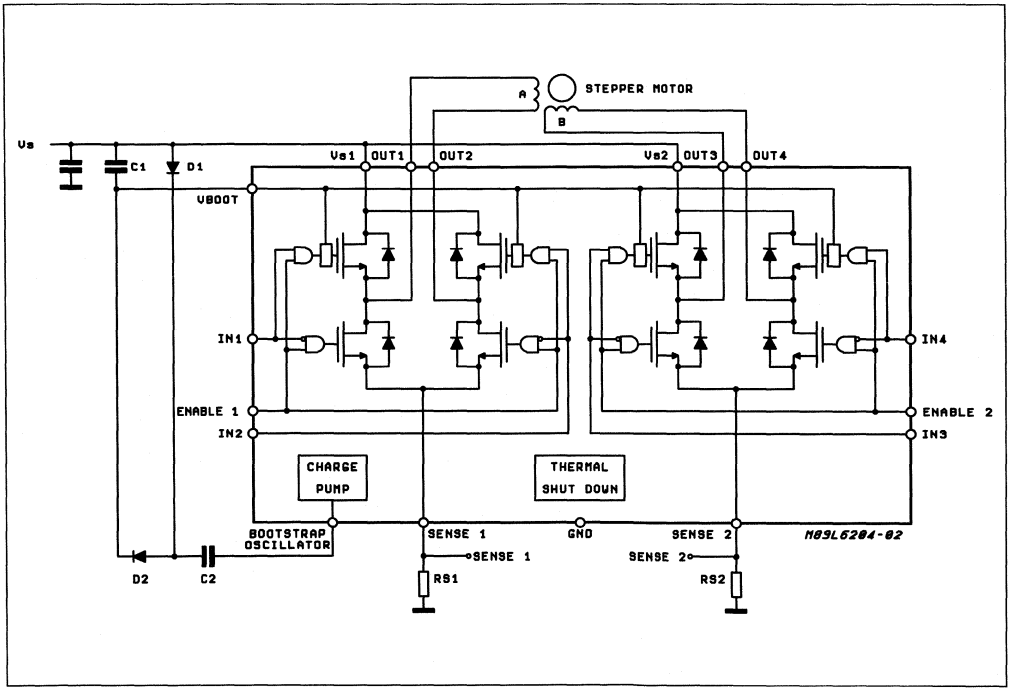
TRANSISTORS

I_{DSS}	Leakage Current	OFF		1		mA
R_{DS}	On Resistance	ON		1.2		Ω

LOGIC LEVELS

V_{INL}, V_{ENL}	Input Low Voltage		-0.3		0.8	V
V_{INH}, V_{ENH}	Input High Voltage		2		7	V
I_{INL}, I_{ENL}	Input Low Current	IN1 = IN2 = IN3 = IN4 = EN1 = EN2 = L			-10	µA
I_{INH}, I_{ENH}	Input High Current	IN1 = IN2 = IN3 = IN4 = EN1 = EN2 = H		50		µA

APPLICATION DIAGRAM



CIRCUIT DESCRIPTION

L6204 is a dual full bridge IC designed to drive DC motors, stepper motors and other inductive loads. Each bridge has 4 power DMOS transistor with R_{DSon} = 1.2Ω and the relative protection and control circuitry. (see fig. 3)
The 4 half bridges can be controlled indepen-dently by means of the 4 inputs IN!, IN2, IN3, IN4 and 2 enable inputs ENABLE1 and ENABLE2.
External connections are provided so that sensing resistors can be added for constant current chopper applications.

LOGIC DRIVE (*)

INPUTS			OUTPUT MOSFETS
	IN1 IN3	IN2 IN4	
EN1=EN2=H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
EN1=EN2=L	X	X	All transistor turned OFF

L = Low H = High X = Don't care
(*) True table for the two full bridges

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (fig. 1). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (see fig. 2).

Figure 1: Intrinsic Structures in the POWER MOS Transistors

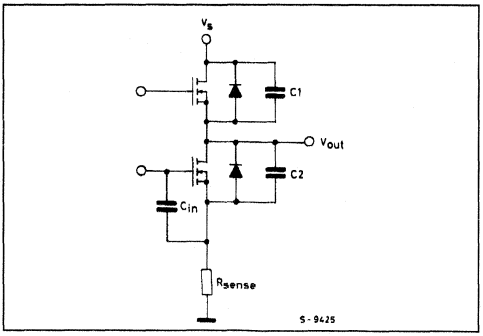
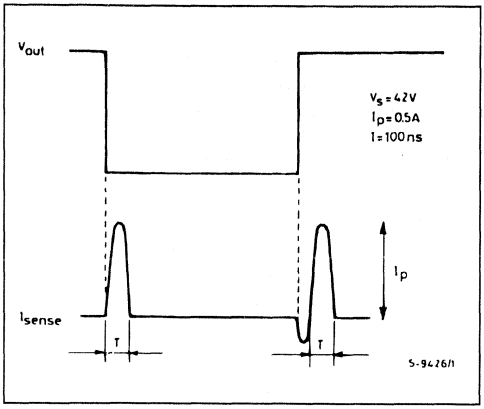


Figure 2: Current Typical Spikes on the Sensing Pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistors is ON it can be considered as a resistor $R_{DS(ON)}$ = 1.2Ω at a junction temperature of 25°C.
In this condition the dissipated power is given by :

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by :

$$P_{OFF} = V_S \cdot I_{DSS}$$

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOTSTRAP CAPACITORS

To ensure the correct driving of high side drivers

Figure 3a: Two Phase Chopping

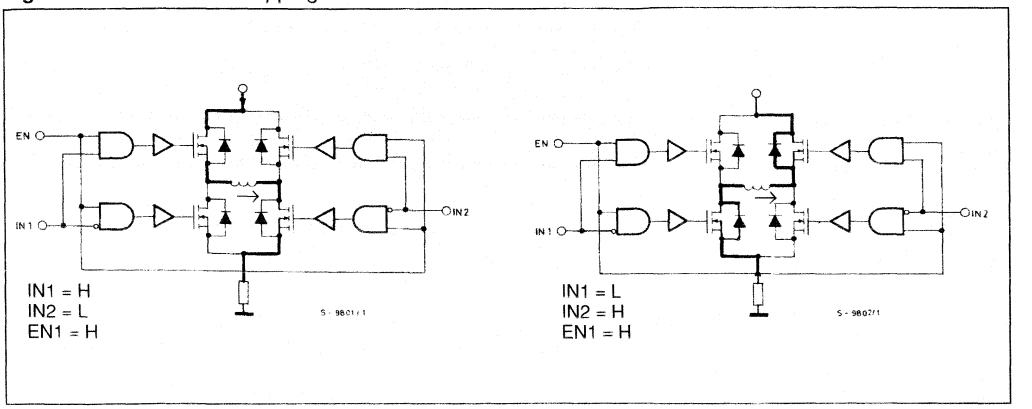


Figure 3b: One Phase Chopping

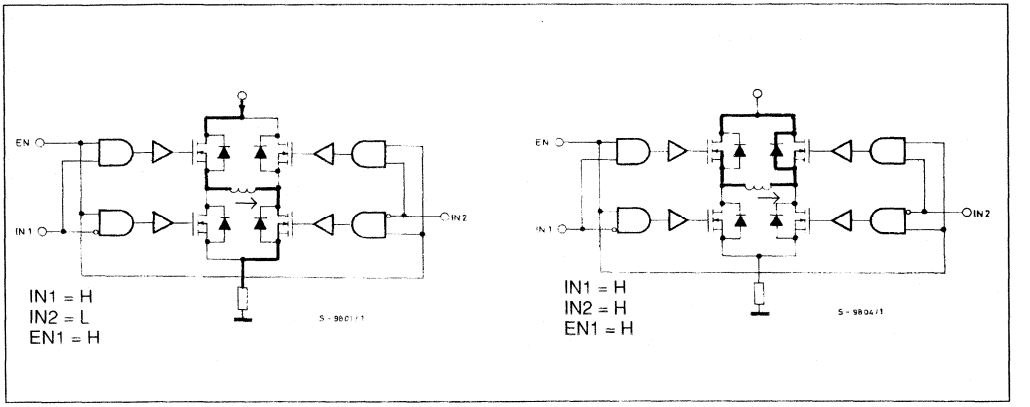
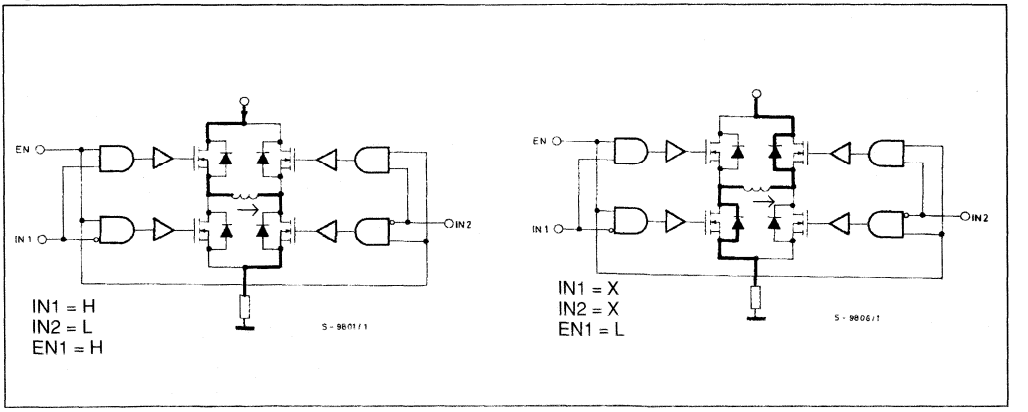
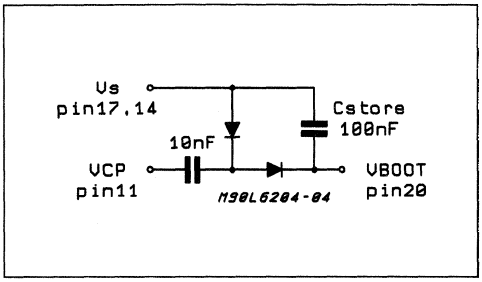


Figure 3c: Enable Chopping



a voltage higher than V_S is supplied on pin 20 (V_{boot}).
This bootstrap voltage is not needed for the lower power DMOS transistor because their sources are grounded.
To produce this voltage a charge pump method is used and mAde by two external capacitors and two diodes. It can supply the 4 driving blocks of the high side drivers. Using an external capacitor the turn-on speed of the high side driver is very high; furthermore with different capacitance values it is possible to adapt the device to different switching frequencies. It is also possible to operate two or more L6204s using only 2 diodes and 2 capacitance for all the ICs; all the Vboot pins are connected to the C_{store} capacitance while the pin 11 (VCP) of just one L6204 is connect to C_{pump}, obviously all the L6204 ICs have to be connected to the same V_S. (see fig. 4)

Figure 4



DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail-to-rail short, the logic circuits provide a dead time.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS(ON)}$. I_L for voltages less than 0.7 V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION (each bridge)

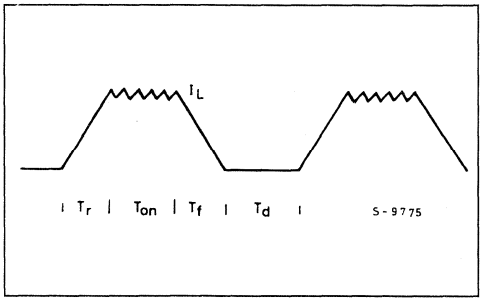
In order to achieve the high performance provided by the L6204 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat.
The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 5 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case :

$$E_{OFF/ON} = [R_{DS(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

Figure 5



ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by :

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is :

$$E_{COM} = V_S \cdot IL \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where :

T_{COM} = Commutation Time and it is assumed that ;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100$ ns
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time :

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by :

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_S \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = (E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF})_{bridge\ 1} + (E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF})_{bridge\ 2} + E_{QUIESCENT}$$

The Total Power Dissipation P_{DIS} is simply :

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall Time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

SGS-THOMSON MICROELECTRONICS

L6210

DUAL SCHOTTKY DIODE BRIDGE

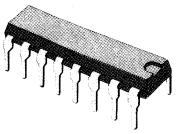
- MONOLITHIC ARRAY OF EIGHT SCHOTTKY DIODES
- HIGH EFFICIENCY
- 4A PEAK CURRENT
- LOW FORWARD VOLTAGE
- FAST RECOVERY TIME
- TWO SEPARATED DIODE BRIDGES

The L6210 is a monolithic IC containing eight Schottky diodes arranged as two separated diode bridges.

This diodes connection makes this device versatile in many applications.

They are used particular in bipolar stepper motor applications, where high efficient operation, due to low forward voltage drop and fast reverse recovery time, are required.

The L6210 is available in a 16 Pin Powerdip Package (12+2+2) designed for the 0 to 70°C ambient temperature range.



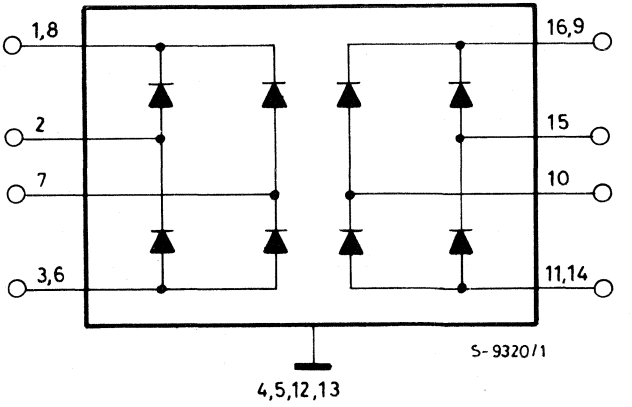
Powerdip 12+2+2

ORDERING NUMBER: L6210

ABSOLUTE MAXIMUM RATINGS

I_f	Repetitive forward current peak	2	A
V_r	Peak reverse voltage (per diode)	50	V
T_{amb}	Operating ambient temperature	70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

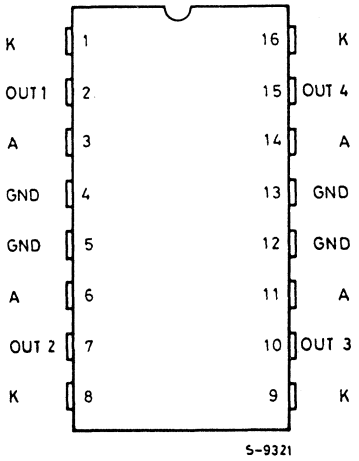
BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal impedance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal impedance junction-ambient without external heatsink	max	65	°C/W

CONNECTION DIAGRAM
(Top view)



ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Forward voltage drop	I_f = 100mA		0.65	0.8	V
		I_f = 500mA		0.8	1	
		I_f = 1A		1	1.2	
I_L	Leakage current	V_R = 40V T_{amb} = 25°C			1	mA

NOTE: At forward currents of greater than 1A, a parasitic current of approximately 10 mA may be collected by adiacent diodes.

Fig. 1 - Reverse current vs. voltage

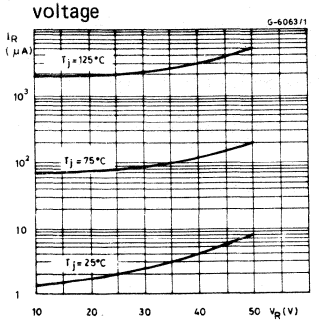
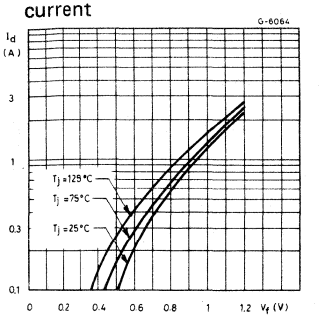


Fig. 2 - Forward voltage vs. current



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L6210 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 3 or to an external heatsink (Figure 4).

During soldering the pin temperature must not exceed 260°C and the soldering time must not be longer then 12s. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 3 - Example of P.C. board copper area which is used as heatsink

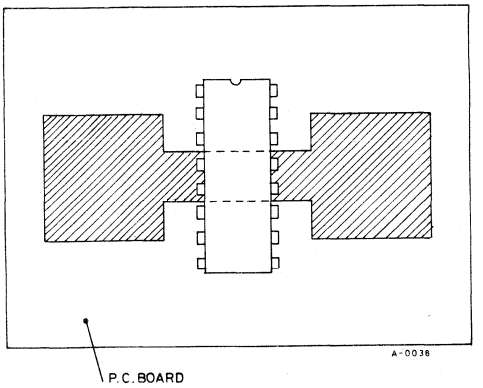
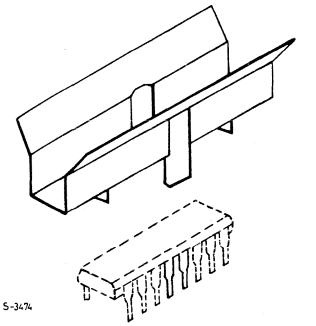


Fig. 4 - Example of an external heatsink

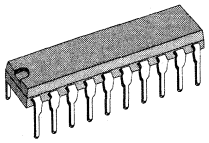


SOLENOID DRIVER + SWITCH MODE POWER SUPPLY

ADVANCE DATA

- OPERATING SUPPLY VOLTAGE UP TO 46V
- 1A POWER SUPPLY (5V)
- 5A SOLENOID DRIVER
- PRECISE ON CHIP REFERENCE VOLTAGE
- DISCONTINUOUS MODE - FREQUENCY VARIABLE
- VERY HIGH EFFICIENCY
- 1Ω OUTPUT DMOS (SMPS)
- INTERNAL CURRENT LIMIT (SMPS SECTION)
- EXTERNALLY PROGRAMMABLE SOLENOID CURRENT RISING SLOPE
- EXTERNALLY PROGRAMMABLE FIXED HYSTERESIS CONTROL
- OPTIMIZED DMOS $R_{DS\ ON}$ FOR HIGH SIDE CHOPPING

MULTIPOWER BCD TECHNOLOGY



Powerdip 16+2+2

DESCRIPTION

The L6213 is an IC containing a S.M.P.S. delivering 1A at a voltage of 5V and a section designed to drive a solenoid with a current up to 5A.

The device is realized in BCD mixed technology, which combines isolated DMOS power transistor with CMOS and Bipolar circuits on the same chip.

The SMPS section can deliver 1A DC with an output voltage of 5V, including current limiting, reset and power fail for microprocessor and thermal protection.

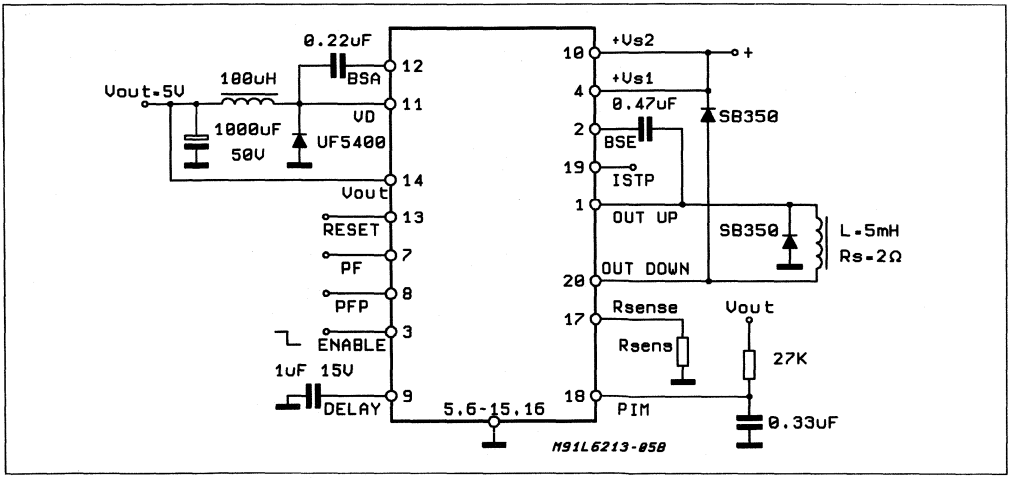
The solenoid driver section is designed for high current applications like hammer driver in electronic typewriter.

The solenoid output section contains a high side and a low side DMOS, which $R_{DS\ ON}$ are optimized for high side chopping. The current rising slope is externally programmable through an external capacitor.

The level of hysteresis of the current can be changed through an external resistor.

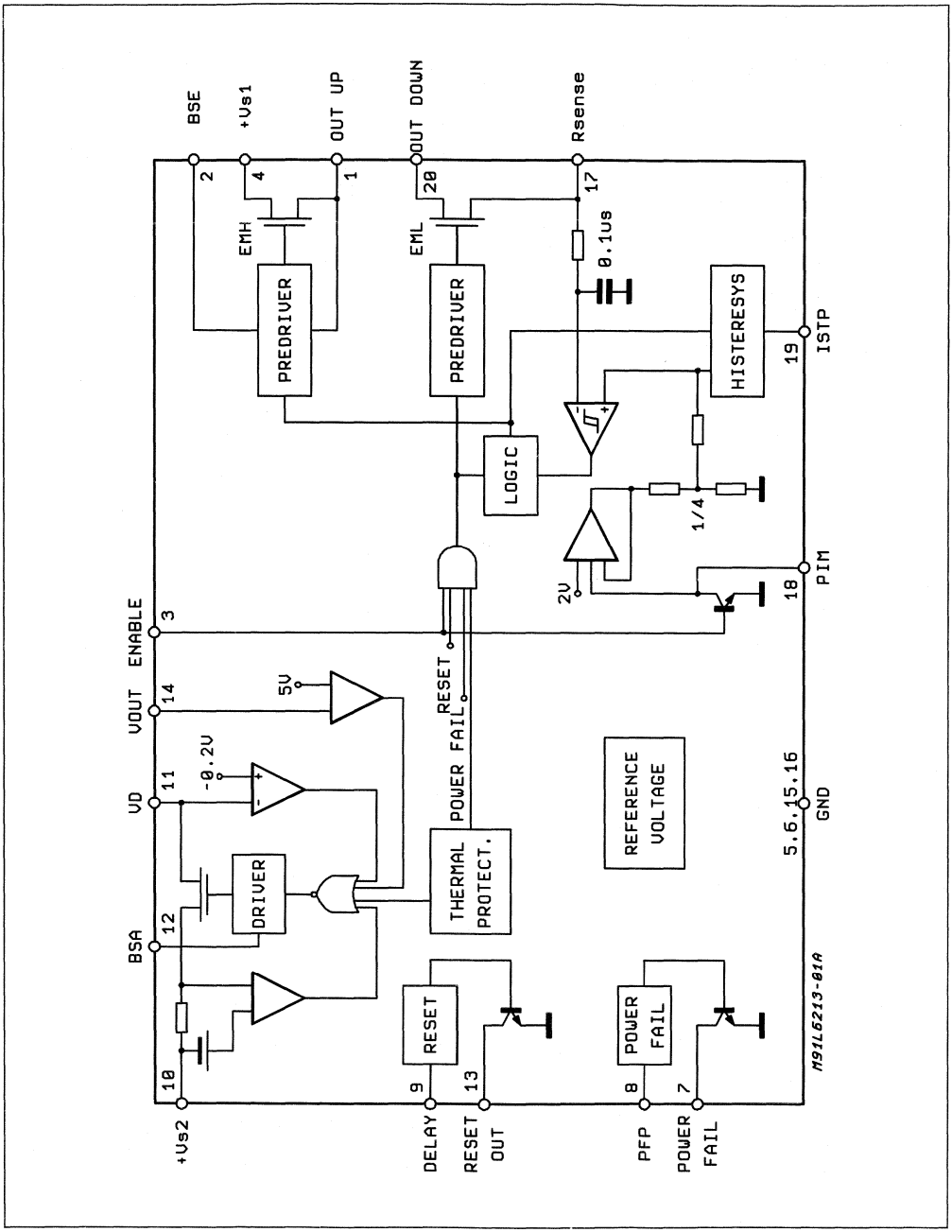
The device is supplied in Powerdip 16+2+2, and use the four center pins to conduct heat to the printed circuit.

APPLICATION CIRCUIT



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



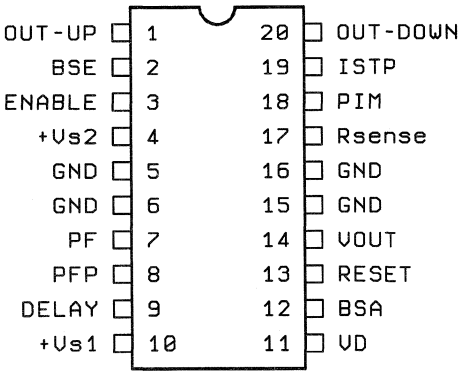
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	52	V
V_D; V_{OUT-UP}	Output Negative Voltage DC	-1.3	V
V_D	Output Negative Voltage peak at t = 0.1µs f = 100KHz	-5V	V
$V_{OUT-DOWN}$	Output Positive Voltage DC	V_S + 1.3	V
	Output Positive Voltage peak at t = 0.1µs f = 25KHz	V_S + 5	V
V_{OUT-UP}	Output Negative Voltage peak at t = 0.1µs f = 25KHz	-5	V
PFP	Input Voltage	25	V
V_O, Enable PIM	Input Voltage	7	V
Reset, PF	Output Voltage	20	V
CD, ISTP	Input Voltage	5.5	V
Out-Up Out-Down	Output Current DC = 10% T_{ON} = 3.5ms	5.5	A
T_{stg}	Storage Temperature	-50 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	60	°C/W

PIN CONNECTION (Top view)



M91L6213-02A

PIN DESCRIPTION

Nr.	Name	Description
1	Out-Up	Solenoid section upper DMOS output.
2	BSE	Solenoid section upper DMOS bootstrap. A capacitor connected between pin 2 and pin 1 ensures the efficient driving of the solenoid section upper DMOS.
3	ENABLE	Solenoid control input - TTL compatible.
4	$+V_{S1}$	Unregulated voltage input - Solenoid section.
5, 6	GND	Ground.
7	PF	Power fail output, the saturation of PF is guaranteed if VPS exceed 3V. PF is at logic 1 a time T_1 after RESET reached the high level. PF came back to logic 0 when VPS goes down under 18V. (see fig. 1)
8	PFP	Power fail programming. A resistor divider connected to VPS changes the Power fail threshold levels.
9	CD	Capacitor delay. A capacitor connected to this pin determines the Reset signal delay time t_d.
10	V_{S2}	Unregulated voltage input - SMPS sections.
11	VD	Regulator output and diode voltage control.
12	BSA	SMPS section DMOS bootstrap. A capacitor connected between pin 12 and pin 11 ensures efficient driving of SMPS DMOS.
13	RESET	Reset output. The saturation of Reset is guaranteed if VPS exceeds 3V. The Reset output reaches the logic level 1 a time delay (set by capacitor CD) after VPS has reached a rising threshold voltage. Reset reaches 0 level when VPS goes down below folling threshold.
14	V_{out}	Feed back input of the regulation loop.
15, 16	GND	Ground.
17	R_{sense}	Connection for solenoid sensing resistor.
18	PIM	Programming of solenoid current rising edge. An RC network connected to this pin determines the slope of the solenoid current rising edge.
19	ISTP	Programming of solenoid current histeresys.
20	Out-Down	Solenoid section lower DMOS output.

ELECTRICAL CHARACTERISTICS (Refer to the application circuit, T_J =25°C, I_{out} Power Supply = 50mA, VPS from 12V to 46V; unless otherwise specified.

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STEP-DOWN SECTION							
10, 4	V_i	Supply Voltage		14		46	V
14	V_o	Output Voltage	I_O = 0.05 to 1A	4.85		5.2	V
	$R_{DS\ on}$	On State Drain Resistance	T_J = 25°C; VPS = 15 to 46V		0.56	0.7	Ω
10	$t_{h\ on}$	Turn-on Threshold	VPS Rising Fig. 1	10		12	V
10	$t_{h\ off}$	Turn-off Threshold	VPS Falling Fig. 1	10		12	V
10	I_B	Input Bias Current				15	mA
11	I_{lim}	Static Current Limiting		2.2		3.4	A
2, 10	I_i	Total Input Current	ENABLE = 1, VPS = 46V, I_{load} = 0			13	mA
2, 10	I_i	Total Input Current	ENABLE = 1, VPS = 15V, I_{load} = 0			18	mA
11	t_{dp}	Protection Current Maximum Delay Time				1	µs
	t_{off}	Minimum Power off State	VPS = 46V I_O = 50mA	4.2		7.8	µs

ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER FAIL							
10	V_{thR}	Rising Threshold Voltage	PFP open Fig. 1	19.5	20	23	V
10	V_{thF}	Falling Threshold Voltage	PFP open Fig. 1	16.6	18.1	19.5	V
10	ΔV_{th}	Threshold Hysteresis	PFP open Fig. 1	0.5			V
8	I_{PFI}	Divided Internal Current				130	µA
8	$V_{th\text{-}PFP}$	Rising Threshold Voltage	VPS = 24V	1.1	1.21	1.29	V
8	$V_{th\text{-}PFP}$	Falling Threshold Voltage	VPS = 24V	0.98	1.06	1.13	V
8	$\Delta V_{th\text{-}PFP}$	Threshold Hysteresis	VPS = 24V	30			mV
7	V_{sat}	Output PF Saturation	PF current = 2.5mA VPS = 3 to 46V			0.4	V
7	I_{leak}	Output Leakage Current	VPS = 46V VPF = 20V			50	µA
7	t1	Delay to Reset	RESET High to PF high Delay Time (fig. 1)	0		1	µs
7	t2	Noise Immunity	When VPS drops to 8V for a time from 0 to t2, PF must be at 1 logic level (fig. 2)	0		1	µs
7	t3	Noise Immunity	When VPS drops to 17V for a time greater than t3, PF must be at 0 logic level (fig. 2)	4			µs
RESET							
9	I_d	Delay Source Current	V_D = 0 to 4.1V	70		140	µA
9	I_d	Delay Sink Current	VD = 4.3 to 2V	10			mA
13	V_{sat}	Output RESET Saturation	RESET Current = 2.5mA VPS = 3 to 46V			0.4	V
13	I_{leak}	Output Leakage Current	VPS = 46V RD = 4 to 5V V_{RESET} = 20V			50	µA
13	t4	Noise Immunity	When VPS drops to 10V for a time greater than t4 RESET must be at 0 logic level (fig. 1)	4			µs
SOLENOID CONTROL SECTION							
18	Vsat	Saturation Voltage	ENABLE = 1 I PIM = 5mA			0.2	V
18	I_{leak}	Leakage Current	PIM = 0.2 to 2.5V ENABLE = 0			±100	µA
18	V_{clamp}	Clamp Voltage		1.9	2	2.1	V
17		Minimum Offset Threshold	PIM = GND V_{sens} = 10mV ENABLE = 0	lower MOS must be in conduction			
17		MAximum Offset Voltage	PIM = GND V_{sens} = 50mV ENABLE = 0	lower MOS must be open			
17	V_{sense}	Static Voltage Limiting Threshold	V_{sens} going from 0 to 0.6V PIM = 3V, the EMH DMOS goes to high resistance state when V_{sens} is within: (see Block Diagram)	0.475	0.5	0.525	V
17		Maximum Delay Time				1	µs
	t_p	Protection Time		2		4	µs
	EMH R_{on}	On State Drain to Source Resistance	T_j = 25°C, VPS 15 to 46V		0.35	0.45	Ω
	EML R_{on}	On State Drain to Source Resistance	Tj = 25°C, VPS 15 to 46V		0.28	0.4	Ω
17	V_{sense}	Vsense Hysteresis	IST = Open IST = 0.75V IST = 3V	35 15 80	50 25 100	65 35 120	mV mV mV

Figure 1: Power Fail and Reset Static Operation. (PFP open)

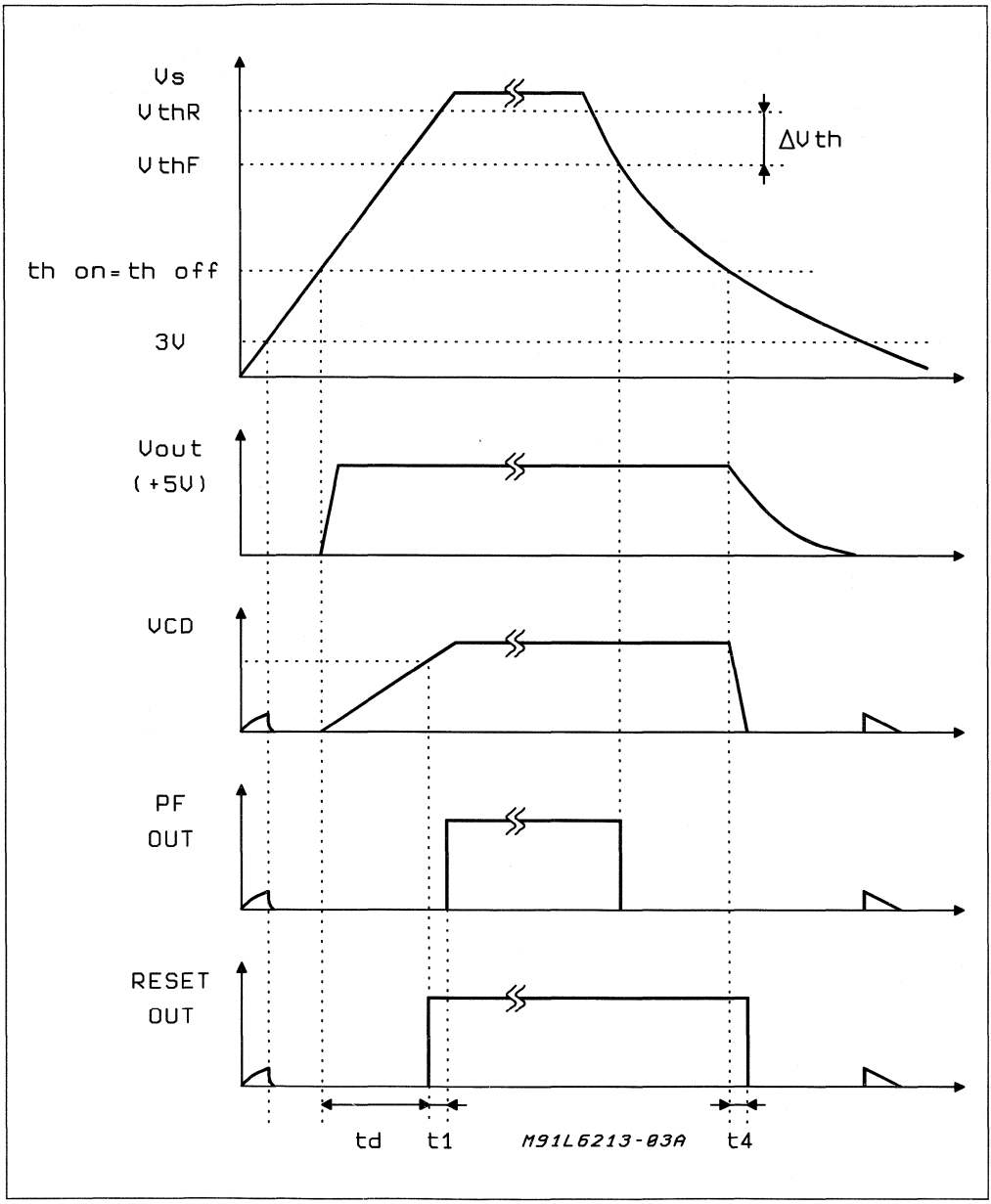
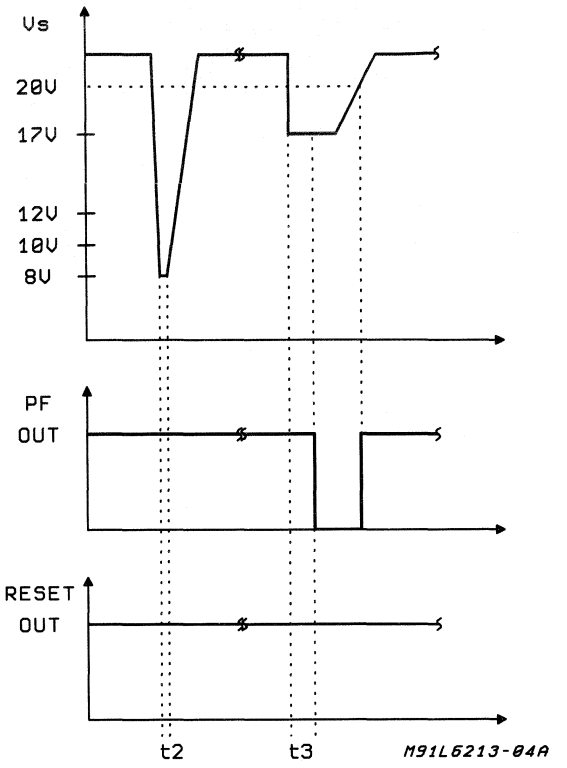


Figure 2: Power Fail and Reset Noise Immunity and Dynamic Operation.



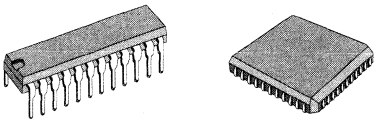
SGS-THOMSON MICROELECTRONICS

L6219

STEPPER MOTOR DRIVER

ADVANCE DATA

- ABLE TO DRIVE BOTH WINDINGS OF BIPOLAR STEPPER MOTOR
- OUTPUT CURRENT UP TO 750mA EACH WINDING
- WIDE VOLTAGE RANGE 10V TO 50V
- HALF-STEP, FULL-STEP AND MICROSTEPPING MODE
- BUILT-IN PROTECTION DIODES
- INTERNAL PWM CURRENT CONTROL
- LOW OUTPUT SATURATION VOLTAGE
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- INTERNAL THERMAL SHUTDOWN



Powerdip 20+2+2 **PLCC44**

ORDERING NUMBERS:

L6219 L6219D

DESCRIPTION

The L6219 is a bipolar monolithic integrated circuits intended to control and drive both winding of a bipolar stepper motor or bidirectionally control two DC motors.

The L6219 with a few external components form a complete control and drive circuit for LS-TTL or microprocessor controlled stepper motor system.

The power stage is a dual full bridge capable of sustaining 50V and including four diodes for current recirculation.

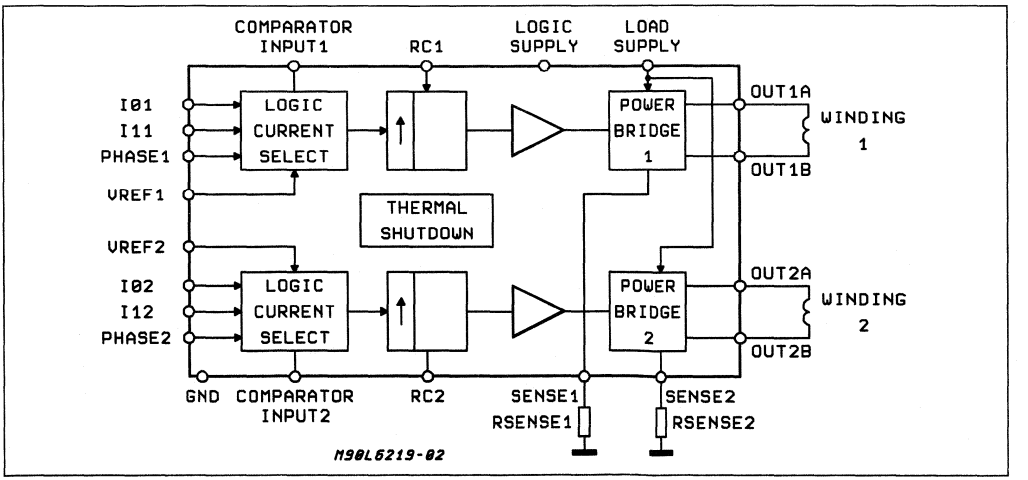
A cross conduction protection is provided to avoid simultaneous cross conduction during switching current direction.

An internal pulse-width-modulation (PWM) controls the output current to 750mA with peak start-up current up to 1A.

Wide range of current control from 750mA (each bridge) is permitted by means of two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction.

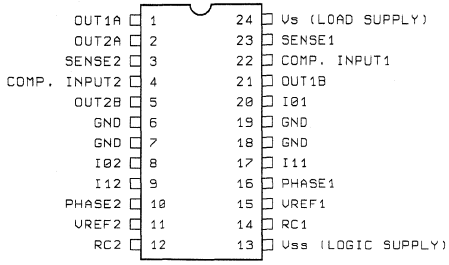
A thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

BLOCK DIAGRAM

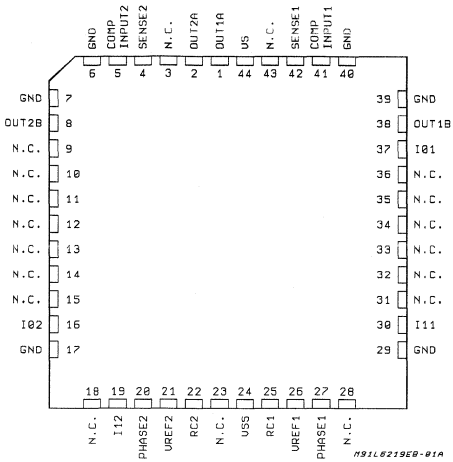


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS (Top view)



Powerdip



PLCC44

PIN FUNCTIONS

PLCC (*)	PDIP	Name	Function
1;2	1;2	OUTPUT A	See pins 5;21
4;42	3;23	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor
5;41	4;22	COMPARATOR INPUT	Input connected to the comparators. The voltage across the sense resistor is feedback to this input throught the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_T C_T (t_{off} = 1.1 R_T C_T). See fig. 1.
8;38	5;21	OUTPUT B	Output Connection. The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
6;7;17	6;19	GROUND	See pins 7;18
29;39; 40	7;18	GROUND	Ground Connection. With pins 6 and 19 also conducts heat from die to printed circuit copper.
16;37	8;20	INPUT 0	See INPUT 1 (pins 9;17)
19;30	9;17	INPUT 1	These pins and pins 8;20 (INPUT 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See Funcional Description.
20;27	10;16	PHASE	This TTL-compatible logic inputs sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
21;26	11;15	REFERENCE VOLTAGE	A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
22;25	12;14	RC	A parallel RC network connected to this pin sets the OFF time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators (t_{off} = 1.1 R_T C_T).
24	13	V_{ss} - LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry
44	24	Vs - LOAD SUPPLY	Supply Voltage Input for the Output Stages.

(*) Pins: 3, 9,10,11,12,13,14,15,18,23,28,31,32,33,34,35,36,43 are Not Connected.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
I_o	Output Current (peak)	±1	A
I_o	Output Current (continuous)	±0.75	A
V_{SS}	Logic Supply Voltage	7	V
V_{IN}	Logic Input Voltage Range	-0.3 to +7	V
V_{sense}	Sense Output Voltage	1.5	V
T_J	Junction Temperature	+150	°C
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Description		PLCC	PDIP	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max.	12	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	45 (*)	60 (*)	°C/W

(*) With minimized copper area.

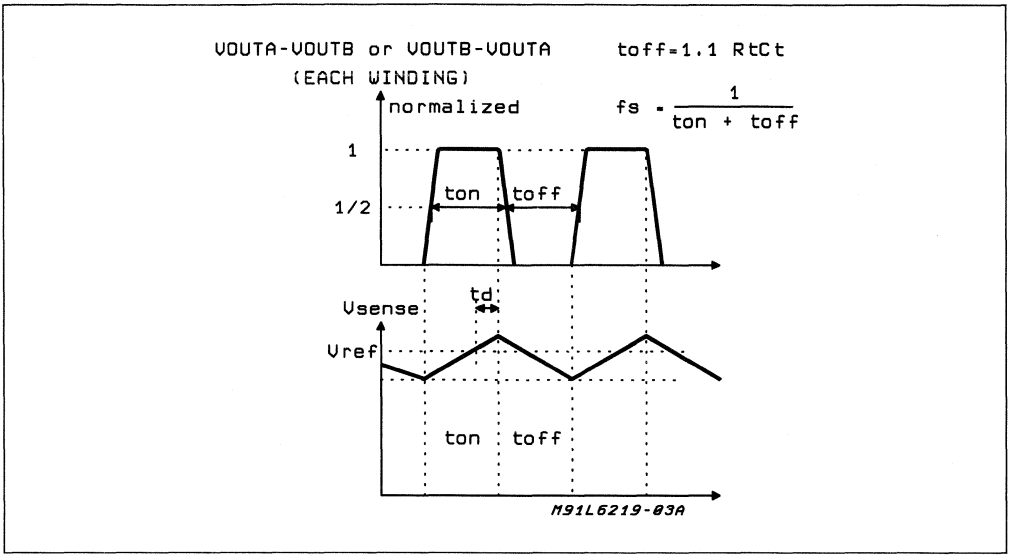
ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_S = 50V, V_{SS} = 4.75V to 5.25V, V_{REF} = 5V; unless otherwise specified) See fig. 3.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT DRIVERS (OUT_A or OUT_B)						
V_S	Motor Supply Range		10		50	V
I_{CEX}	Output Leakage Current	V_{OUT} = Vs V_{OUT} = 0	- -	<1 <-1	50 -50	µA µA
$V_{CE(sat)}$	Output Saturation Voltage	Sink Driver, I_{OUT} = +500mA Sink Driver, I_{OUT} = +750mA Source Driver, I_{OUT} = -500mA Source Driver, I_{OUT} = -750mA	- - - -	0.3 0.7 1.1 1.3	0.6 1 1.4 1.6	V V V V
I_R	Clamp Diode Leakage Current	V_R = 50V	-	<1	50	µA
V_F	Clamp Diode Forward Voltage	Sink Diode Source Diode I_F =750mA		1 1	1.5 1.5	V V
$I_{S(on)}$	Driver Supply Current	Both Bridges ON, No Load	-	8	15	mA
$I_{S(off)}$	Driver Supply Current	Both Bridges OFF	-	6	10	mA
CONTROL LOGIC						
$V_{IN(H)}$	Input Voltage	All Inputs	2.4	-	-	V
$V_{IN(L)}$	Input Voltage	All Inputs	-	-	0.8	V
$I_{IN(H)}$	Input Current	VIN = 2.4V	-	<1	20	µA
$I_{IN(L)}$	Input Current	VIN = 0.84V	-	-3	-200	µA
V_{REF}	Reference Voltage	Operating	1.5	-	7.5	V
$I_{SS(ON)}$	Total Logic Supply Current	I_o = I_1 = 0.8V, No Load	-	54	64	mA
$I_{SS(OFF)}$	Total Logic Supply Current	I_o = I_1 = 2.4V, No Load	-	10	14	mA
COMPARATORS						
V_{REF} / V_{sense}	Current Limit Threshold (at trip point	I_o = I_1 = 0.8V	9.5	10	10.5	-
		I_o = 2.4V, I_1 = 0.8V	13.5	15	16.5	-
		I_o = 0.8V, I_1 = 2.4V	25.5	30	34.5	-
t_{off}	Cutoff Time	Rt = 56KΩ C_t = 820pF	-	50		µs
t_d	Turn Off Delay	Fig. 1	-	1		µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PROTECTION						
T_J	Thermal Shutdown Temperature		-	170	-	°C

Figure 1



FUNCTIONAL DESCRIPTION

The circuit is intended to drive both windings of a bipolar stepper motor.
The peak current control is generated through switch mode regulation.
There is a choice of three different current levels with the two logic inputs I_{01} - I_{11} for winding 1 and I_{02} - I_{12} for winding 2.
The current can also be switched off completely

Input Logic (I_0 and I_1)

The current level in the motor winding is selected with these inputs. (See fig. 2)
If any of the logic inputs is left open, the circuit will treat it has a high level input.

I_o	I_1	Current Level
H	H	No Current
L	H	Low Current 1/3 I_o max
H	L	Medium Current 2/3 I_o max
L	L	Maximum Current I_o max

Phase

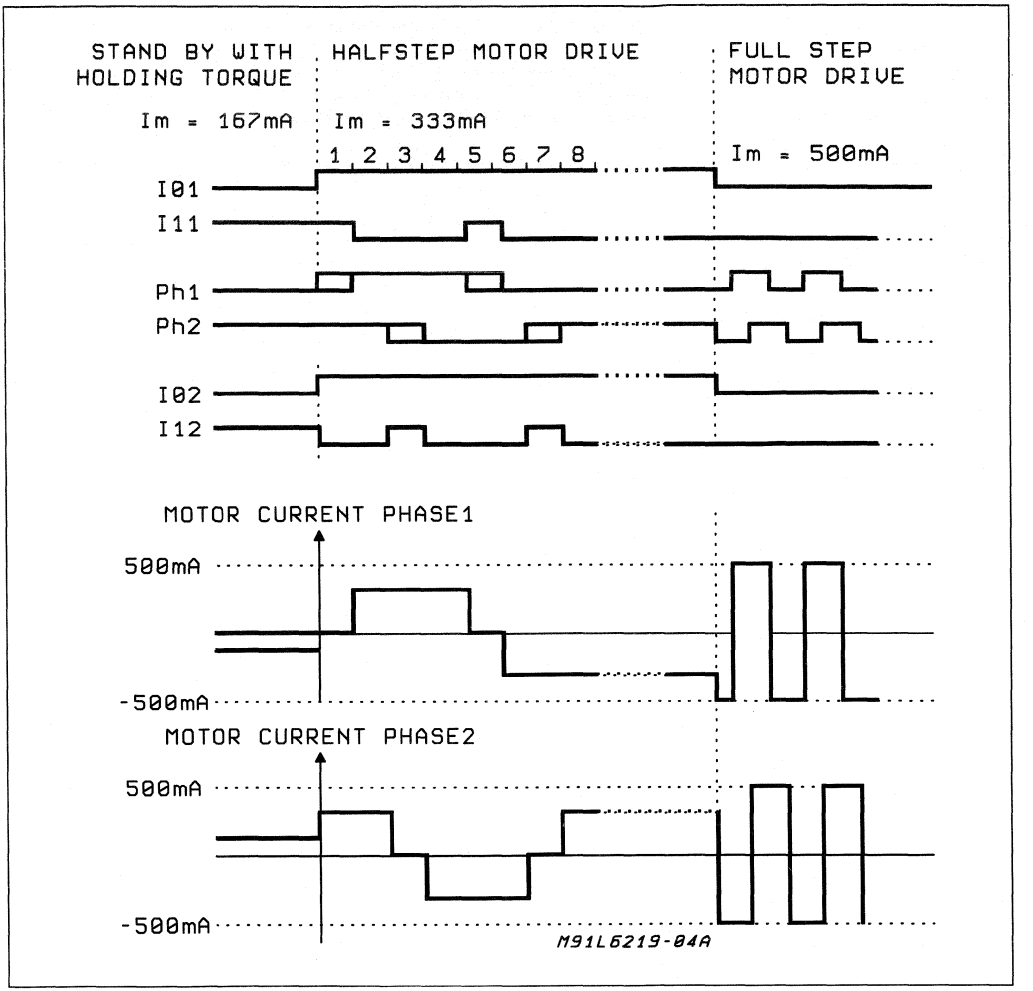
This input determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift.
High level on the PHASE input causes the motor current flow from Out A through the winding to Out B

Current Sensor

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators.
Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_o and I_1.
The motor current flows through the sensing resistor R_S.
When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator goes high, which triggers the pulse generator.
The max peak current I_{max} can be defined by:

$$I_{max} = \frac{V_{ref}}{10\ R_s}$$

Figure 2: Principle Operating Sequence



Single-pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off}, which is determined by the time components R_t and C_t.

$$t_{off} = 1.1 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.
If a new trigger signal should occur during t_{off}, it is ignored.

Output Stage

The output stage contains four Darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.
The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.
It should be noted however, that is not permitted to short circuit the outputs.
Internal circuitry is added in order to increase the accuracy of the motor current particularly with low current levels.

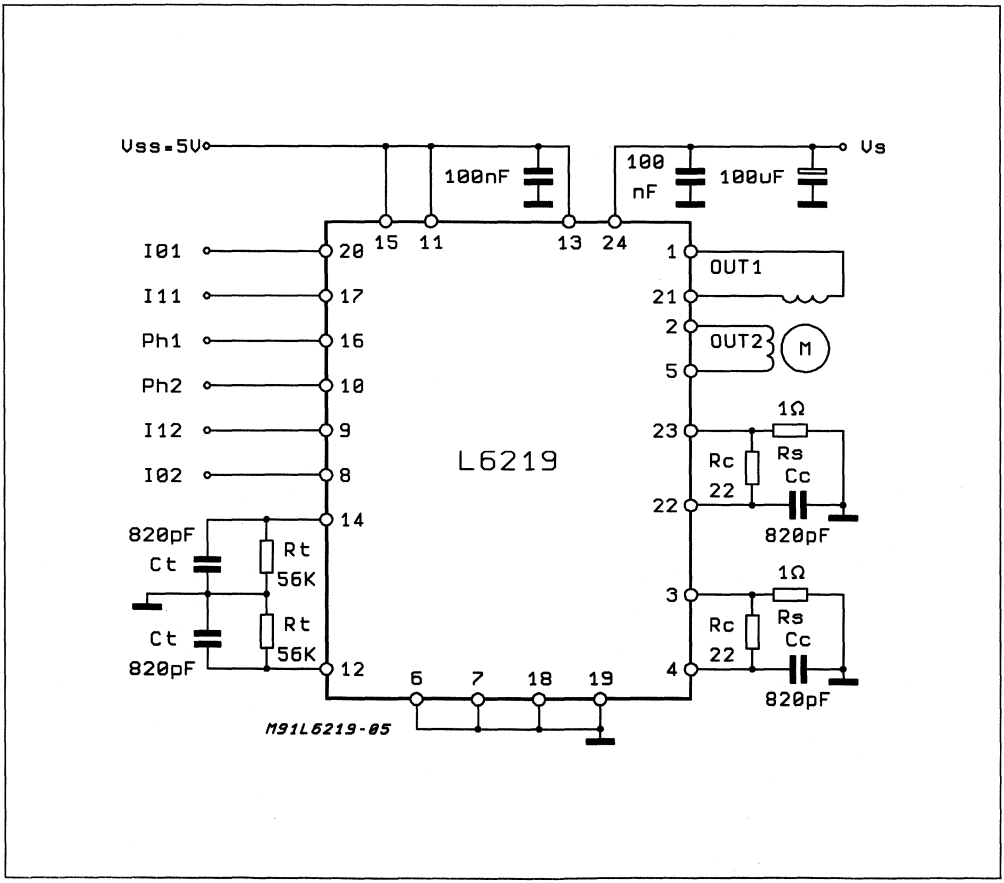
V_S, V_{SS}, V_{Ref}
The circuit will stand any order of turn-on or turn-off the supply voltages V_S and V_{SS}. Normal dV/dt values are then assumed.
Preferably, V_{Ref} should be tracking V_{SS} during power-on and power-off if V_S is established.

APPLICATION INFORMATIONS (Note 1)
Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.
Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.
Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100nF capacitor, located near the package between power line and ground.
The ground lead between R_s, and circuit GND should be kept as short as possible.
A typical Application Circuit is shown in Fig. 3.
Note that C_t must be NPO type or similar else.
To sense the winding current, paralleled metal film resistors are recommended (R_s)

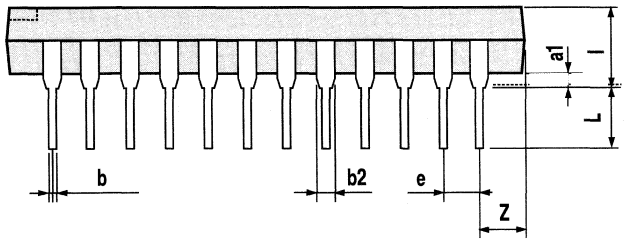
Note 1 - Other information is available as "Smart Power Development System":
Test board HWL6219 (Stepper driver)
Software SWL6219 (Floppy disc)

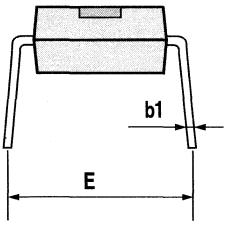
Figure 3: Typical Application Circuit. (Pin out referred to DIP24 package)

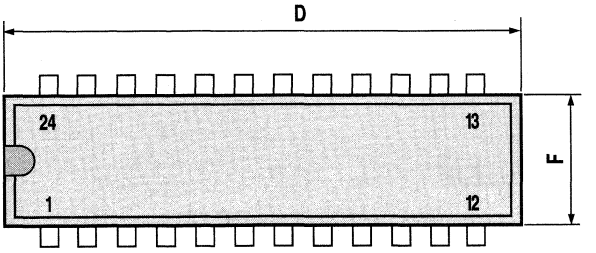


DIP24 (20+2+2) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.38			0.015		
b	0.41		0.51	0.016		0.020
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	1.40	1.52	1.65	0.055	0.060	0.065
D			30.23			1.19
E		7.62			0.300	
e		2.54			0.100	
F			6.86			0.270
I			4.32			0.170
L	3.18			0.125		

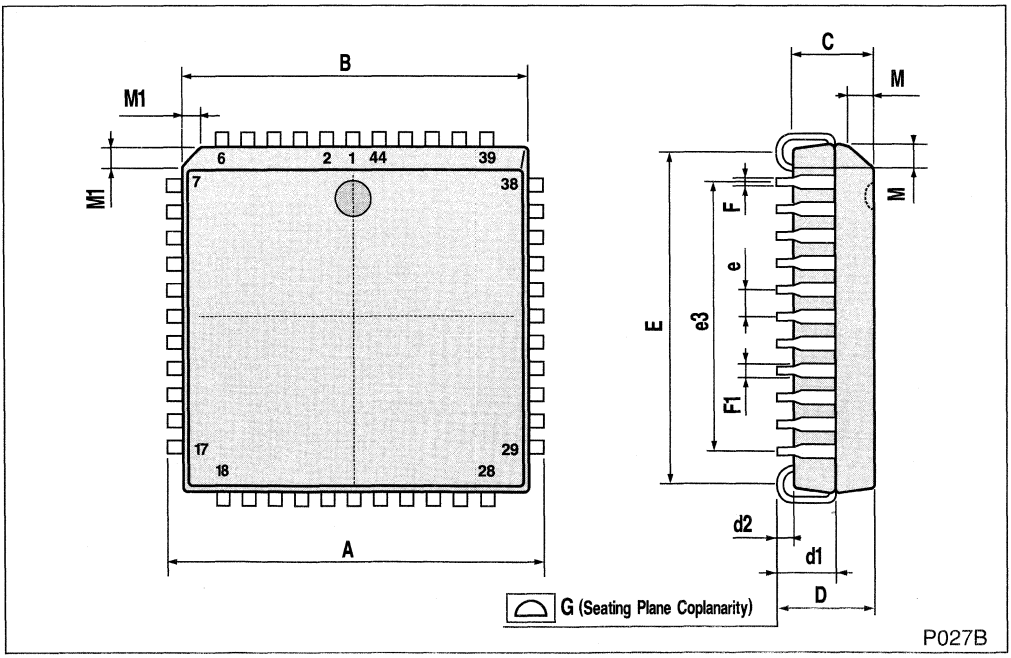






PLCC44 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



L6220
L6220N

QUAD DARLINGTON SWITCHES

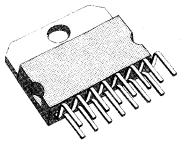
- TWO NON INVERTING + TWO INVERTING INPUTS WITH INHIBIT
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

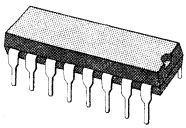
The L6220 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common inhibit input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6220 mounted in a Powerdip 12 + 2 + 2 package and the L6220N mounted in a 15-lead Multiwatt package.



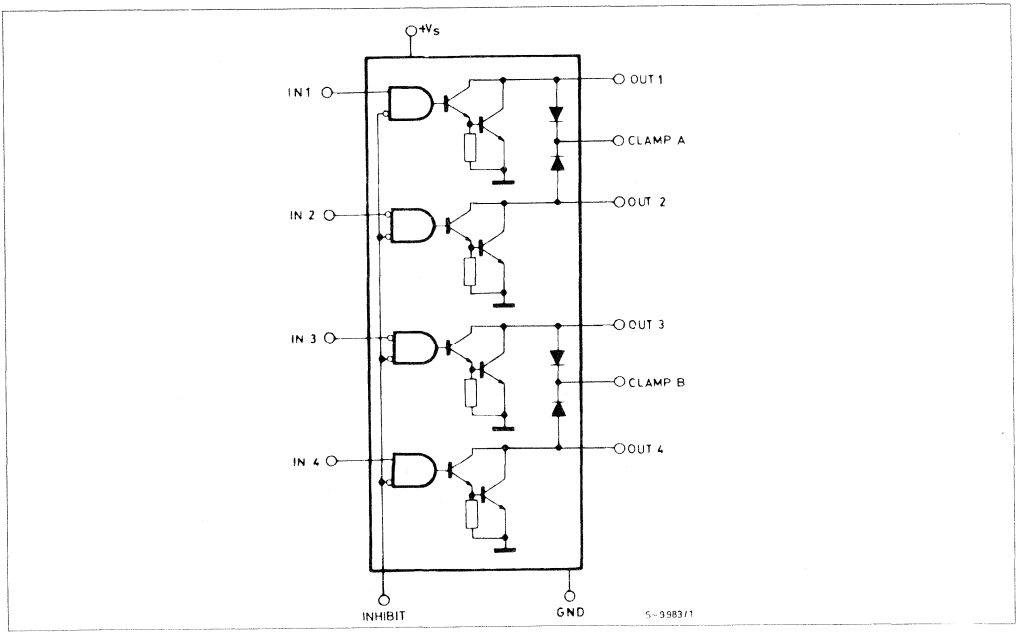
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6220
L6220N

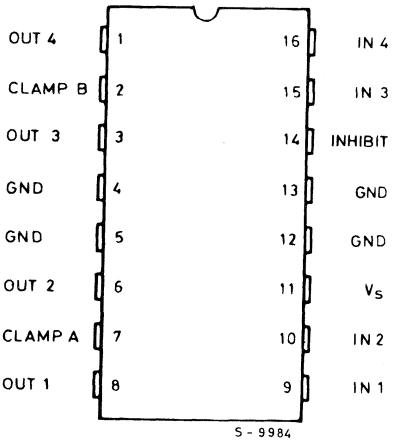
BLOCK DIAGRAM



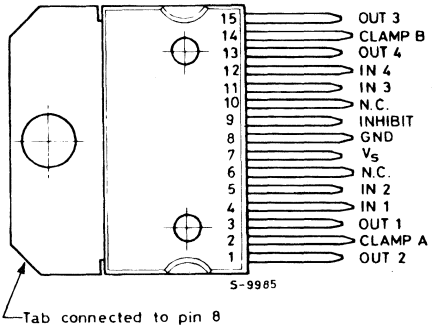
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Ouput Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{INH}	Input Voltage, Inhibit Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (Powerdip) at T_{case} = 90 °C (Multiwatt) at T_{amb} = 70 °C (Powerdip) at T_{amb} = 70 °C (Multiwatt)	4.3 20 1 2.3	W W W W

CONNECTION DIAGRAMS (top views)



L6220 (Powerdip)



L6220N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt–15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	-
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	-	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Inhibit	Input 1, 4	Power Out	Inhibit	Inputs 2, 3	Power Out
L	H	ON	L	L	ON
L	L	OFF	L	H	OFF
H	X	OFF	H	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
INHIBIT	Inhibit Input to all Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS Refer to the test circuits Fig. 1 to Fig. 9 (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

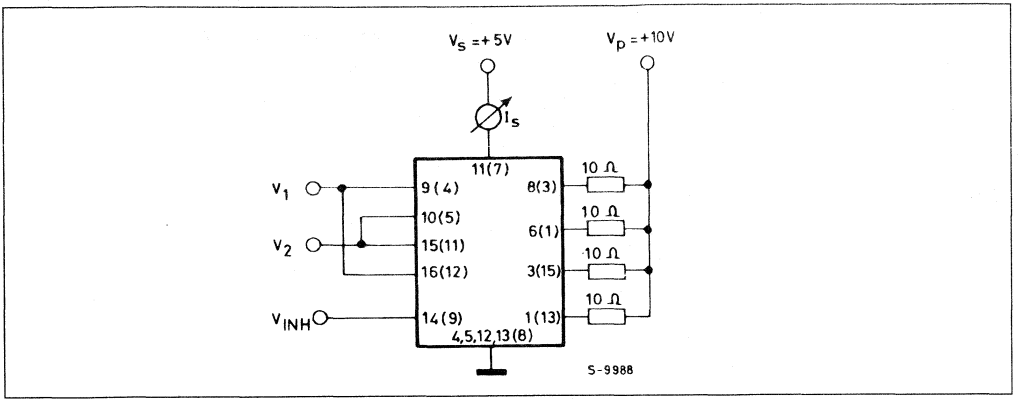
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage		4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A			20	mA
		All Outputs OFF			20	mA
$V_{CE\ (sus)}$	Output Sustaining Voltage	I_C =100 mA $V_{INH} = V_{INH}H$	46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50 V $V_{IN\ 1..4} = V_{IN}H$			1	mA
$V_{CE\ (sat)}$	Collector Emitter Saturation Voltage (one output on ; all others off.)	V_s = 4.5 V, $V_{IN\ 2..3} = V_{IN}L$, $V_{INH} = V_{INH}L$, I_C = 0.6 A			1	V
		V_s = 4.5 V, $V_{IN\ 2..3} = V_{IN}L$, $V_{INH} = V_{INH}L$, I_C = 1 A			1.2	V
		V_s = 4.5 V, $V_{IN\ 2..3} = V_{IN}L$, $V_{INH} = V_{INH}L$, I_C = 1.8 A			1.6	V
$V_{IN}L$, $V_{INH}L$	Input Low Voltage				0.8	V
$I_{IN}L$, $I_{INH}L$	Input Low Current	$V_{IN} = V_{IN}L$ $V_{INH} = V_{INH}L$			− 100	µA
$V_{IN}H$, $V_{INH}H$	Input High Voltage		2.0			V
$I_{IN}H$, $I_{INH}H$	Input High Current	$V_{IN} = V_{IN}H$ $V_{INH} = V_{INH}H$			± 10	µA
I_R	Clamp Diode Leakage Current	V_R = 50 V $V_{INH} = V_{INH}H$			100	µA
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.6	V
		I_F = 1.8 A			2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5 V R_L = 10 Ω			2	µs
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5 V R_L = 10 Ω			5	µs
ΔI_s	Logic Supply Current Variation	V_{IN} = 5 V V_{EN} = 5 V, I_{out} = − 500 mA for each Channel			150	mA

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic Supply Current.



Set V_1 = 4.5V, V_2 = 0.8V, V_{INH} = 4.5V or V_1 = 0.8V, V_2 = 4.5V, V_{INH} = 0.8 for I_S (all outputs off).
Set V_1 = 2V, V_2 = 0.8V, V_{INH} = 0.8V for I_S (all outputs on).

Figure 2 : Output Sustaining Voltage.

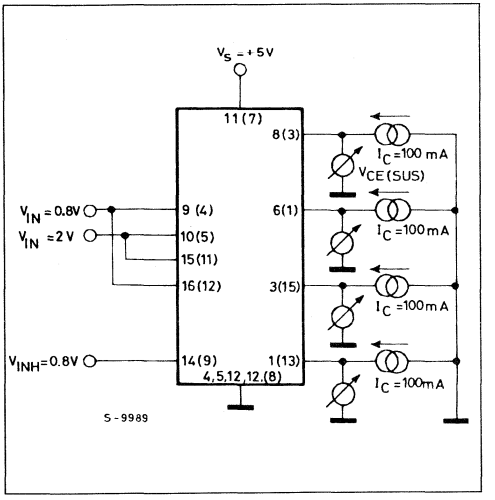


Figure 3 : Output Leakage Current.

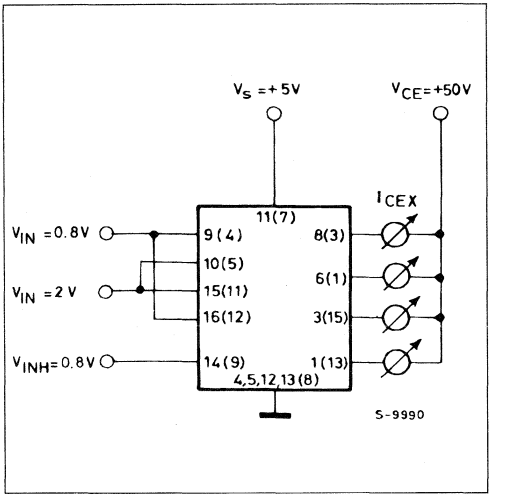


Figure 4 : Collector-emitter Saturation Voltage.

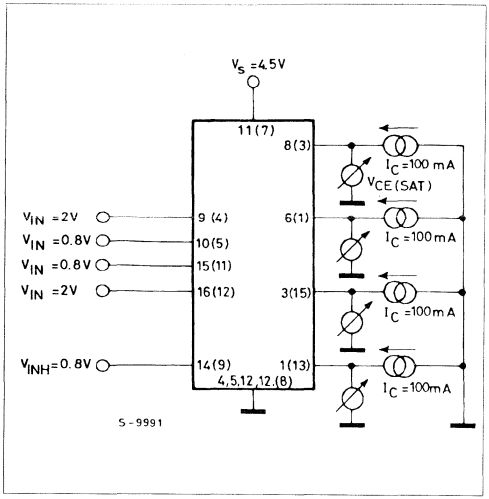
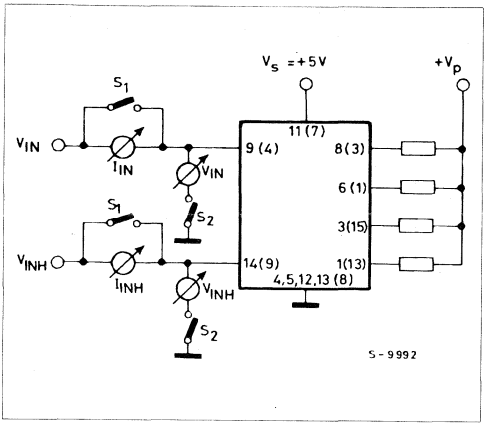


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{INH} = 0.8V for I_{IN} L, I_{INH} L
Set S_1, S_2 open, V_{IN}, V_{INH} = 2V for I_{IN} H, I_{INH} H
Set S_1, S_2 close, V_{IN}, V_{INH} = 0.8V for V_{IN} L, V_{INH} L
Set S_1, S_2 close, V_{IN}, V_{INH} = 2V for V_{IN} H, V_{INH} H.

Figure 6 : Clamp Diode Leakage Current.

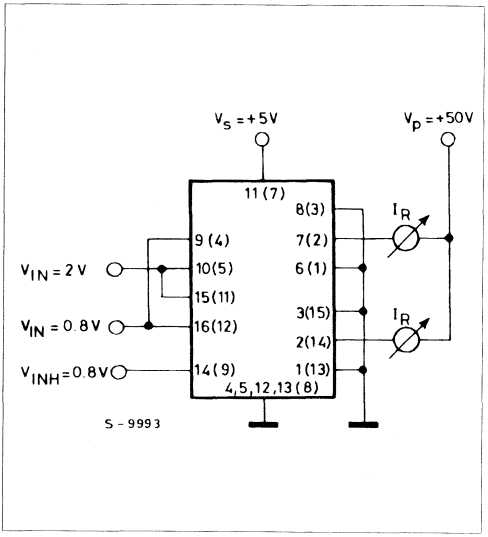


Figure 7 : Clamp Diode Forward Voltage.

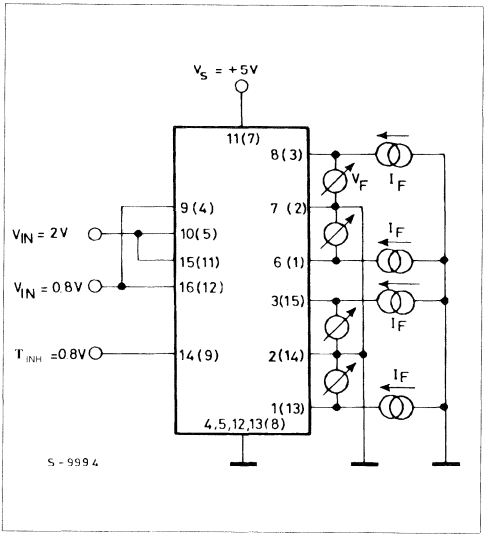


Figure 8 : Switching Times Test Circuit.

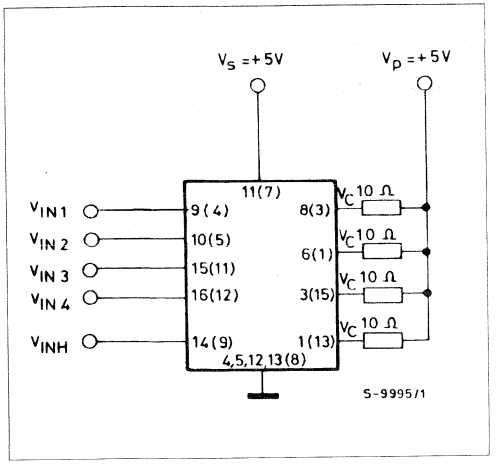


Figure 9 : Switching Times Waveforms.

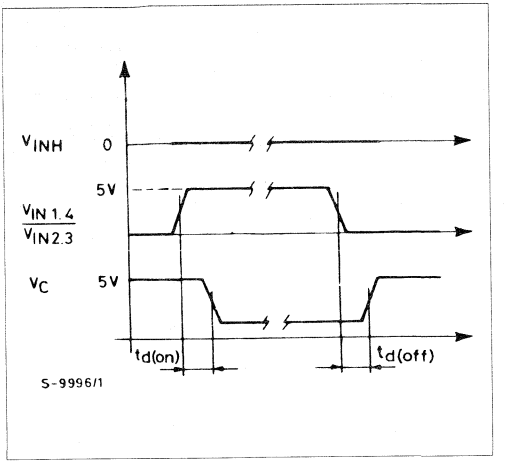


Figure 10 : Collector Saturation Voltage vs. Collector Current.

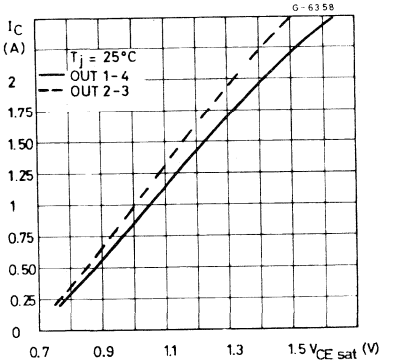


Figure 11 : Free- wheeling Diode Forward Voltage vs. Diode Current.

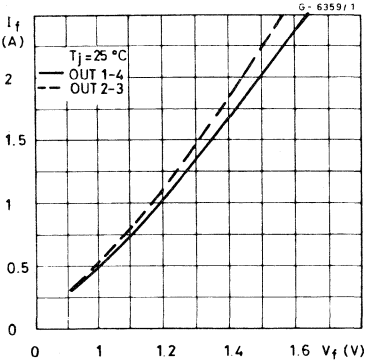


Figure 12 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1 A.

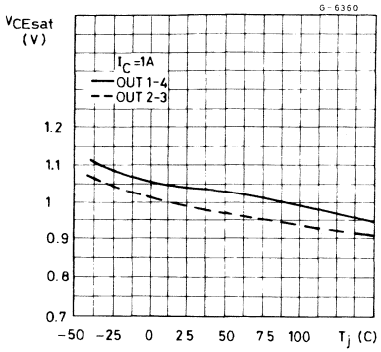


Figure 13 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_f = 1A .

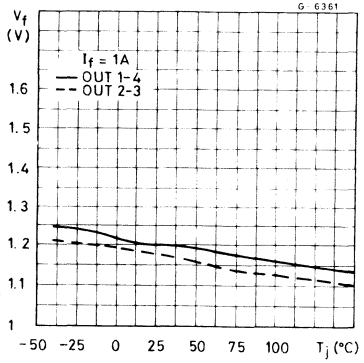


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1.8A.

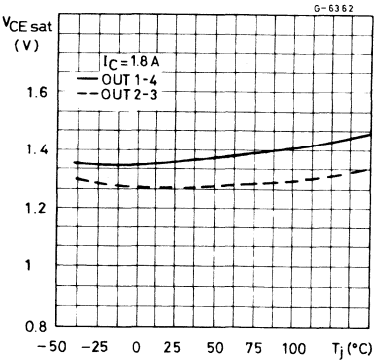


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1.8A.

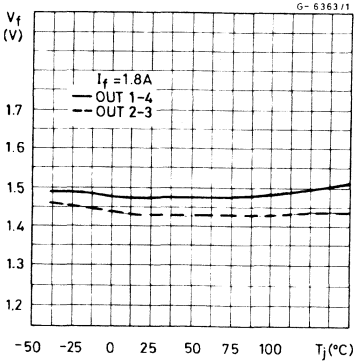


Figure 16.

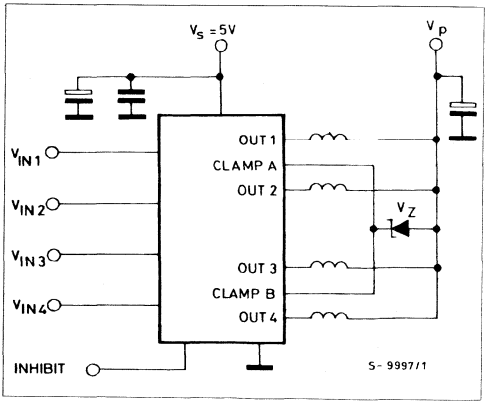
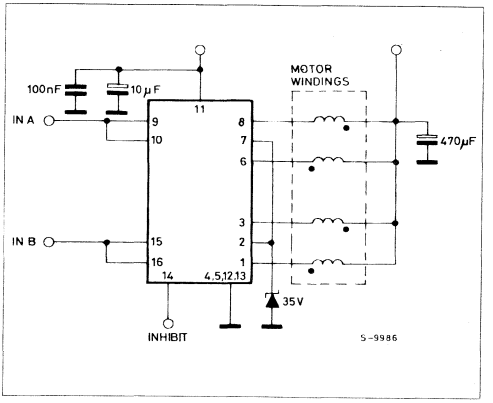


Figure 17 : Unipolar Stepper Motor Driver.



APPLICATION INFORMATION

When inductive loads are driven by L6220/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (Fig. 16). For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.
2) The instantaneous power must be limited to avoid the reverse second breakdown.

The particular internal logic allows an easier full step driving using only two input signals.

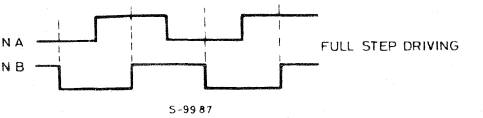


Figure 18 : Allowed Peak Collector-current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6220).

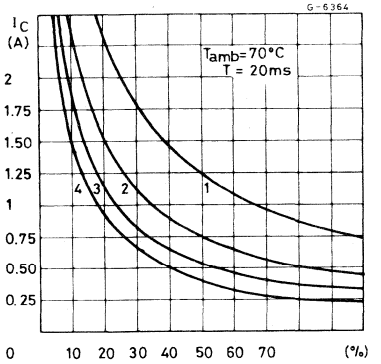
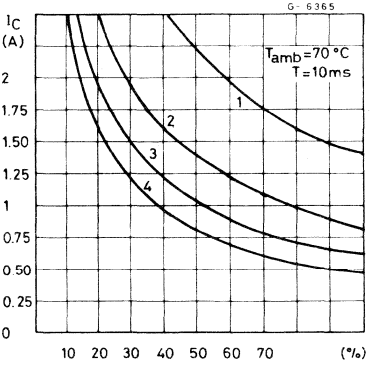


Figure 19 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6220N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6220 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 20) or to an external heatsink (Fig. 21).

The diagram of figure 22 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 20 : Example of P.C. Board Copper area which is used as Heatsink.

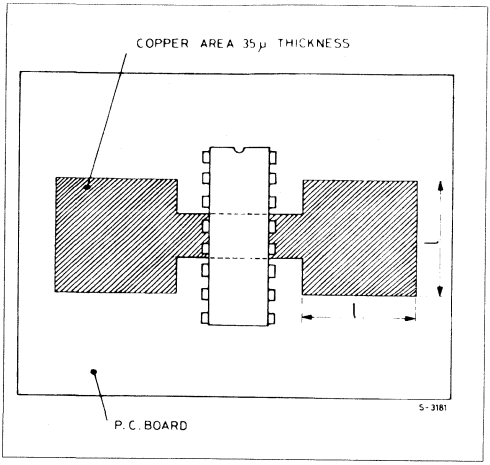


Figure 21 : External Heatsink Mounting Example.

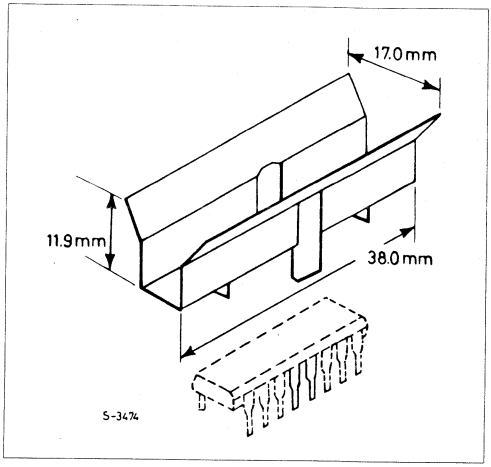


Figure 22 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

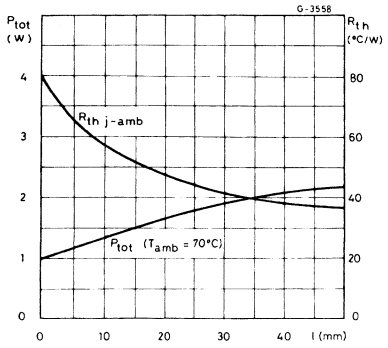
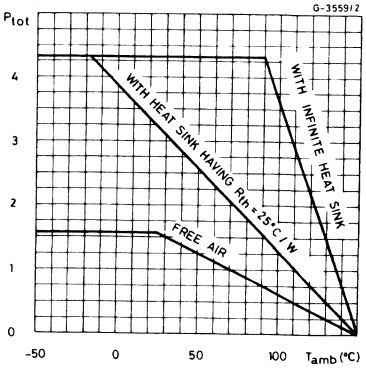


Figure 23 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



L6221A
L6221N

QUAD DARLINGTON SWITCH

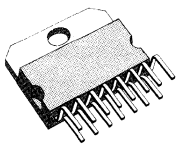
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

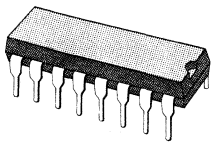
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6221A mounted in a Powerdip 12 + 2 + 2 package and the L6221N mounted in a 15--lead Multiwatt package.



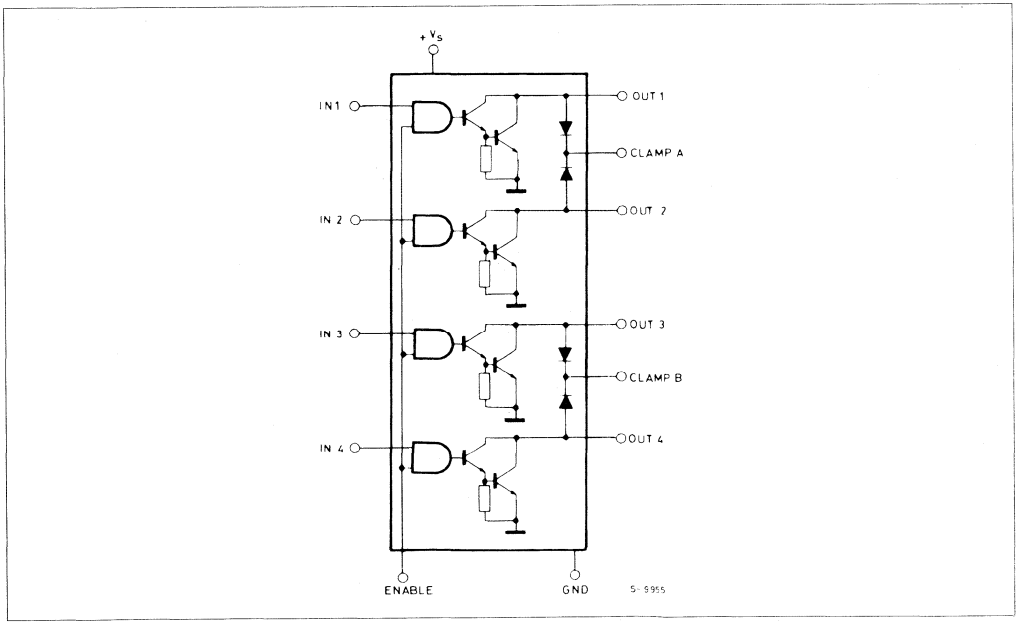
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6221A
L6221N

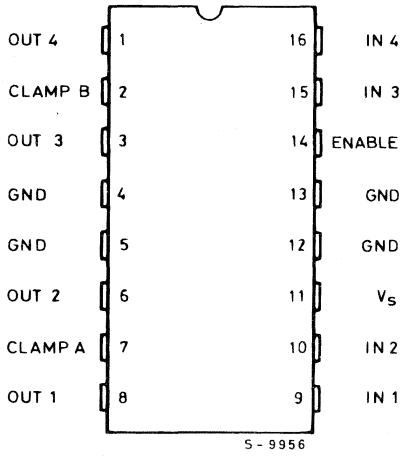
BLOCK DIAGRAM



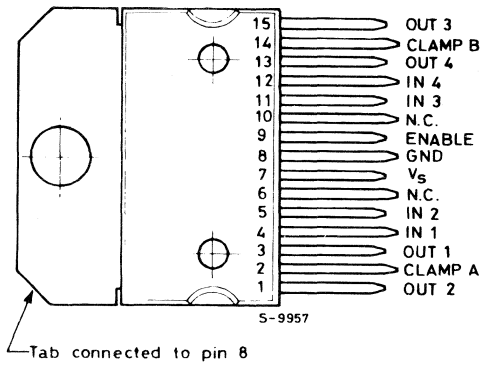
ABSOLUTE MAXIMUM RATINGS

V_o	Output Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{EN}	Input Voltage, Enable Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (powerdip) at T_{case} = 90 °C (multiwatt) at T_{amb} = 70 °C (powerdip) at T_{amb} = 70 °C (multiwatt)	4.3 20 1 2.3	W W W W

PIN CONNECTIONS (top views)



L6221A (Powerdip)



L6221N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt-15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS Refer to the test circuit to Fig. 1 to Fig. 9
(VS = 5V, Tamb = 25 °C unless otherwise specified)

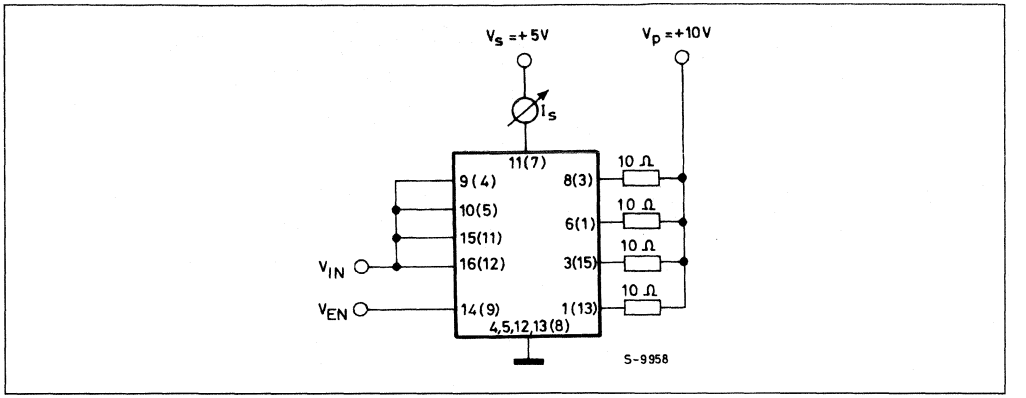
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage			4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A				20	m A
		All Outputs OFF				20	m A
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = V_{INL} V_{EN} = V_{ENH} I_C = 100 mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{EN} = V_{ENH} V_{IN} = V_{INL}				1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	V_s = 4.5V V_{IN} = V_{INH} V_{EN} = V_{ENH}	I_C = 0.6 A			1	V
			I_C = 1 A			1.2	V
			I_C = 1.8 A			1.6	V
V_{INL}, V_{ENL}	Input Low Voltage					0.8	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN} = V_{INL} V_{EN} = V_{ENL}				– 100	µ A
V_{INL}, V_{ENH}	Input High Voltage			2.0			V
I_{INH} , I_{ENH}	Input High Current	V_{IN} = V_{INH} V_{EN} = V_{ENH}				± 10	µ A
I_R	Clamp Diode Leakage Current	V_R = 50 V V_{EN} = V_{ENH} V_{IN} = V_{INL}				100	µ A
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.6	V
		I_F = 1.8 A				2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5V R_L = 10Ω				2	µ s
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5V R_L = 10Ω				5	µ s
ΔI_s	Logic Supply Current Variation	V_{IN} = 5V V_{EN} = 5V I_{out} = – 500 mA for Each Channel				150	m A

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic supply current.



Set V_{IN} = 4.5V, V_{EN} = 0.8V, or V_{IN} = 0.8V, V_{EN} = 4.5V, for I_S (all outputs off)
Set V_{IN} = 2V, V_{EN} = 2V, for I_S (all outputs on)

Figure 2 : Output Sustaining Voltage.

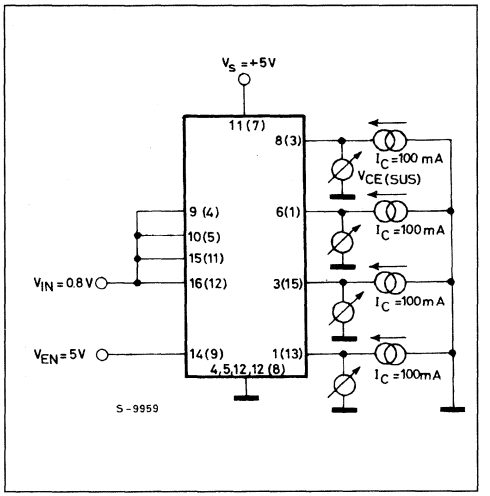


Figure 3 : Output Leakage Current.

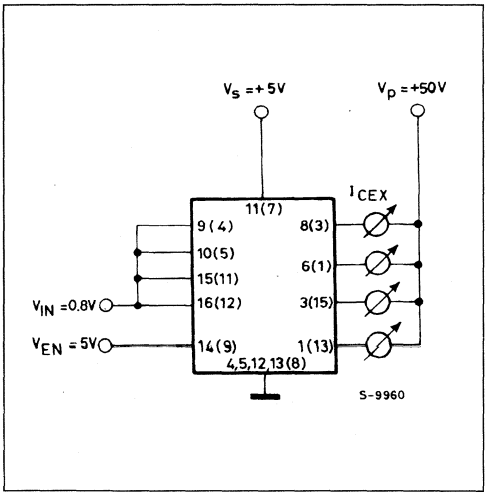


Figure 4 : Collector-emitter Saturation Voltage.

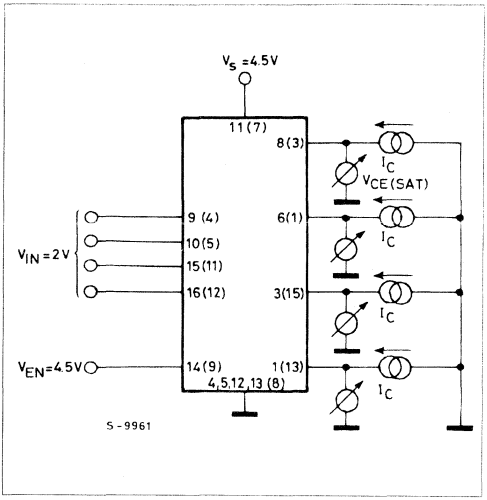
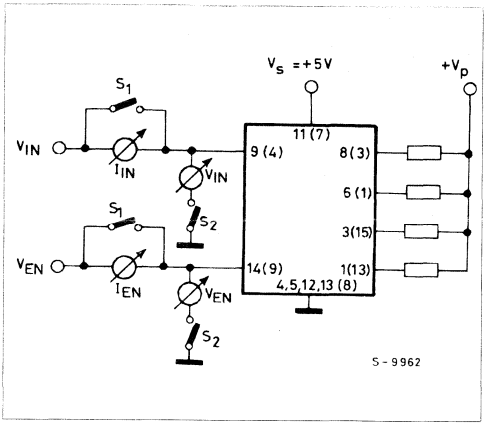


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{EN} = 0.8V for I_{IN} L, I_{EN} L
Set S_1, S_2 open, V_{IN}, V_{EN} = 2V for I_{IN} H, I_{EN} H
Set S_1, S_2 close, V_{IN}, V_{EN} = 0.8V for V_{IN} L, V_{EN} L
Set S_1, S_2 close, V_{IN}, V_{EN} = 2V for V_{IN} H, V_{EN} H

Figure 6 : Clamp Diode Leakage Current.

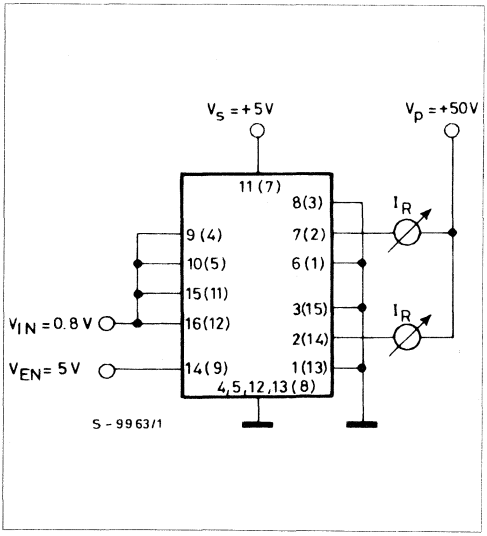


Figure 7 : Clamp Diode Forward Voltage.

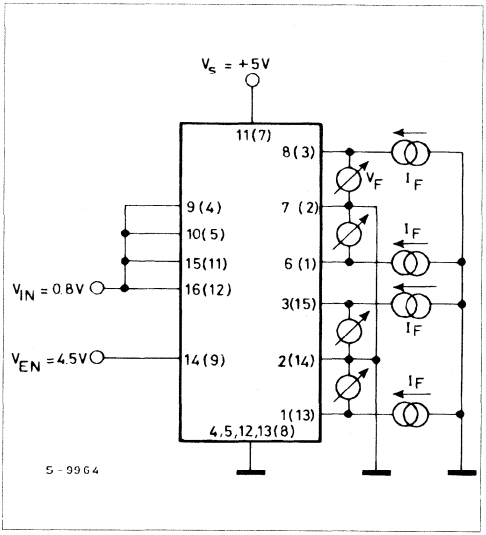


Figure 8 : Switching Times Test Circuit.

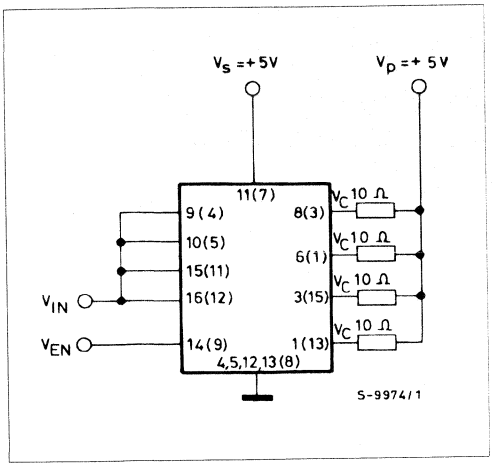


Figure 9 : Switching TImes Waveforms.

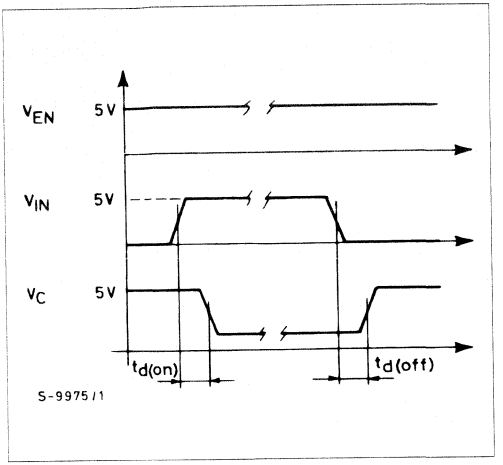


Figure 10 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221A).

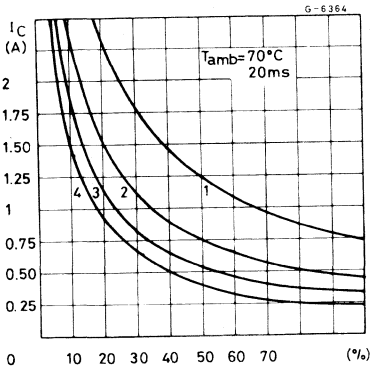


Figure 11 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221N).

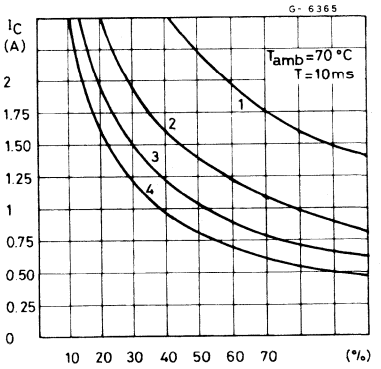


Figure 12 : Collector Saturation Voltage vs. Collector Current.

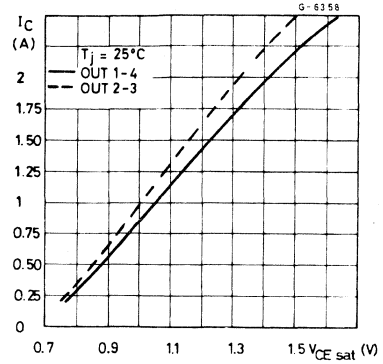


Figure 13 : Free-wheeling Diode Forward Voltage vs. Diode Current.

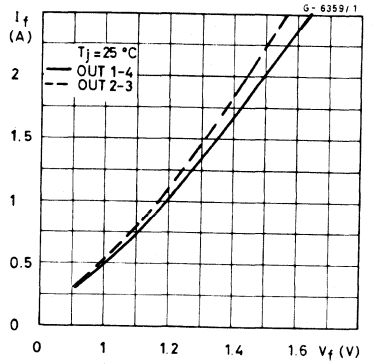


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1A.

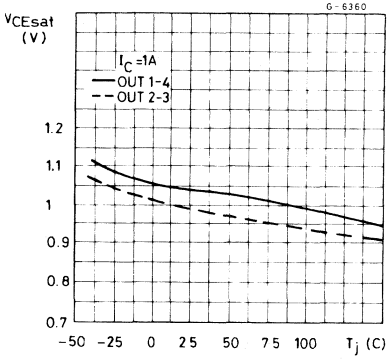


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1A.

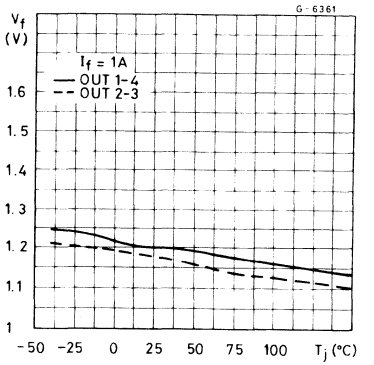


Figure 16 : Saturation Voltage vs. Junction Temperature at IC = 1.8A.

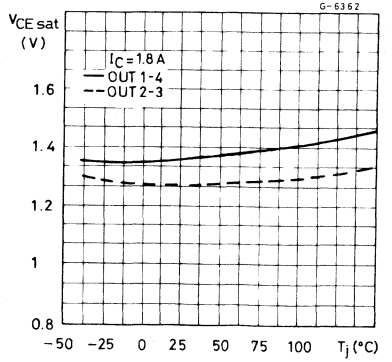


Figure 17 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at If = 1.8A.

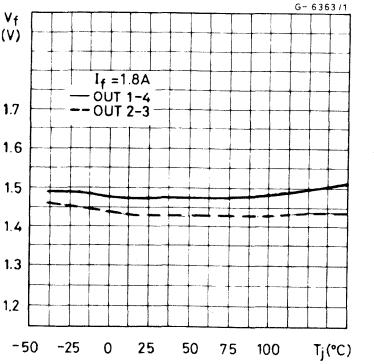
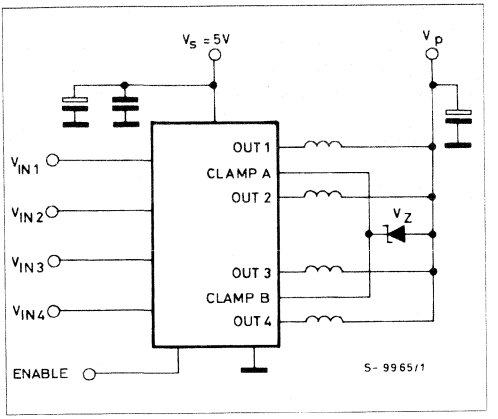


Figure 18.



APPLICATION INFORMATION

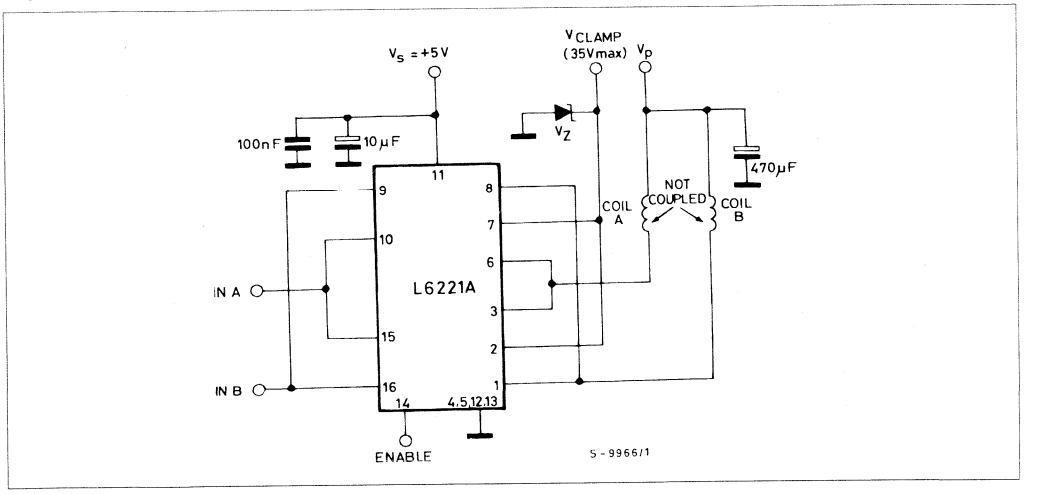
When inductive loads are driven by L6221A/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 18).

For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.
2) The instantaneous power must be limited to avoid the reverse second breakdown.

Figure 19 : Driver for Solenoids up to 3A.



Some care must be taken to ensure that the collectors are placed close together to avoid different current partitioning at turn-off.

We suggest to put in parallel channel 1 and 4 and channel 2 and 3 as shown in figure 19 for the similar electrical characteristics of the logic section (turn-on and turn-off delay time) and the power stages (collector saturation voltage, free-wheeling diode forward voltage).

Figure 20 : Saturation Voltage vs. Collector Current.

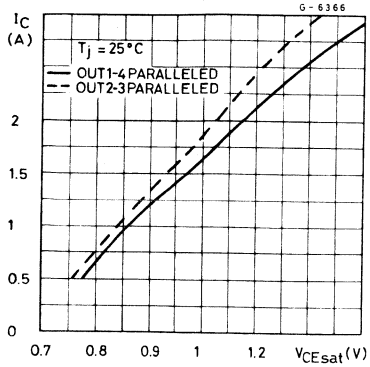


Figure 21 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221A).

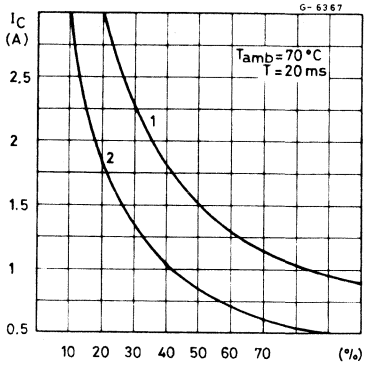
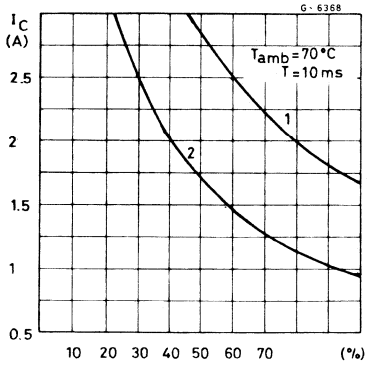


Figure 22 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6221A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 23) or to an external heatsink (Fig. 24).

The diagram of figure 25 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35µ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 23 : Example of P.C. Board Copper Area Which is Used as Heatsink.

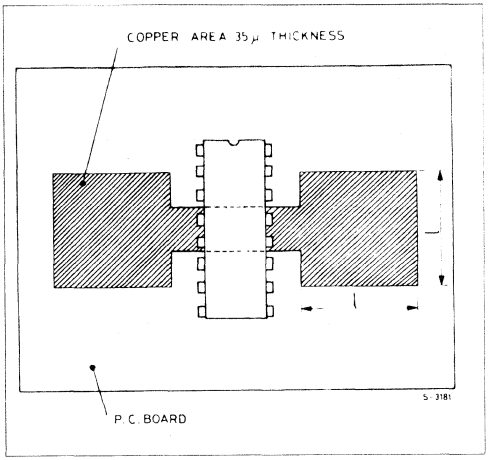


Figure 24 : External Heatsink Mounting Example.

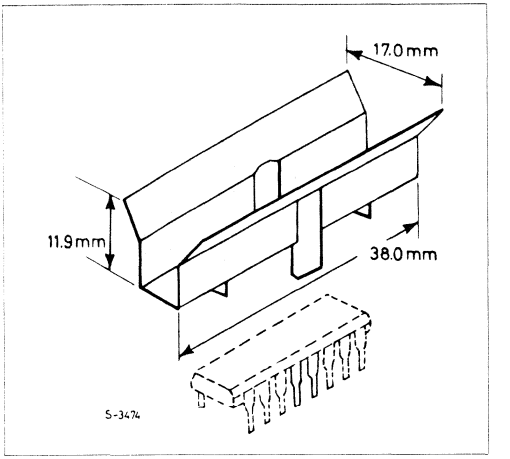


Figure 25 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side " α".

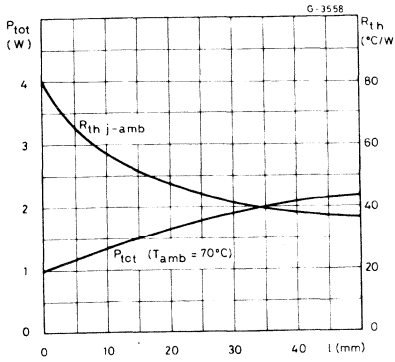
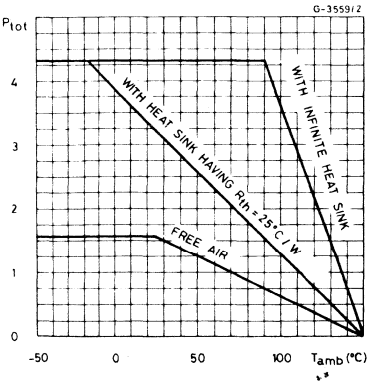


Figure 26 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



QUAD DARLINGTON SWITCH

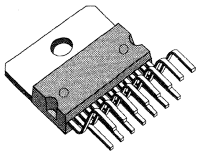
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 60 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

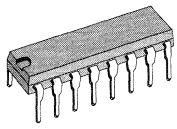
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6221C mounted in a Powerdip 12 + 2 + 2 package and the L6221CN mounted in a 15--lead Multiwatt package.



Multiwatt 15

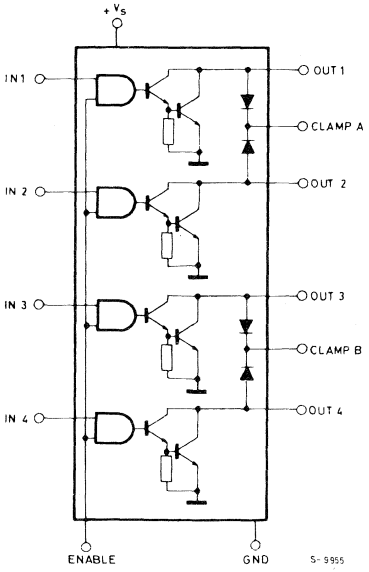


Powerdip 12 + 2 + 2

ORDERING NUMBERS :

L6221CN L6221C

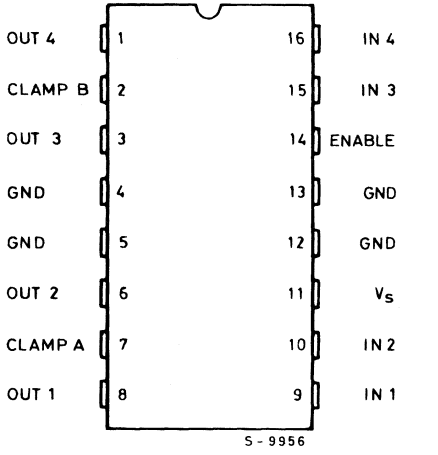
BLOCK DIAGRAM



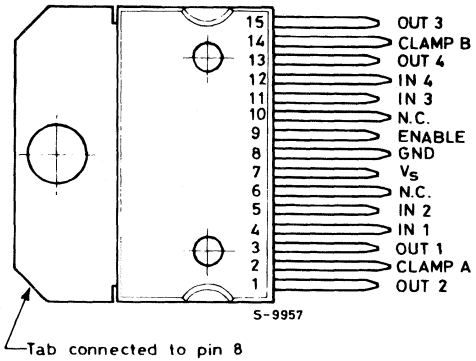
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_O	Output Voltage		60	V
V_S	Logic Supply Voltage		7	V
V_{IN} , V_{EN}	Input Voltage, Enable Voltage		V_S	
I_C	Continuous Colllector Current (for each channel)		1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10% ton = 5ms)		2.5	A
I_C	Collector Peak Current (non repetitive, t = 10µs)		3.2	A
T_{op}	Operating Temperature Range (junction)		-40 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
I_{sub}	Output Substrate Current		350	mA
P_{tot}	Total Power Dissipation	at T_{pins} = 90°C (powerdip)	4.3	W
		at T_{case} = 90°C (multiwatt)	20	W
		at T_{amb} = 70°C (powerdip)	1	W
		at T_{amb} = 70°C (multiwatt)	2.3	W

PIN CONNECTIONS (top views)



L6221C (Powerdip)



L6221CN (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt-15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERiSTICS Refer to The Test Circuit to Fig.1 to Fig.9 (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

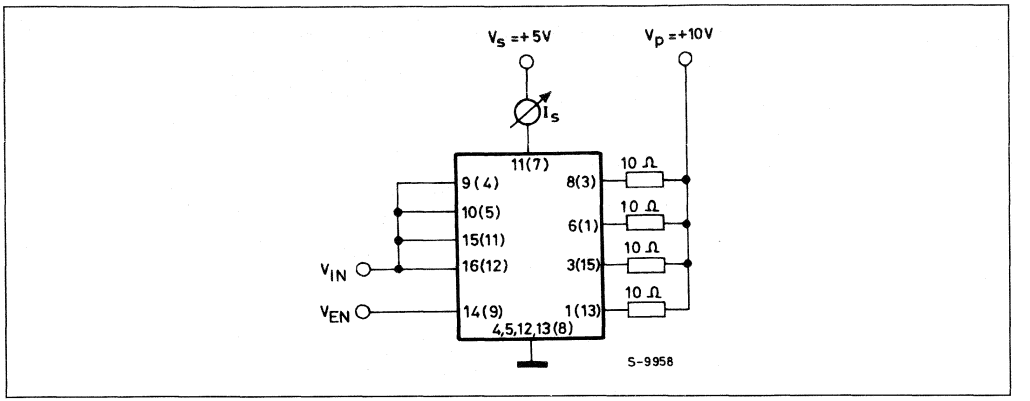
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage		4.5		5.5	V
I_S	Logic Supply Current	All outputs ON I_C = 0.7A All outputs OFF			20 20	mA mA
I_{CEX}	Output Leakage Current	V_{CE} = 60V V_{EN} = V_{ENH} V_{IN} = V_{INL}			1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on; all others inputs off).	V_S = 4.5V V_{IN} = V_{INH} V_{EN} = V_{ENH} I_C = 1A I_C = 2A			 1.4 1.85	 V V
V_{INL}, V_{ENL}	Input Low Voltage				0.8	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN} = V_{INL} V_{EN} = V_{ENL}			-100	µA
V_{INH}, V_{ENH}	Input High Voltage		2			V
I_{INH}, I_{ENH}	Input High Current	V_{IN} = V_{INH} V_{EN} = V_{ENH}			100	µA
I_R	Clamp Diode Leakage Current	V_R = 60V V_{EN} = V_{ENH} V_{IN} = V_{INL}			100	µA
V_F	Clamp Diode Forward Voltage	I_F = 1A I_F = 2A			1.8 2.2	V V
$t_{d(on)}$	Turn on Delay Time	V_P = 5V R_L = 10Ω			2	ms
$t_{d(off)}$	Turn off Delay Time	V_P = 5V R_L = 10Ω			5	µs
ΔI_S	Logic Supply Current Variation	V_{IN} = 5V V_{EN} = 5V I_{out} = -500mA for Each Channel			150	mA

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic supply current.



Set V_{IN} = 4.5V, V_{EN} = 0.8V, or V_{IN} = 0.8V, V_{EN} = 4.5V, for I_S (all outputs off)
Set V_{IN} = 2V, V_{EN} = 2V, for I_S (all outputs on)

Figure 2 : Output Sustaining Voltage.

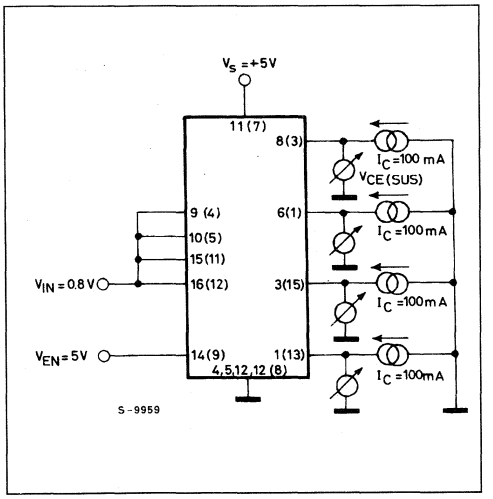
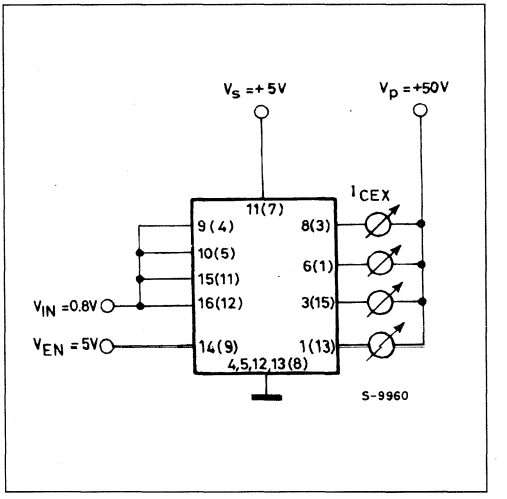


Figure 3 : Output Leakage Current.



V_P = +60V

Figure 4 : Collector-emitter Saturation Voltage.

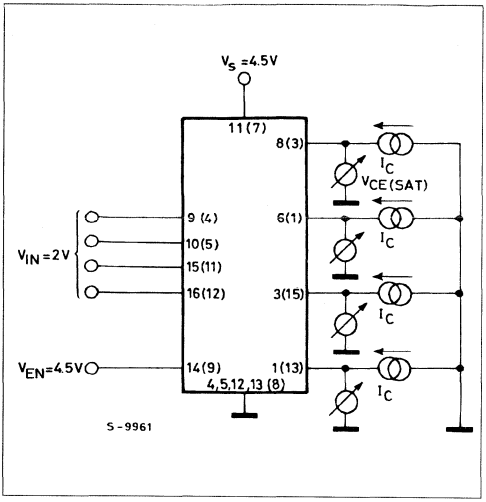
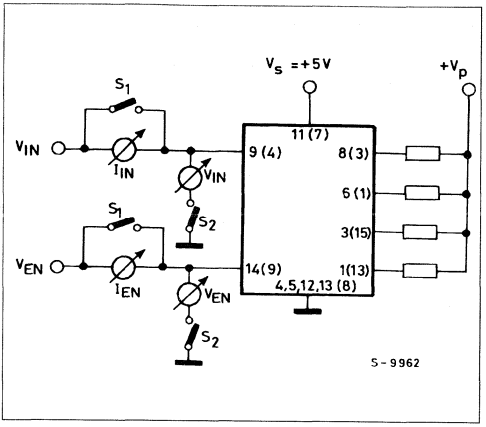


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{EN} = 0.8V for I_{IN} L, I_{EN} L
Set S_1, S_2 open, V_{IN}, V_{EN} = 2V for I_{IN} H, I_{EN} H
Set S_1, S_2 close, V_{IN}, V_{EN} = 0.8V for V_{IN} L, V_{EN} L
Set S_1, S_2 close, V_{IN}, V_{EN} = 2V for V_{IN} H, V_{EN} H

Figure 6 : Clamp Diode Leakage Current.

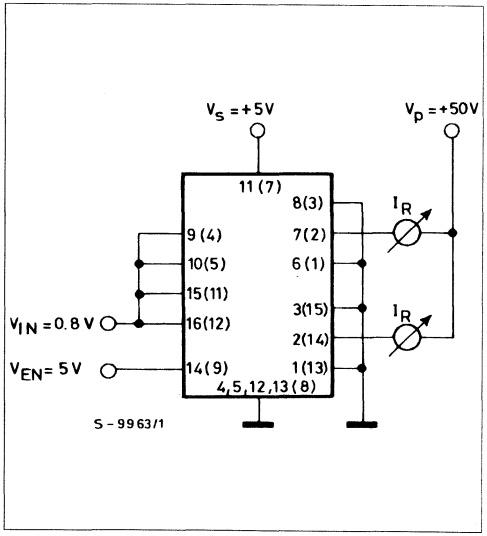
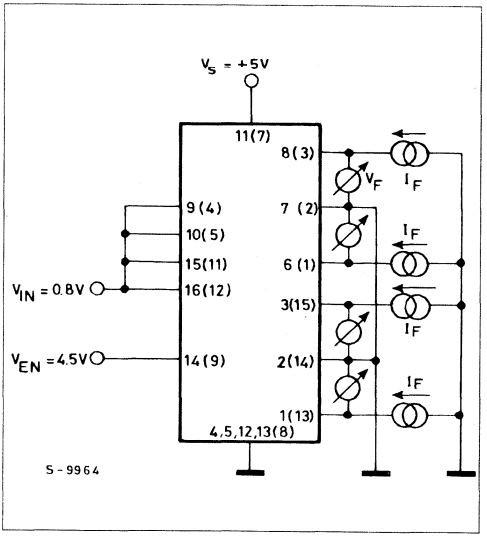


Figure 7 : Clamp Diode Forward Voltage.



V_P = +60V

Figure 8 : Switching Times Test Circuit.

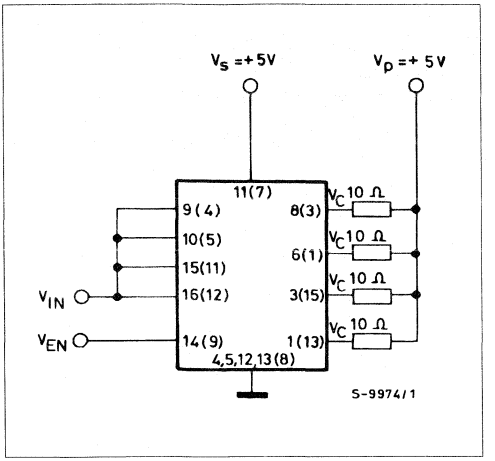


Figure 9 : Switching TImes Waveforms.

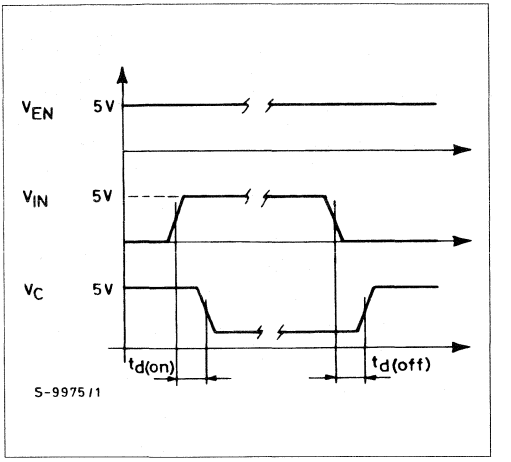


Figure 10 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221C).

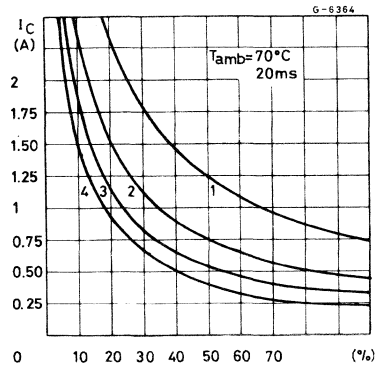


Figure 11 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221CN).

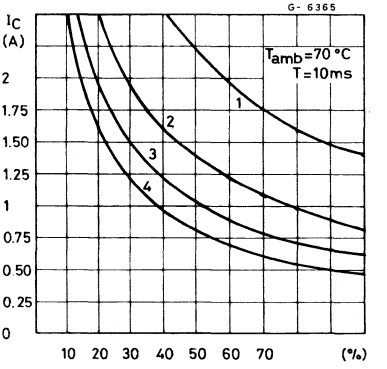


Figure 12 : Collector Saturation Voltage vs. Collector Current.

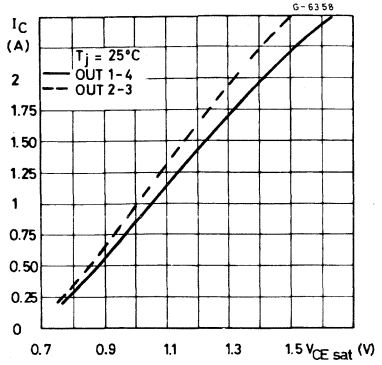


Figure 13 : Free-wheeling Diode Forward Voltage vs. Diode Current .

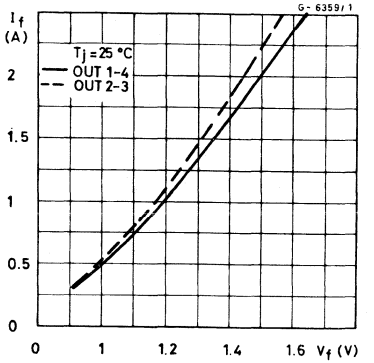


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1A.

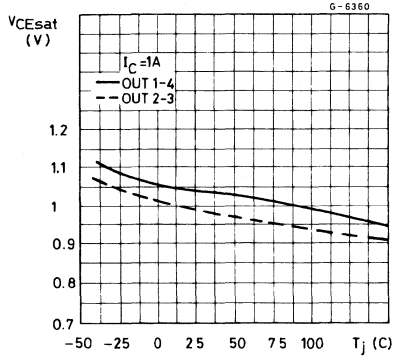


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1A.

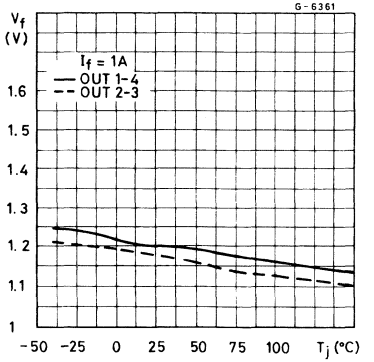


Figure 16 : Saturation Voltage vs. Junction Temperature at IC = 1.8A.

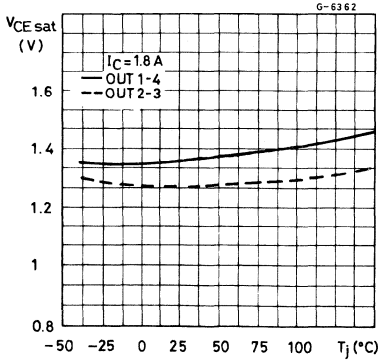


Figure 17 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at If = 1.8A.

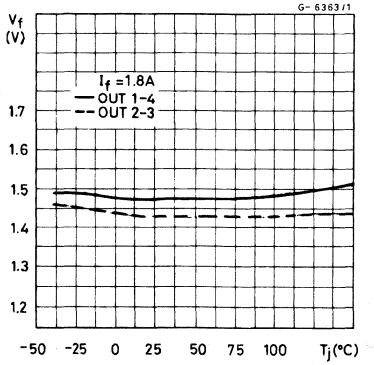
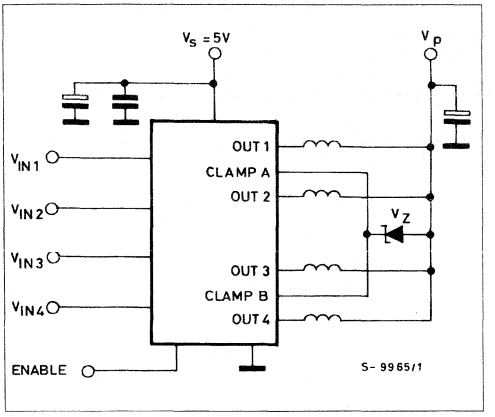


Figure 18.



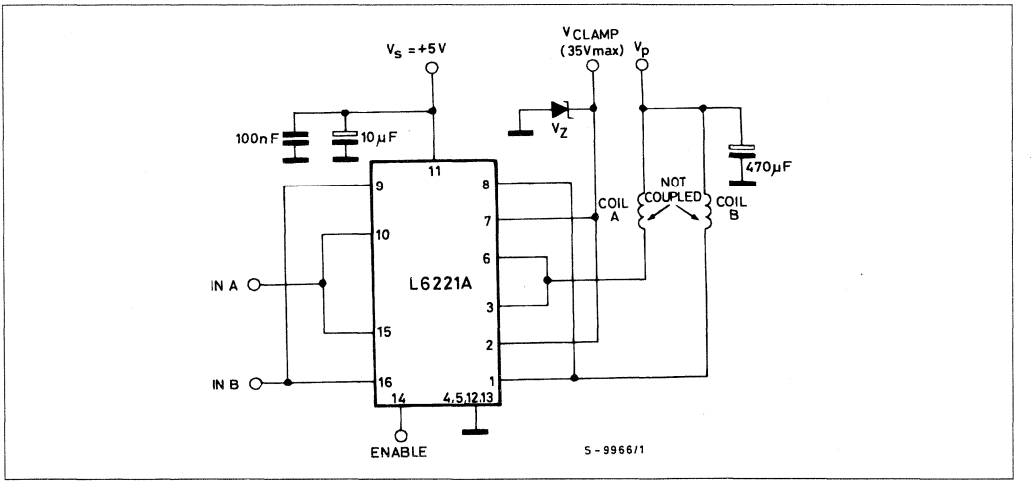
APPLICATION INFORMATION

When inductive loads are driven by L6221C/CN, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 18).

The zener has to be chosen in such a way that V_{CLAMP} is limited to 60V taking into account the zener's voltage changes due to: spread on V_Z, temperature changes, and the voltage drop due to ohmic resistance.

Moreover, the instantaneous power must be limited in order to avoid the reverse second breakdown.

Figure 19 : Driver for Solenoids up to 3A.



Some care must be taken to ensure that the collectors are placed close together to avoid different current partitioning at turn-off.

We suggest to put in parallel channel 1 and 4 and channel 2 and 3 as shown in figure 19 for the similar electrical characteristics of the logic section (turn-on and turn-off delay time) and the power stages (collector saturation voltage, free-wheeling diode forward voltage).

Figure 20 : Saturation Voltage vs. Collector Current.

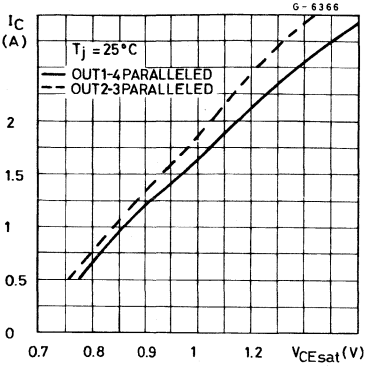


Figure 21 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221N).

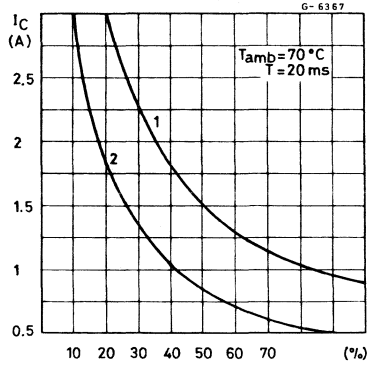
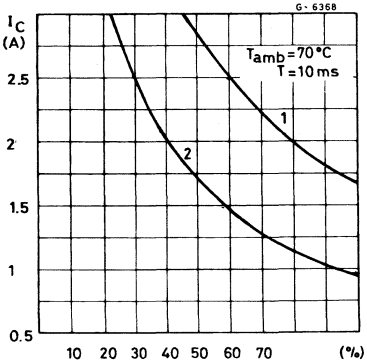


Figure 22 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221CN).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6221C can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 23) or to an external heatsink (Fig. 24).

The diagram of figure 25 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 23 : Example of P.C. Board Copper Area Which is Used as Heatsink.

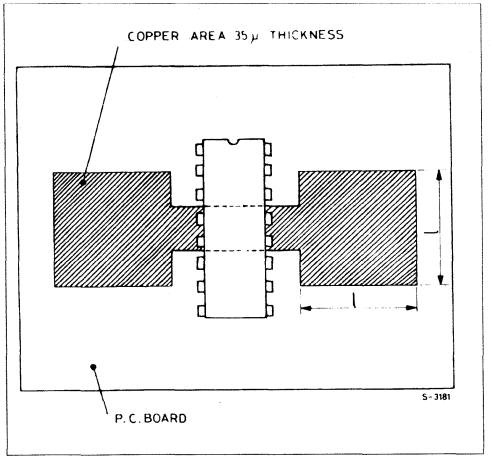


Figure 24 : External Heatsink Mounting Example.

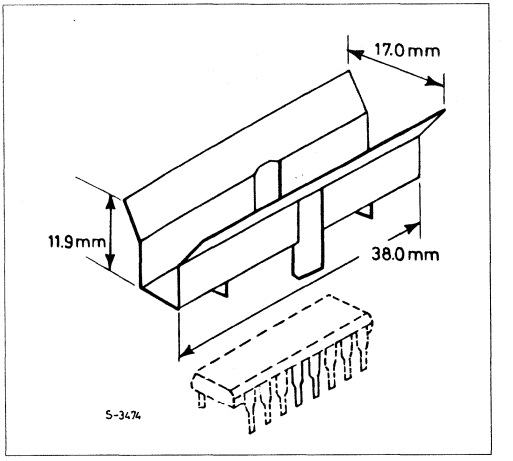


Figure 25 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side " α".

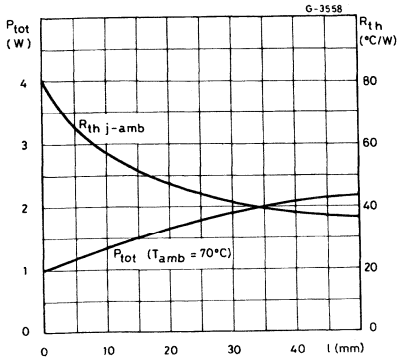
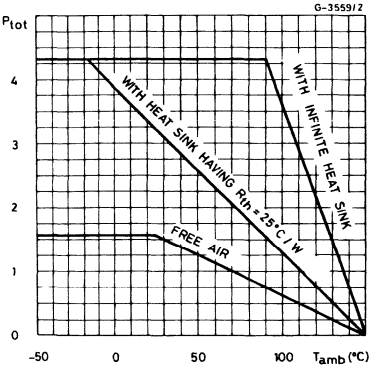


Figure 26 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



SGS-THOMSON MICROELECTRONICS

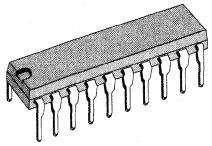
L6223A

DMOS PROGRAMMABLE HIGH SPEED UNIPOLAR STEPPER MOTOR DRIVER

ADVANCE DATA

- HIGH EFFICIENCY UNIPOLAR STEPPER MOTOR DRIVER
- HIGH SPEED UNIPOLAR STEPPER MOTOR DRIVER
- SUPPLY VOLTAGE UP TO 46V
- PHASE CURRENT UP TO 1A
- UP TO 2A/PHASE IN DUAL CONFIGURATION
- PARALLEL CMOS µP INTERFACE FOR FULL/HALF STEP MOTOR ROTATION
- SERIAL INTERFACE FOR 6 BIT PROGRAMMING
- CLOSE/OPEN LOOP, 8 PWM CURRENT LEVELS
- DUAL PWM FREQUENCY SELECTION
- INPUT BIDIRECTIONALLY PROTECTED
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



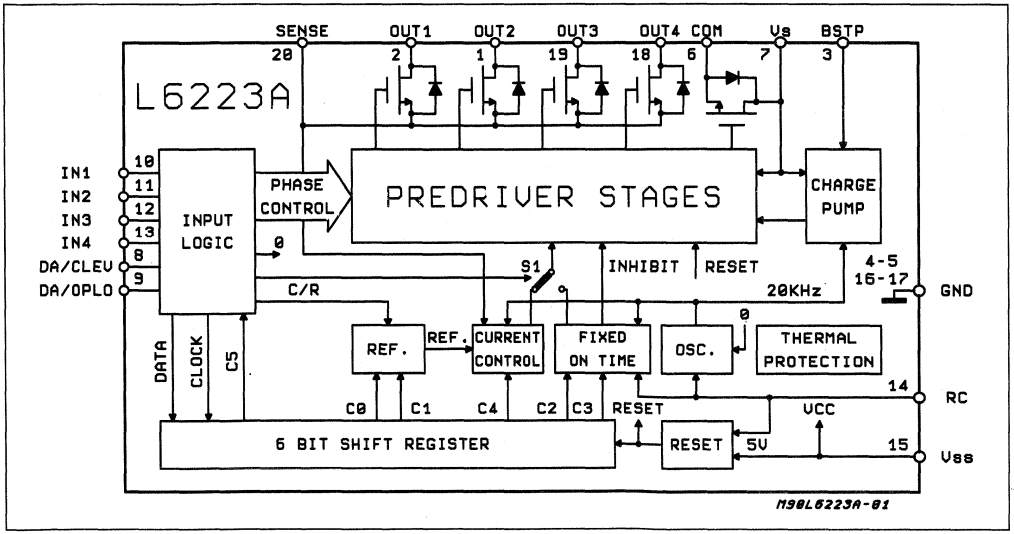
POWERDIP 16+2+2

ORDERING NUMBER : L6223A

DESCRIPTION

The L6223A is a programmable integrated system for driving a unipolar stepper motor. It is realized in Multipower BCD technology. The DMOS output stage, realized by a single upper DMOS switch and four lower DMOS, can deliver up to 1A/phase with motor supply voltages up to 46V. All inputs are CMOS and microprocessor compatible. An internal 6-bit shift register allows the device to be programmed to select different duty cycles in open loop mode and different chopping frequencies in closed loop mode. When the current control is in closed loop mode it is also possible to select a reduced current chopping level to optimize system efficiency. The L6223A is

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

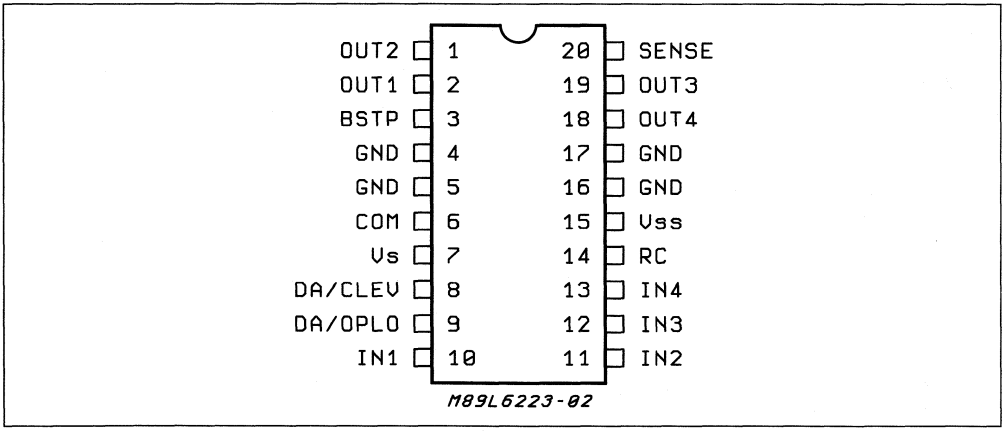
designed to work with a single sense resistor. During chopping t(OFF) time the current is reduced by half, improving efficiency. Higher current applications can be achieved by paralleling two L6223A. The L6223A is mounted in a 20-lead Powerdip package, (16+2+2). Four ground leads conduct heat to dedicated heatsink area on the PCB.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SS}	Logic supply	7	V
V_S	Supply voltage	50	V
V_I	Logic input voltage (*)	– 0.3V to V_{SS}	
V_O	Output voltage	100	V
V_{Opeak}	Output peak voltage (tpk = 5µs,10% d.c.)	125	V
I_{pl}	Output sink peak current d.c. 10% t(on) = 10µs	3	A
I_{ph}	Output source peak current d.c. 10%,t(on) = 10µs	6	A
P_{tot}	Total power dissipation: T_{pins} = 90°C	4.3	W
	T_{amb} = 70°C (**)	2	W
V_{sense}	Sensing voltage	– 1V to V_{SS}	
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

(*) Oscillator running
(**) 4 cm^2 copper area on PCB, see fig. 34

PIN CONNECTION (top wiew)



THERMAL DATA

$R_{thj\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

PIN DESCRIPTION

No.	Name	Function
1,2 18,19	OUT2,OUT1 OUT4,OUT3	Outputs for motor windings.
3	BSTP	A bootstrap capacitor connected between this pin and COM will generate the internal overvoltage required for driving the gate of the upper DMOS.
6	COM	Output for common wire of motor.
4,5 16,17	GND	Common ground. Also provides heatsinking to PCB.
7	V_S	Power supply
8	DA/CLEV	Digital input. 1) In PROGRAM MODE,operates in XOR with DA/OPLO to load data into 6-bit shift register. 2) In OPERATING MODE,works with the other digital inputs to reduce the current level (see Table 2 and Table 3).
9	DA/OPLO	Digital input. 1) In PROGRAM MODE, operates in XOR with DA/CLEV to load data into 6-bit shift register. 2) In OPERATING MODE,selects current control method: open loop (H) or closed loop (L).
10,11 12,13	IN1,IN2 IN3,IN4	Digital inputs. When all inputs are low level,the device is in PROGRAMMING MODE. In OPERATING MODE: 1) FULL MODE - IN1 to IN4 drive the motor phases. A previous programming is requested. 2) SIMPLIFIED MODE - IN1 and IN2 drive the phases,IN3 is ENABLE, IN4 works with DA/CLEV to enable the reduce current level. Previous programming not needed.
14	RC	Input for external RC network. Defines the higher of two possible chopping frequencies. If this pin is set to ground it will reset the IC.
15	V_{SS}	Logic supply.
20	SENSE	Output for sense resistor.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_S = 42V, V_{SS} = 5V, external RC network: R = 18kΩ, C = 3.3nF, unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_S	Power Supply		9	32	46	V
V_{SS}	Logic Supply		4.5	5	5.5	V
I_S	Power Supply Quiescent Current	IN1, IN2, IN3, IN4 = L RC = 0V DA/CLEV = L DA/OPLO = L		2	4	mA
I_{SS}	Logic Supply Quiescent Current	IN1, IN2, IN3, IN4 = L RC = 0V DA/CLEV = L DA/OPLO = L		14	20	mA
I_{OL}	Output Leakage Curr.	V_O = 100V (Fig. 1)			1	mA
V_{rs}	Reset Threshold Voltage (Pin 14)				0.9	V
T_{BOOT}	Bootstrap Refresh Pulse	C_{BOOT}= 10nF		3	5	µs
SINK MOS						
$R_{DS(ON)}$	ON Resistance	(Fig. 2a and Fig. 3)			1.2	Ω
SOURCE MOS						
$R_{DS(ON)}$	ON Resistance	(Fig. 2b and Fig. 3)			0.7	Ω
CURRENT CONTROL SECTION						
V_{ref}	Internal Reference Volt.	DA/CLEV = L; IN4 = H I_O = 100% nominal value	0.475	0.5	0.525	V
$f_{(OSC)}$	Oscillator Frequency	(Fig. 20)	18	20	22	KHz
$t_{(dis)}$	RC Network Discharge Time (t_{ON} min)	(Fig. 20)	2.3	3	4.3	µs
R_{int}	Internal Discharge Resistor (pin 14)			1.2		kΩ
T_W	Sense Filter Time Constant	(Fig. 4)	1	1.4	2.3	µs
LOGIC LEVELS						
$V_{(IN)L}$	Input Low Voltage		–0.3		0.8	V
$V_{(IN)H}$	Input High Voltage		2.4		V_{SS}	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SWITCHING TIMING						
t2, t4	Fall/Rise Time (IN1, 2, 3, 4)	$R_{(load)}$ = 39 Ω (Fig. 5) Pure Resistive Load to V_S			250	ns
t1, t3	Input-Output Delay (IN1, 2, 3, 4)	$R_{(load)}$ = 39 Ω (Fig. 5) Pure Resistive Load to V_S			700	ns
t_{dPWM}	Close Loop PWM Control Delay	(Fig. 4) Note 1			1	µs
PROGRAMMING TIMING						
t1	Loading Time	(Fig. 6)	1.7			µs
t2	Protection Time	(Fig. 6) Note 2	0.2			µs
t3	Data Set-up	(Fig. 6)	0			ns
t4	Data Hold	(Fig. 6)	1.6			µs
t5	Setting Time	(Fig. 6)	200			ns

Note 1) Upper DMOS turn ON delay when the signal is applied at the input comparator (point A in Fig. 4).
Note 2) Internal clock pulse is generated only if IN1...IN4 stay Low for almost 0.2 µs. This delay avoids undesirable programmings.

Figure 1: Output leakage I_{OL} Test Circuit

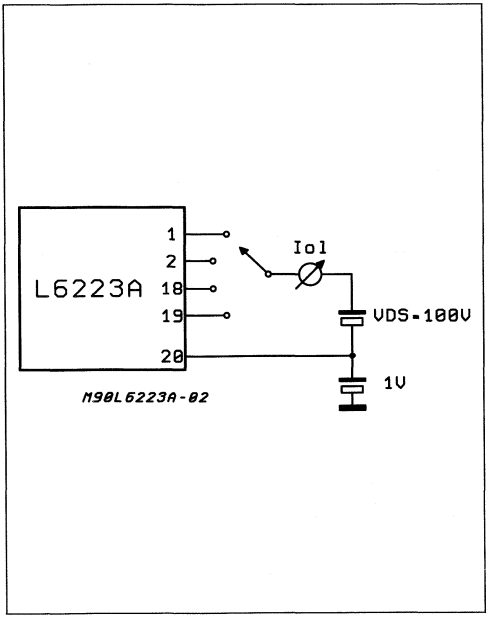


Figure 2a: Source Output DMOS $R_{DS(ON)}$ Test Circuit

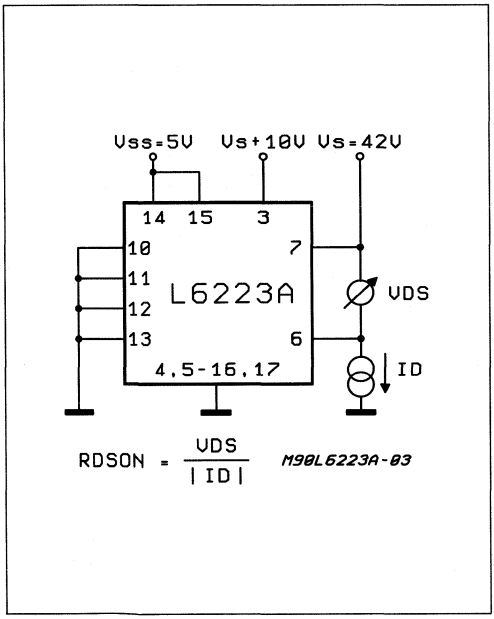


Figure 2b: Sink Output DMOS $R_{DS(ON)}$Test Circuit

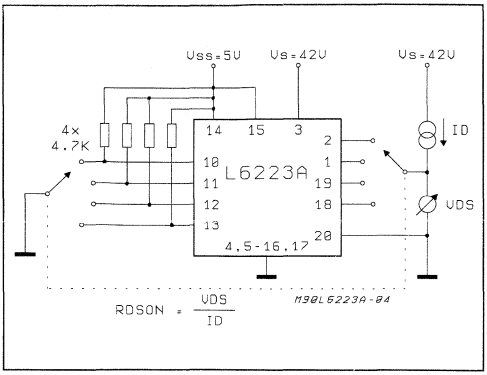


Figure 3: Typical normalized $R_{DS(ON)}$ vs. Junction temperature

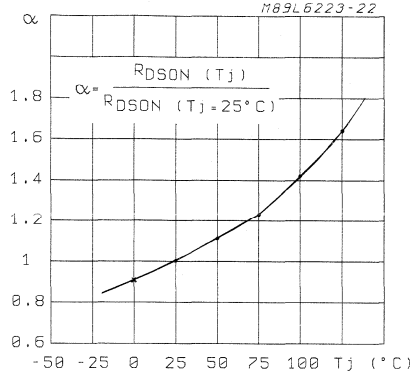


Figure 4: Sense Filter RC Time Constant and PWM Closed Loop control Circuit

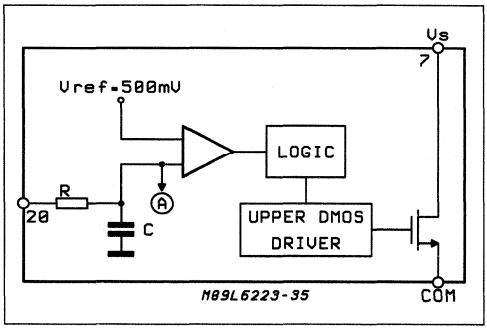


Figure 5: Output Sink Current Delay vs Input Control

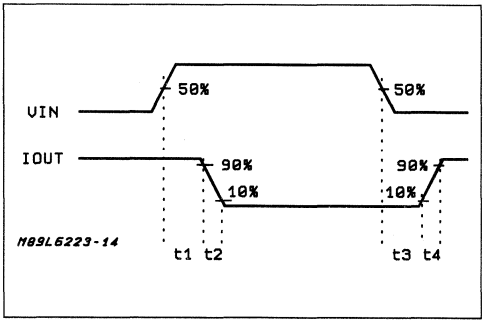
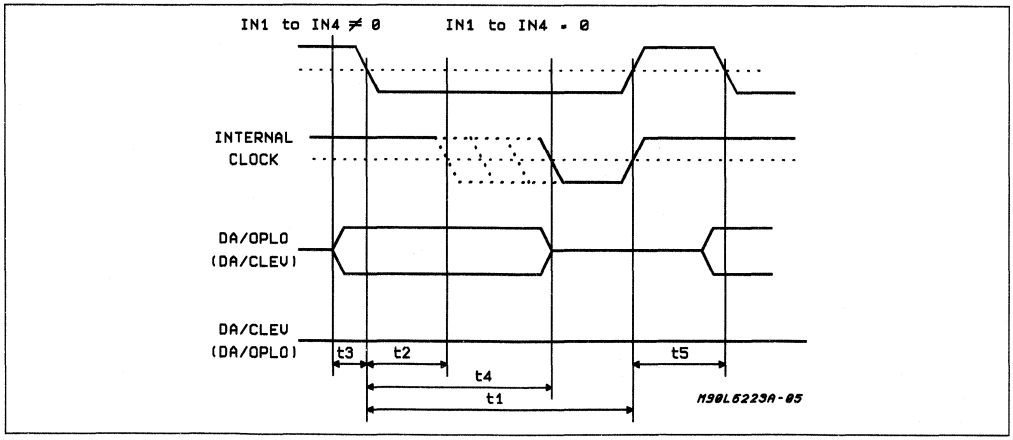


Figure 6: Programming Timing Diagram (see Block Diagram)



BLOCK DIAGRAM DESCRIPTION

Input Logic
Decodes the input signals IN1, IN2, IN3, IN4, DA/OPLO, and DA/CLEV for programming the device and driving the motor. The six inputs are CMOS compatible and can interface directly with a microprocessor.

Predriver Stages
Drive the gates of the five DMOS. They interface the power section with the logic section. The internal inhibit, when activated, disables the power section. The reset initializes the shift register and disables the power section.

6 bit Shift Register
Internal memory which defines the working configuration of the device along with the input signals.

Current Control
When selected with the input DA/OPLO = L (Closed Loop), it will maintain a constant output current level by chopping. The value of the reference voltage, which is compared to the sense voltage, is given by the Ref Block. The chopping frequency depends on bit C4.

Ref Block
Defines the current chopping level according to bits C0 and C1 and the input signals.

Fixed on Time
When selected with DA/OPLO = H, it will define according to bits C2 and C3 the chopping duty cycle for the Open Loop mode. The chopping frequency is fixed.

Oscillator
Provides the clock setting the S/R FLIP-FLOP that turn ON/OFF the upper DMOS (Fig. 22). The higher operative chopping frequency is defined by the external RC network (typically 20KHz). At the phase change a syncronous clock pulse is generated

Reset Logic Block
Generates the reset signal for the logic at power on and disables the outputs. The reset can also be generated externally by setting the RC pin to less that 0.9V.

Thermal Protection
Disables the power section in case of over temperature condition.

Charge Pump
Along with an external bootstrap capacitor connected between the BSTP and COM pins, this block generates the internal over voltage required to drive the upper DMOS on.

Power Output
Driven by the Predriver Stages, it supplies the power for the motor windings.

CIRCUIT OPERATION

The five N DMOS transistors of the output stage drive the unipolar motor windings, controlling the current by chopping. In particular, the four Low side (OUT1, OUT2, OUT3, OUT4) switch the phase configurations, and the High side DMOS (COM) is for chopping control.
For this transistor a charge pump circuit provides its necessary gate drive over voltage.
The microprocessor outputs are interfaced with the L6223A output stages through the input logic block. This block also protects the device from microprocessor output errors and failures from the power section back to the microprocessor outputs. The six digital inputs IN1, IN2, IN3, IN4, DA/CLEV, DA/OPLO, are decoded for motor control and rotation when in "Operating mode" and used for the internal six Bit memory programming when in "Programming Mode".
Table 1 shows the condition that selects these device status. The programming of the internal six bit memory sets operative conditions such as:

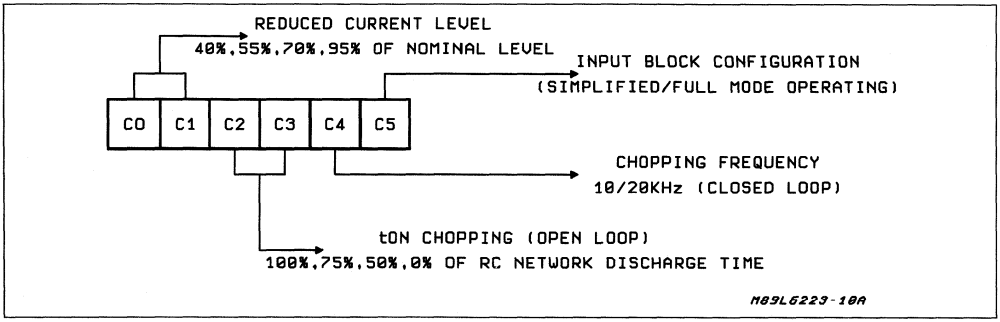
- PWM CURRENT LEVELS
- CHOPPING FREQUENCY
- LOGIC IN/OUT DECONDING

This memory works like a shift register. Each bit is introduced serially by decoding the IN1, IN2, IN3, IN4 low status for the internal clock pulse generation and by the DA/CLEV DA/OPLO, inputs in exor, as data in.
Figure 7 shows the six bit meaning.
In the operating mode two different input drive are possible. In SIMPLIFIED OPERATING MODE the IC needs few logic wire for the motor rotation, but only the full step driving sequence can be performed.

Table 1

Device status	Bit C5	IN1	IN2	IN3	IN4	DA/CLEV	DA/OPLO
Simplified mode operating	L	Phase A Driver	Phase B Driver	Enable	Alternative Current Reduction "LOW"	Current Reductio Active "HIGH"	Open/Closed Loop current control
Full mode operating	H	Phase A	Phase $\bar{A}$ driver	Phase B driver	Phase B driver		
Programming mode	X	L	L	L	L	serial data in	serial data in

Figure 7: Internal Six-Bit Shift Register Bit Functions



CIRCUIT OPERATION (continued)

The FULL OPERATING MODE permits all the driving possibilities. The 4 low side DMOS transistors are drived directly by the 4 inputs IN1, IN2, IN3, IN4 which define directly the phases configuration. The chopping of the motor current can be in open loop or in close loop. When in open loop (fixed on-time block) the DA/OPLO pin is High and the motor current is not controlled but it mostly depends from the bits C2 nd C3. When in close loop the DA/OPLO is Low and the output current is controlled at a constant value defined by the internal reference and by the sensing resistor value. The internal reference depends by the programming bits C0, C1, and by the input configurations. During the power on sequence the reset circuitry prevents current spikes disabling the outputs and by resetting the memory.

Power Section

The basic concept for the current control is explained by examining the winding pair phase A (MA) in Figure 24. With Q5 = ON, Q2 = OFF the current rises until $R_S I_P$ equals the comparator threshold value. The comparator output resets the F/F and Q5 switches off. In this condition the current decay path begins as shown in Figure 25. The current value becomes $I_P/2$, according to the double number of turns interested. In order to reduce the dissipation, Q2 is also driven on. Q5 remains off (PWM off time) up to a new clock pulse sets again the F/F. The winding current behaviour is shown in Figure 26.

Since during PWM off time the current value is half that of the on time and since in a typical application Toff >>Ton, the device dissipation is further reduced.

The five DMOS transistors are connected to the "predriver stages" block, that drives the DMOS gates, and interfaces them to the internal input logic. The "charge pump" provides correct voltage for Q5 UPPER DMOS gate drive by using the external bootstrap capacitor.

Programming Mode

The Programming Mode is defined by the inputs IN1=IN2=IN3=IN4=Low. When in PROGRAMMING MODE the outputs are disabled. The waveform shown in Fig. 8 represents one pos-

sible timing diagram for programming. When the inputs IN1...IN4 are together Low a clock pulse is generated internally which clocks a data bit into the shift register. If the time interval during which all four inputs are Low is less than 0.2µs, no clocks pulse in generated thus preventing undesirable programming. To generate another clock pulse at least one of the four inputs must first go High and then Low again. The first bit is loaded into C0 and after 6 clock pulse it will be in the C5 posistion. Two programming technique are suggested. The first (Fig. 8) uses IN4 in such a way that the power section is disabled the total programming time (the carriage of the 6 programming bits). Fig. 9 shows another technique: the motor driving signals at the inputs IN1...IN4 are interrupted switching IN1...IN4 Low to carry a single bit. This permits the motor to be enabled for the 50% of total programming time. During the motor rotation it's suggested to program the device immediately after the motor phase change: this make neglectable the motor driving discontinuity due to the device programming.

Figure 8: Waveform for programming: the output is disabled during all the programming duration (see Table 4).

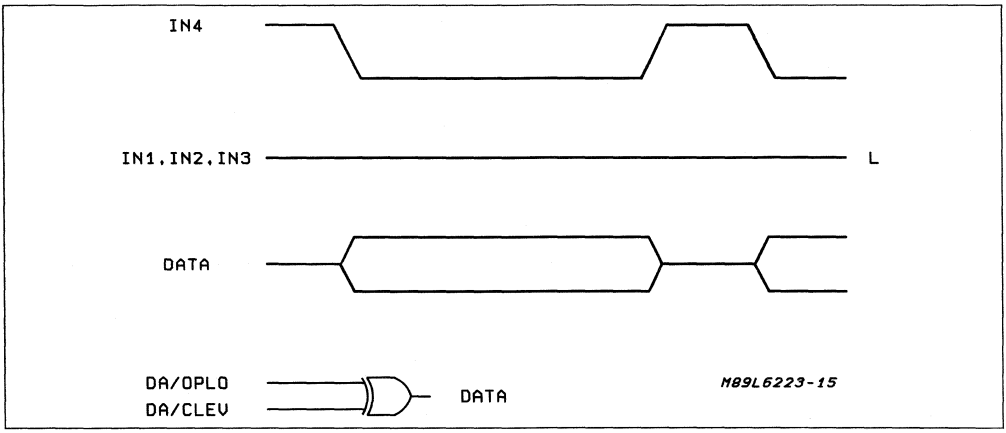
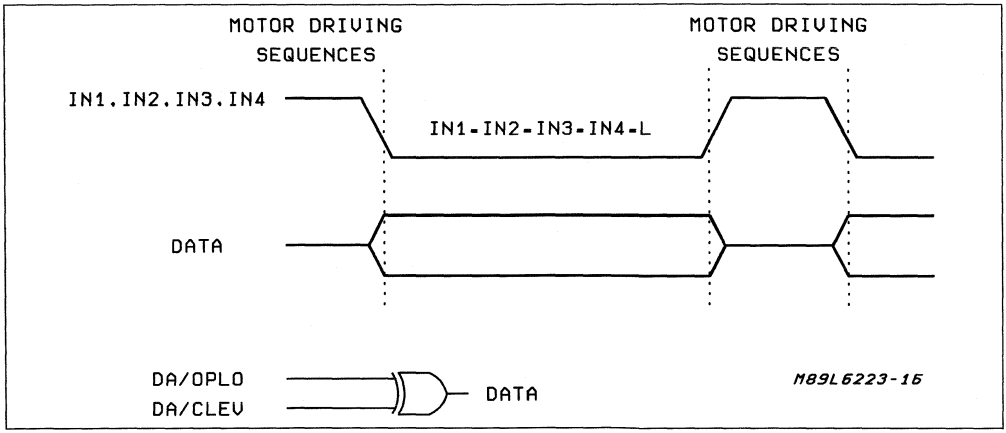


Figure 9: Waveform for programming: the output is disabled only when all four inputs are at the low level.



Operating Mode

The bit C5 defines the two available input configurations.
C5 = H: FULL MODE OPERATING
The digital inputs have the following functions:

- IN1 drives OUT1
- IN2 drives OUT2
- IN3 drives OUT3
- IN4 drives OUT4

The output DMOS is ON when the corrisponding input is low

- DA/CLEV enables the current reduction (see Tab 2)
- DA/OPLO selects the motor current control mode (open or close loop).

Since each input drives one phase of the motor it is possible to work either in Half Step or in Full Step mode. DA/OPLO defines the current control mode as follow:

– DA/OPLO = H open loop
– DA/OPLO = L closed loop

The reduced current level is enabled by the inputs IN1, IN2, IN3, IN4 or by DA/CLEV (Tab. 2). The reduced current value depends from the bits C0, C1 (TAB. 5). The outputs are disabled when the inputs are in a prohibited state (Tab. 4).

C5 = L, SIMPLIFIED MODE OPERATING

When in SIMPLIFIED MODE OPERATING the inputs assume the following functions:

- IN1 drives Phase A
- IN2 drives Phase B
- IN3 ENABLE input (active High)
- IN4 enables the reduced current (Tab. 3)
- DA/CLEV enables the reduced current (Tab. 3)
- DA/OPLO selects the motor current control mode

The SIMPLIFIED MODE OPERATING configuration does not allow the drive of a unipolar motor in Half step.
The signal DA/OPLO functions as in FULL Mode Operation. When the current control is implemented in closed loop, the reduced current level is enabled by the inputs IN4, DA/CLEV (Tab. 3). The current reduction depends from the bits C0, C1 (Tab. 5).

Open/Closed Loop Motor Current Control

The logic input DA/OPLO selects the current control mode as previously seen. When in open loop, the chopping frequency is that one as defined by the external RC network. In open loop are available three different t(ON), depending from the bits C2, C3 (Tab. 6), as a percentage of the RC discharge time $t_{(dis)}$.

When in closed loop two different chopping frequencies are selectable by means of the bit C4 (Tab. 7). The higher is defined by the external RC network. The other one is exactely the half. In closed loop 5 different current levels are available: the nominal current level and four reduced current levels (Tab. 5). The nominal current level is set by an internal reference voltage of 0.5V. The configuration of bits C0, C1 sets the reference voltage to a pecentage of the nominal value.

TRUTH TABLES (L = Low; H = High; X = don't care)

Table 2

IN1	IN2	IN3	IN4	DA/CLEV	C/R*
H	H	X	X	X	H
X	X	H	H	X	H
H	H	H	H	X	H
X	X	X	X	H	H

*) C/R = H, reduced current

Table 3

IN4	DA/CLEV	C/R
L	X	H*
X	H	H*
H	L	L**

*) Reduced current **) Nominal current

Table 4

IN1	IN2	IN3	IN4	Output Stage
L	L	X	X	DISABLED
X	X	L	L	DISABLED

Table 5

C0	C1	Reduced Current Level (*)
L	L	40%
L	H	50%
H	L	70%
H	H	85%

*) Nominal level percentage

Table 6

C2	C3	$t_{(ON)}/t_{(OSC)}$*
L	L	75
L	H	50
H	L	100
H	H	Output Disabled

*) RC discharge time percentage

Table 7

C4	Chopping Frequency
L	20kHz
H	10kHz

L6223A Operating Configuration vs. 6bits Shift Register Programming (External RC network: R = 18kΩ C = 3,3nF)

Nr	SHIFT REGISTER bITS C5	C4	C3	C2	C1	C0	Full/Simpl. Operation Mode	Close Loop Frequency (kHz)	Open Loop $t_{(ON)}$ [%]	Close Loop Current Level [%]
0	0	0	0	0	0	0	S	20	75	40%
1	0	0	0	0	0	1	S	20	75	70%
2	0	0	0	0	1	0	S	20	75	55%
3	0	0	0	0	1	1	S	20	75	85%
4	0	0	0	1	0	0	S	20	100	40%
5	0	0	0	1	0	1	S	20	100	70%
6	0	0	0	1	1	0	S	20	100	55%
7	0	0	0	1	1	1	S	20	100	85%
8	0	0	1	0	0	0	S	20	50	40%
9	0	0	1	0	0	1	S	20	50	70%
10	0	0	1	0	1	0	S	20	50	55%
11	0	0	1	0	1	1	S	20	50	85%
12	0	0	1	1	0	0	S	20	DISABLED	40%
13	0	0	1	1	0	1	S	20	DISABLED	70%
14	0	0	1	1	1	0	S	20	DISABLED	55%
15	0	0	1	1	1	1	S	20	DISABLED	85%
16	0	1	0	0	0	0	S	10	75	40%
17	0	1	0	0	0	1	S	10	75	70%
18	0	1	0	0	1	0	S	10	75	55%
19	0	1	0	0	1	1	S	10	75	85%
20	0	1	0	1	0	0	S	10	100	40%
21	0	1	0	1	0	1	S	10	100	70%
22	0	1	0	1	1	0	S	10	100	55%
23	0	1	0	1	1	1	S	10	100	85%
24	0	1	1	0	0	0	S	10	50	40%
25	0	1	1	0	0	1	S	10	50	70%
26	0	1	1	0	1	0	S	10	50	55%
27	0	1	1	0	1	1	S	10	50	85%
28	0	1	1	1	0	0	S	10	DISABLED	40%
29	0	1	1	1	0	1	S	10	DISABLED	70%
30	0	1	1	1	1	0	S	10	DISABLED	55%
31	0	1	1	1	1	1	S	10	DISABLED	85%
32	1	0	0	0	0	0	F	20	75	40%
33	1	0	0	0	0	1	F	20	75	70%
34	1	0	0	0	1	0	F	20	75	55%
35	1	0	0	0	1	1	F	20	75	85%
36	1	0	0	1	0	0	F	20	100	40%
37	1	0	0	1	0	1	F	20	100	70%
38	1	0	0	1	1	0	F	20	100	55%

L6223A Operating Configuration vs. 6bits Shift Register Programming (Continued)

Nr	SHIFT REGISTER bITS C5	C4	C3	C2	C1	C0	Full/Simpl. Operation Mode	Close Loop Frequency (kHz)	Open Loop $t_{(ON)}$ [%]	Close Loop Current Level [%]
39	1	0	0	1	1	1	F	20	100	85%
40	1	0	1	0	0	0	F	20	50	40%
41	1	0	1	0	0	1	F	20	50	70%
42	1	0	1	0	1	0	F	20	50	55%
43	1	0	1	0	1	1	F	20	50	85%
44	1	0	1	1	0	0	F	20	DISABLED	40%
45	1	0	1	1	0	1	F	20	DISABLED	70%
46	1	0	1	1	1	0	F	20	DISABLED	55%
47	1	0	1	1	1	1	F	20	DISABLED	85%
48	1	1	0	0	0	0	F	10	75	40%
49	1	1	0	0	0	1	F	10	75	70%
50	1	1	0	0	1	0	F	10	75	55%
51	1	1	0	0	1	1	F	10	75	85%
52	1	1	0	1	0	0	F	10	100	40%
53	1	1	0	1	0	1	F	10	100	70%
54	1	1	0	1	1	0	F	10	100	55%
55	1	1	0	1	1	1	F	10	100	85%
56	1	1	1	0	0	0	F	10	50	40%
57	1	1	1	0	0	1	F	10	50	70%
58	1	1	1	0	1	0	F	10	50	55%
59	1	1	1	0	1	1	F	10	50	85%
60	1	1	1	1	0	0	F	10	DISABLED	40%
61	1	1	1	1	0	1	F	10	DISABLED	70%
62	1	1	1	1	1	0	F	10	DISABLED	55%
63	1	1	1	1	1	1	F	10	DISABLED	85%

APPLICATION INFORMATION

Single Device Application

Figure 10 shows a typical Single Device Application. With the shown external RC network, the higher chopping frequency is 20 kHz.

In the figure 11, 12 and 13 are shown the waveforms required to drive the motor in Half/Full Step in FULL MODE OPERATING (FMO) and SIMPLIFIED MODE OPERATING (SMO). The sense resistor defines the total motor current. This means that when two phases are ON, the sense current is two times the phase current. In this case the sense resistor value is $R_S = (V_{ref}/2I_P)$, where V_{ref} is the reference voltage and I_P the phase current. We have supposed that the phase current is of the same intensity in the two phases. When only one phase in ON, the current flowing in the sensing resistor is the phase current: this occurs in half step driving mode. The Figures 14 and 15 show the envelope of the sensing voltage in full and half step respectively. When current imbalance is not considered, this envelope represents the current level $2I_P$ controlled by the chopping when L6223A is working at 100% of current; in full step this level is constant while in half step two different levels are present (Figure 15). Actually, in full step two phases are always ON, and the chopping current level can be changed only by the controller. In half step when two phases are ON and L6223A is working at nominal current level ($2I_P$), but when only one phase is ON, L6223A selects automatically the reduced current. This level depends upon the programming bits. In Figure 15 the higher level represents the chopping at nominal value (two phases ON), the lower level the chopping at the reduced current (one phase ON). The negative peak shown in the figures represents the fast current recirculation at the phase change.

Fig. 15 shows also what happens when the reduced current level selected is at 70% of the nominal value. The motor torque is proportional to the vectorial sum of the phase currents: it can be seen that the unipolar stepper motor control actuated by L6223A in half step is at constant torque but not at constat current.

Figure 10: Typical Application Circuit using a single device: the max peak current capability is of 1A/phase (R_S = 0.25Ω)

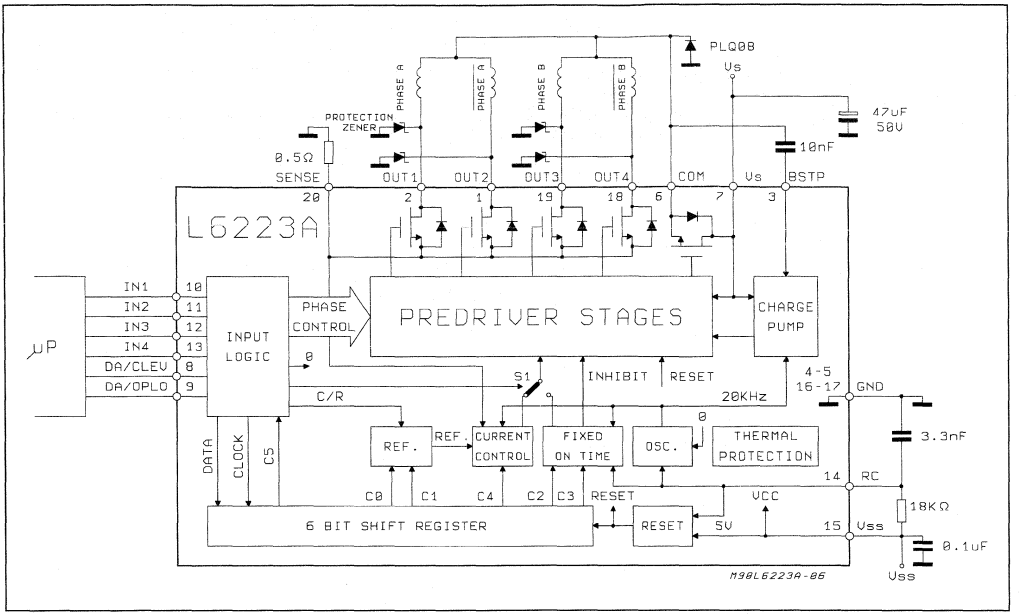


Figure 11: Inputs for Half Step drive, single device FMO.

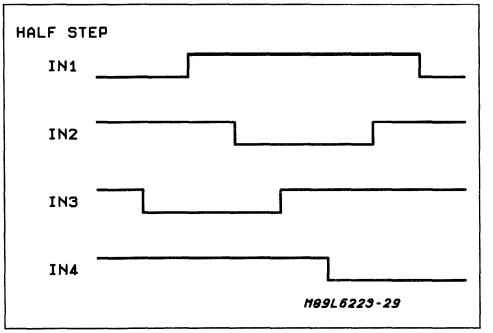


Figure 12: Inputs for Full Step drive, single device FMO.

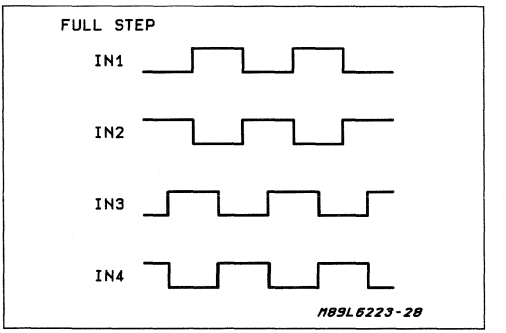


Figure 13: Inputs for Full Step drive single device SMO.

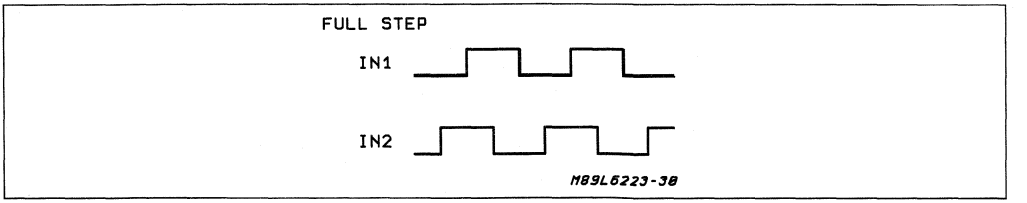


Figure 14: Peak current $2I_p$ crossing the sense resistor R_S in Full step drive. The phase sequence CCW is: AB →BA̅ →A̅B̅ → B̅A (4 Full Steps, 2 phase ON)

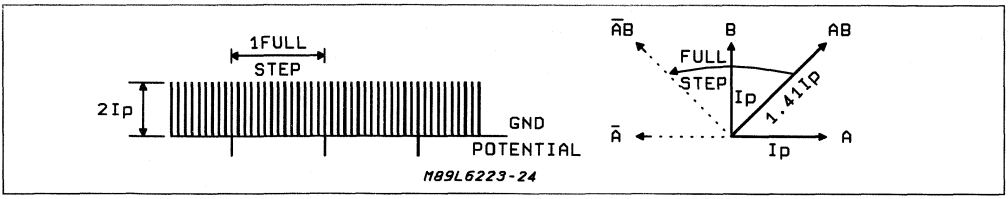


Figure 15: Peak current ($2I_p$/2 phase ON) and reduced peak current ($1.4I_p$/1 phase ON) crossing the sense resistor R_S in Half step drive. The phase sequence is: A →AB → B → BA → A̅ →A̅B̅ →B̅ → B̅A (8 Half Steps, 1 phase ON and 2 phases ON alternatively)

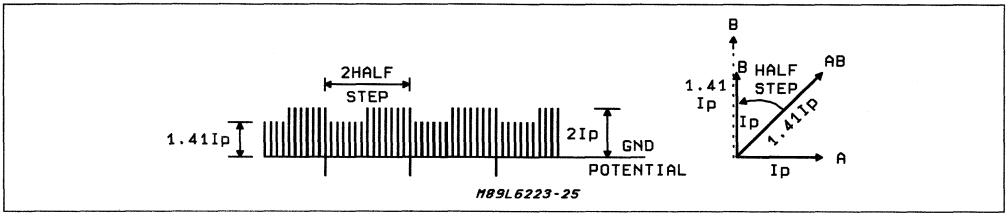
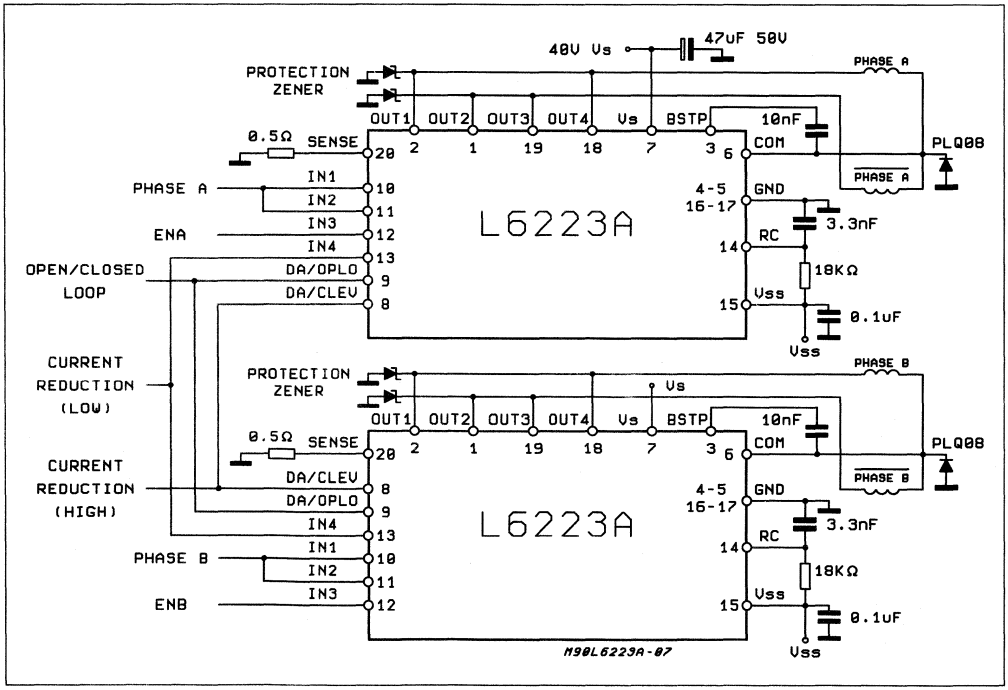


Figure 16: Typical Application Circuit using 2 devices (Paralleled configuration): the max peak current capability is of 2A/phase (R_S = 0.25Ω)



Dual Device Application
Fig. 16 shows how to drive one unipolar stepper motor by means of two L6223A Each device drives one phase of the motor. This permits doubling of the phase current. Since in this configuration each sense resistor controls the phase current (in Single only one sense resistor controls the total motor current), we have: $R_S = (V_{ref}/Ip)$ where V_{ref} is the voltage reference and Ip the phase current in the Dual that is coincident with the chopping current. The configuration in the figure shows the only possible way to parallel two L6223A. The use of another configuration can cause serious demage to the IC during the programming. The waveforms required to drive the motor in half/full step are shown in Fig. 17 and 18: as it can be seen, the two L6223A are in SIMPLIFIED MODE OPERATING configuration. The half step drive can be achieved by driving the inputs IN3 which are ENABLE inputs.

Figure 17: Inputs for Half Step drive dual device SMO.

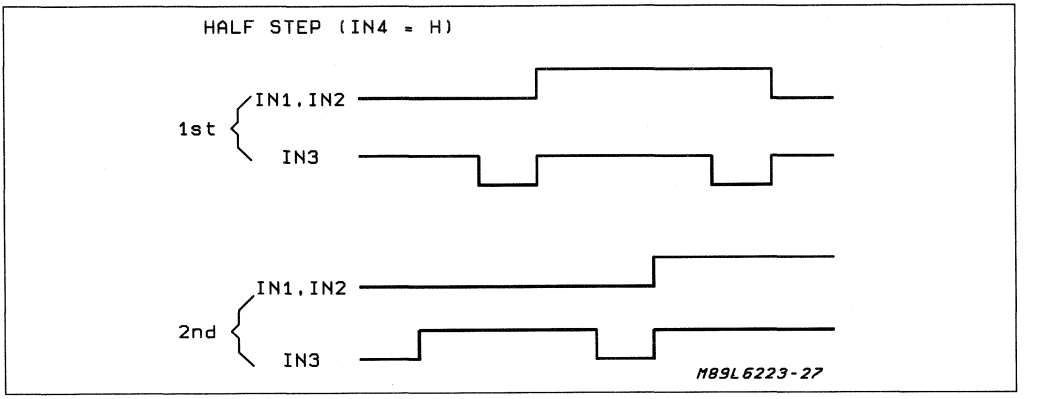
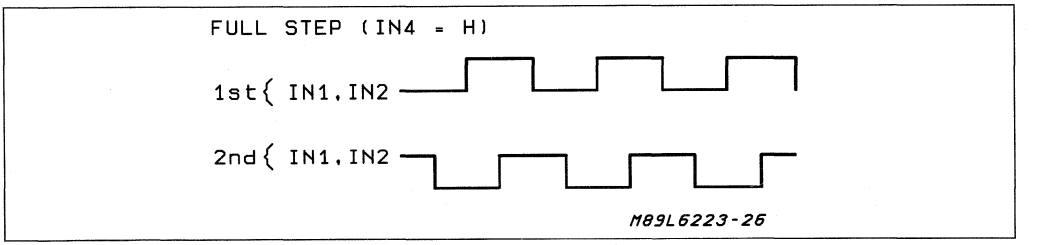
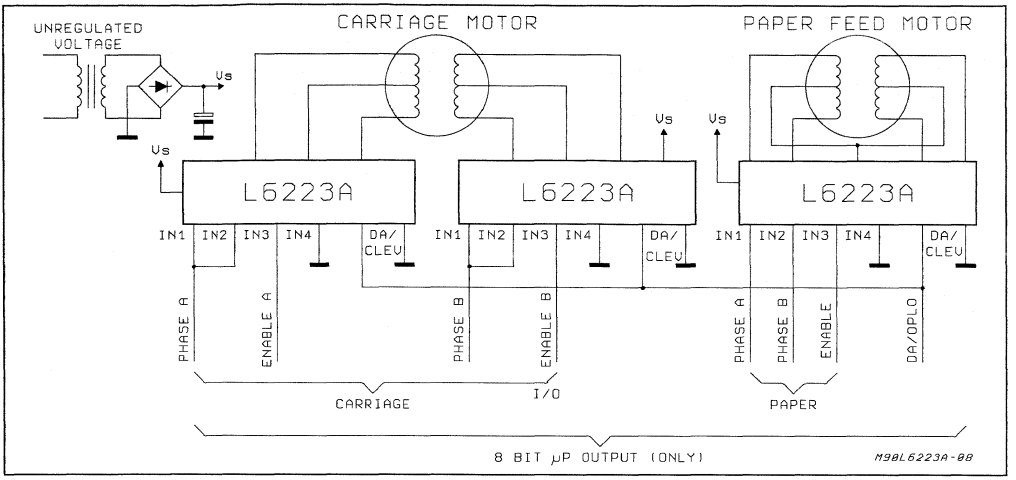


Figure 18: Inputs for Full Step drive single device SMO.



Dot Matrix Printer Motor Driver
Fig. 19 shows how to drive the paper feed and the carriage motors by means of 3 L6223A using a very low wire number. The carriage motor is driven by two paralleled L6223A, the paper feed motor, which requires a lower current, uses one L6223A. The three ICs are working in SIMPLIFIED MODE OPERATING. The inputs IN1-IN2, IN3 are driven as previously seen (Single and Dual Device configuration). The inputs IN4 and DA/CLEV are grounded so that the ICs work in reduced current levels. This means L6223A can select seven current levels through programming: four in closed loop and three in open loop. The input DA/OPLO is used to load the programming data; only the device in PROGRAMMING MODE is programmed. The two paralleled L6223A can deliver up to 2A/phase while the single L6223A, 1A/phase.

Figure 19: Dot Matrix Printer Motor Driver schematic diagram (See also fig. 10, 16).

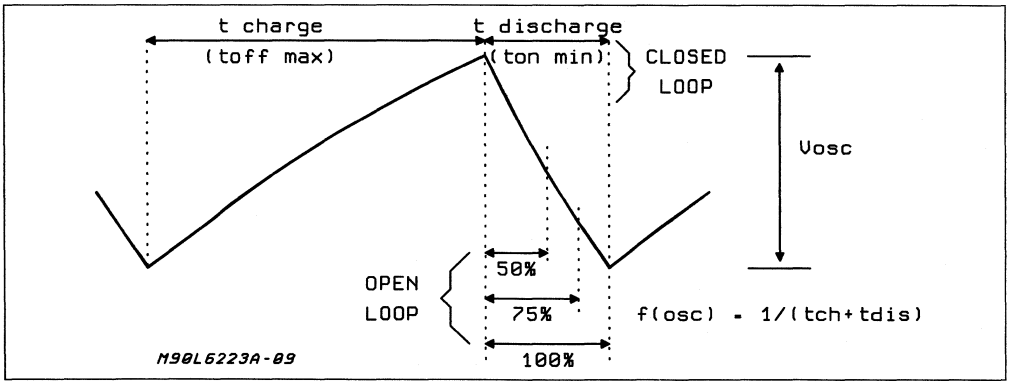


External RC Network (pin 14)

The external RC network provides the higher of the two possible chopping frequencies. The discharge time of the capacitor represents the minimum $t_{(ON)}$ available in closed loop. In open loop it is possible to select a smaller $t_{(ON)}$, (see Fig. 20).

The $t_{(ON)}$ min defines the min current the IC can supply to the motor, as well as the protection "window". This window is necessary to mask the spike generated at the beginning of each chopping period (see Fig. 21a).

Figure 20: Oscillator waveform and timing.



The window must be large enough to mask this spike, without penalizing excessively the min current control. The capacitor C mainly defines the value of the window. The mathematical formulas to calculate the approximate values are:

$f_{(osc)} = 1/(0.84 \cdot RC)$ for $R > 10k\Omega$

$t_{ON(min)} = t_{(window)} = 0.84 \cdot C \cdot R \cdot R_{in}/(R+R_{in})$

for $R_{in} = 1.2k\Omega$

where R_{in} is the resistor internal to the IC for the capacitor discharging.

Figure 21a: Relationship between capacitor discharge of the oscillator, window and sensing voltage

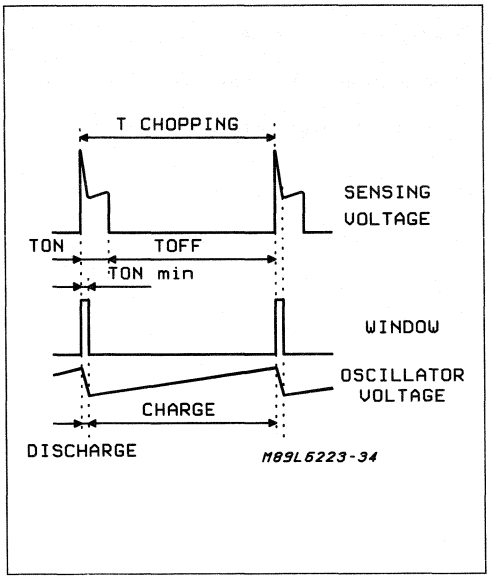
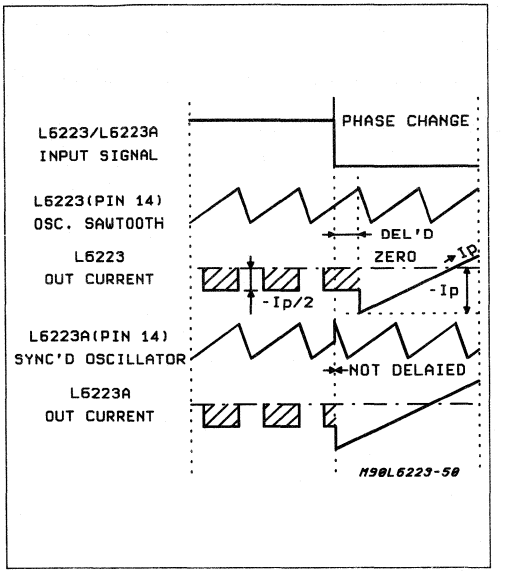


Figure 21b: Oscillator behaviour of the L6223 and of the L6223A (simplified waveforms).

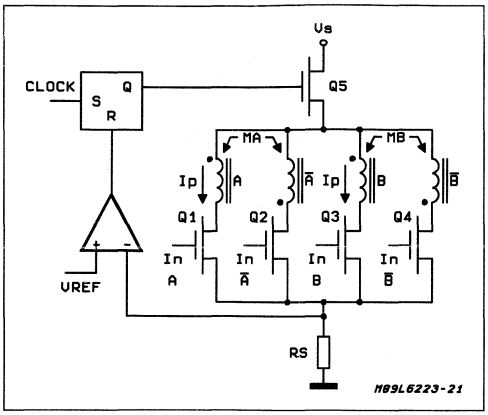


The behaviour of the oscillator at each phase change allows the L6223A to drive high speed unipolar stepper motors.
This is the main functional difference between the L6223A and the L6223 (see fig. 21b).
In the latter, the phase change starts only when the clock pulse sets the F-F (Fig. 22) that is when the capacitor voltage reaches the discharge threshold.
As a result, a variable delay between the leading edge of the input signal and the beginning of the current decay to zero can be expected.
Because of that, driving high speedy stepper motors is produced a noisy beating between chopping frequency and phase change rate.
In the L6223A as soon as the phase change is driven by the inputs, the oscillator voltage Jumps to its top level, a new discharge period is generated and the chopping transistor is switched ON (Q5 in fig. 22). The advantages are a motor phase change synchronous to the driving signal and no beating for whatever rotation speed. By setting pin 14 at a voltage equal or less than Vrs = 0.9V, when the IC is normally supplied and the oscillator is running, the 6 bit shift register is quickly reset and the power outputs are disabled: a delay of 700nsec max must be expected.
The use of this behaviour to reset the device at the turn-on is not allowed; however the reset is automatically provided by the Logic Supply Voltage crossing the threshold of 3.5V (typ.) both at the turn-ON and at the turn-OFF.

Protection

The protection zeners on the outputs protect the IC from overvoltage during chopping and phase change. Actually, at the phase change, the outputs rise to a voltage equal to $V_O = 2V_S + V_m$, where V_S is the power supply and V_m the product of the motor resistance Rm with the peak phase current Ip. Vs is doubled because in the unipolar motor we have two coupled phases connected in series(phase A and $\overline{A}$, B and $\overline{B}$) for each of the two windings of the motor (MA, MB see Fig. 22). The leakage inductance, seen from the outputs of the L6223A, can generate an overvoltage higher than V_O. To protect the IC, the zeners must be able to sustain a power of 400W for 1 microsec and must be able to conduct at a voltage V_z higher than $V_0 = 2V_{s(max)} + V_m$. It's important that during the transition, at the max operating ambient temperature, the zener conduction is guaranteed for a voltage lower than 125V (see Absolute Max Ratings). The ST-BZWO4-85 satisfies this requirement. The diode connected to the common protects this input from the undergounds due to the leakage inductances and/or the imbalancing between the phase currents.

Figure 22: Pover output configuration.



Use of the Programming Mode

A typical application of the L6223A requires driving the motor according to Fig. 23a and Fig. 23b. Starting from $t_0 = t_5$ and continuing until t_1 the motor is kept in stand-by; at time t_1 begins an acceleration period that is completed at time t_3. The motor then is driven at a contant speed until t_4, when the speed is decelerated and is stopped at $t_5 = t_0$ for a new standby period.

During these events the L6223A can be programmed several times for different working modes. The most important parameter is the current through the windings of the stepper: at the time t_0; t_1; t_2; t_3 and t_4 the current can be modified, for example, as it is shown in Fig. 23b. This behaviour allows the best motion control and, at the same time, optimizes efficency of the power output block of the I. C.

But this is not the best in terms of performances by programming: in fact, between t_1 and t_5 the device can be programmed to work in Closed Loop and to chop at half of the RC oscillator frequency during the time t_3 to t_4. In the stand-by condition the I. C. can be programmed to work in Open Loop mode where the current can be fixed by the reduction of the minimum T_{ON} time (75% or 50%) defined by the discharge time of the RC oscillator. Of course in this way the current can be modified by Supply Voltage changes; the same is not possible in Closed Loop operation where the device, in order to keep the windings current constant, modifies the T_{ON} time: wide at low V_S and narrow at high V_S. This is the reason why when the motor is driven at a constant speed (t_3 to t_4) with small current and high Supply Voltage, it could beccme necessary to program the lower chopping frequency to allow a suitable T_{ON} width otherwise the current of the windings would go out of control.

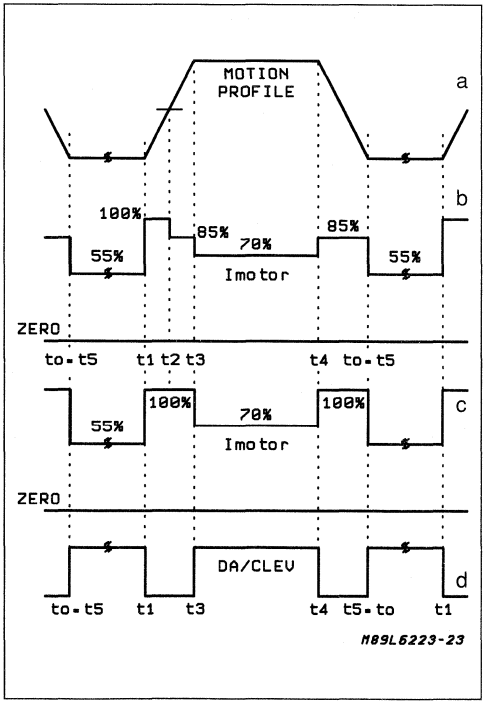
The motion profile, shown in Fig. 23a can be obtained when preferred, with only two program changes actuated while the motor is in stand-by. The current becomes as shown in Fig. 23c. The device can be programmed at $t_0 = t_5$ for I_{motor} = 55% (stand-by) and at t_1 for I_{motor} = 70%: for both the actuations, the DA/CLEV is kept high to allow the program change, while, by keeping it to zero during t_1 - t_3 and t_4 - t_5, the current is automatically select as 100% (Fig. 23d). During t_3 - t_4 the current is reduced according to the percentage programmed at the time t_1.

Power dissipation (Simplified method of calculation).

Here below the Full Step Operating Mode is considered; in addition, the following working conditions have been taken up:

1) Constant speed rotation of the driven unipolar stepper Motor.

Figure 23: a,b) Speed profile and motor current control change for the best efficency of the I.C. **c,d)** Current control change by using DA/CLEV input only, during the stand-by period.



2) Back EMF (BEMF) equal to 80% of its peak during the phase change and equal to 50% of its peak during the chopping period.

3) Constant slope of the current during t_{ON}, t_{OFF} and for power calculation during the phase change (See t_1 in Fig. 27).

4) Current imbalance supposed to be zero.

5) Current ripple during the chopping neglegible. As was previously stated, the current chopping is obtained by means of one PWM Loop that controls the charge time t_{ON} of the inductance of the windings, A and B for example in fig.22.

This time starts each clock pulse and stops when Q5 is switched OFF because of the condition:
$V_{ref} = 2\ R_S I_p$.
A factor 2 is required because the single sensing resistor R_S is crossed by the peak current I_p flowing through each of the two energized windings (A of MA; B of MB).
This configuration can produce an imbalance between the two peak currents because at the phase change the BEMF of one winding (MA) can be out of phase with respect to the BEMF of the other one (MB); in addition, an imbalance may also occur at the phase change when the Power Supply Voltage selected is too low and/or when one motor is driven with too large Lm/Rm ratio.
Nevertheless in most of the applications the dissipated power is not increased and there is no significant change in torque.
During t_{ON} the current Ip, flowing through the phase A (seg. Fig. 24), is defined by V_{ON}
$V_{ON} \cong V_S - R_{tot}\ Ip - BEMF$
where $R_{tot} = R_S + R_m + R_{DSON\ tot}$
in which R_m is the winding resistance of the phase A and $R_{DSON\ tot}$ is the sum of the R_{DSON} of Q1 and Q5: R_m and BEMF are not shown on the Figure 24.
At the end of t_{ON}, the current starts its slow decay and jumps to $I_p/2$ (see Fig. 25) since the total inductance becomes four times L_m (perfect coupling) that is the inductance of the phase A alone. The recirculation time t_{OFF} is defined by:

$$V_{OFF} \cong 2BEMF + I_P\ (R_m + R_{DSONQ1})$$

since $R_{DSONQ1} = R_{DSONOQ2}$.
The current through Q1 is shown in Fig. 26: the current ripple is on Ip and $I_P/2$ during t_{ON} and t_{OFF} respectively. It can be obtained the Duty Cycle:
$DC = V_{OFF} / (2V_{ON} + V_{OFF})$
since $2V_{ON}\ t_{ON} = V_{OFF}\ t_{OFF}$
The slow decay allows a small current ripple as earlier It is considered equal to zero. The current through the phases A and B can be seen in Fig. 27 where the InA and InB signals (see Fig. 22) are shown as well.
These two signals are 90° out of phase with each other and they are 180° out of phase with the corresponding inputs of the IC. In $\overline{A}$ and In $\overline{B}$ are not shown in the Figure.
During the time Tp the motor goes through four steps and the rotation speed V_{rot} (step/sec) can be given by:
$V_{rot} = 4/T_p$.
By considering what was stated above, the following can be applied:

1) Dissipated power by the 4 sink power DMOS (Q1 to Q4).

$$PdL \cong \frac{4\ R_{DSONQ1}\ I_p^2}{T_P}\left[\frac{T_1}{3} + \left(\frac{T_p}{2} + T_1\right)\frac{1 + DC}{2}\right]$$

2) Dissipated power by Q5 (PdH).

$$PdH \cong 4R_{DSONQ5}\ I_p^2\left[DC + \frac{T_1}{T_p}\left(\frac{4}{3} - 4DC\right)\right]$$

where the phase change duration is:

$$T_1 = -\frac{L_m}{R_{tot}}\log_e\left(1 - \frac{2R_{tot}\ I_p}{V_s - 1.6\ BEMF + R_{tot}\ I_P}\right)$$

The chopping produces little power dissipation. It's value can be approximated by:

3) $Pdch \cong 8 \cdot 10^{-3}\ V_s\ I_p$

The sum of 1) + 2) + 3) gives the dissipated power of the output stage. To obtain the total amount of dissipated power it's necessary to include the power dissipation produced by the quiescent currents I_S (from the power stage) and I_{SS} (from the Logical circuits):
$P_{do} = V_S\ I_S + V_{SS}\ I_{SS}$,
considering I_S constat versus V_S. Finally:
$P_{tot} = PdL + PdH + Pdch + Pdo$

Example

Supply Voltage	$V_S = 36V$
Logic Voltage	$V_{SS} = 5V$
Peak current (per phase)	$I_p = 0.7A$
Motor resistance	$R_m = 9\Omega$
Motor inductance	$L_m = 6mH$ at $T_{amb} = 50°C$
Rotation speed	$V_{rot} = 500$ step/sec (const)
Peak of the BEMF	BEMF = 1 Vp
Max ambient temperature	$T_{amb} = 50°C$
Max junction temperature	$T_j = 125°C$

From the Electrical Characteristics of the L6223A (Typical value):

Internal Reference Voltage	$V_{ref} = 0.5V$	
Sink DMOS R_{DSON}	R_{DSON} L = 1.2Ω	at
Source DMOS R_{DSON}	R_{DSON} H = 0.7Ω	$T_j = 25°C$
Power Supply Current	I_S = 4 mA	Worst
Logic Supply Current	I_{SS} = 20 mA	Case

From Fig. 3 (see pag. 6) the following is obtained:
$\alpha \cong 1.65$ at $T_j = 125°C$.
The DMOS ON-Resistances become (worst case):

From Fig. 3 (see pag. 6) the following is obtained:
$\alpha \cong 1.65$ at $T_j = 125°C$.
The DMOS ON-Resistances become (worst case):
R_{DSON} L = α 1.2 = 2Ω
R_{DSON} H = α 0.7 = 1.15Ω
$R_S = 0.36\Omega$
$R_{tot} = 12.5\Omega$
$V_{ON} = 26.24V$ (During the chopping)
$V_{OFF} = 9.7$ (During the chopping)
DC = 15.6%
$T_p = 8$ msec
$T_1 = 250\mu s$ (During the phase change)
PdL = 1.1W
PdH = 0.4W
Pdch = 0.20W
Pdo = 0.24W
At last:
$P_{tot} = 1.94W$

The needed thermal resistance between junction and ambient must be equal to:

$$R_{thj-amb} = \frac{T_{jmasc} - T_{ambmasc}}{P_{tot}} \cong 39°C/W$$

The worst case here considered requires an heatsink of 25°C/W. The calculation of the power dissipation by considering the current imbalance and by simulating a typical motion needed to carry the head of a printer for example, becomes full of difficulties. The use of the Personal Computer is helpful in such a case: few examples are shown from Fig. 28ab until Fig. 31 ab.
Each figure shows the Application Datas and one diagram where the Total Dissipated Power versus the peak of the motor current is plotted.

Figure 24: Motor current Ip during t_{ON} (phase MA; Q5 and R_S sre common whit the phase MB).

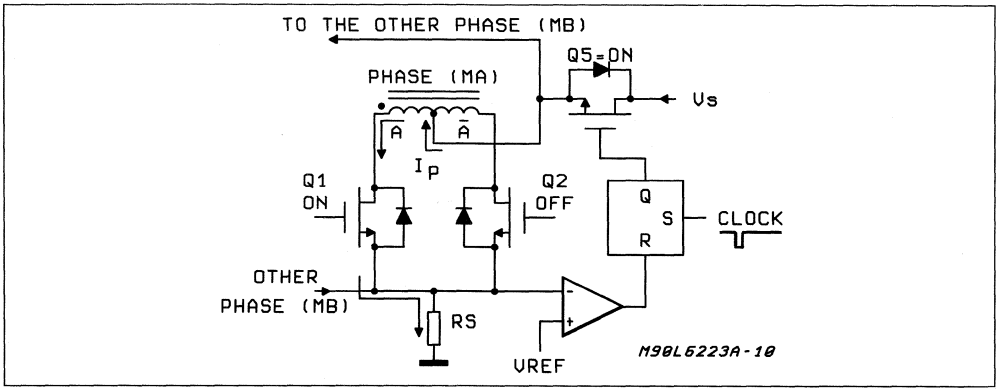
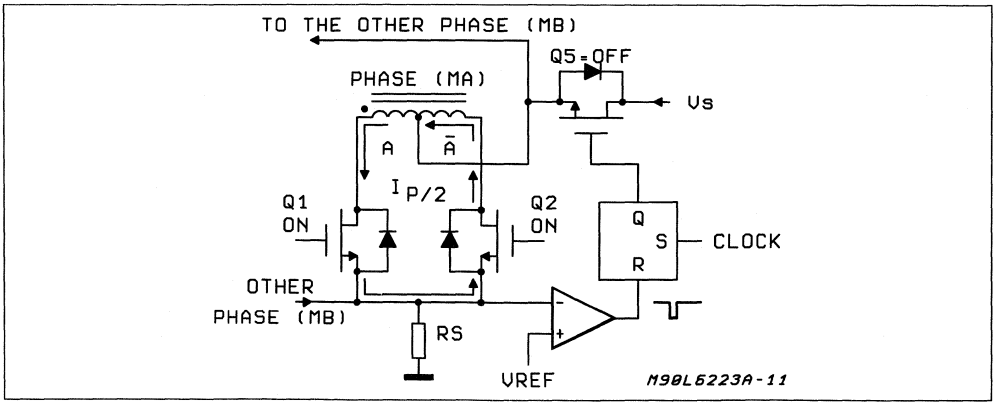


Figure 25: Slow decay of the motor current $I_p/2$ during t_{off} (phase MA).



A max Ambient temperature of 70°C and a max junction temperature of 150°C have been considered for a few applications using one single device and a dual device configuration to drive one stepper motor in the Full Step Mode.
The calculations consider three different conditions of heatsinking: the package with minimum dissipating copper area on the p.c.b. ($R_{thj\text{-}amb}$ =

Figure 26: Phase current waveform during chopping: the current decay during t_{OFF} is halved.

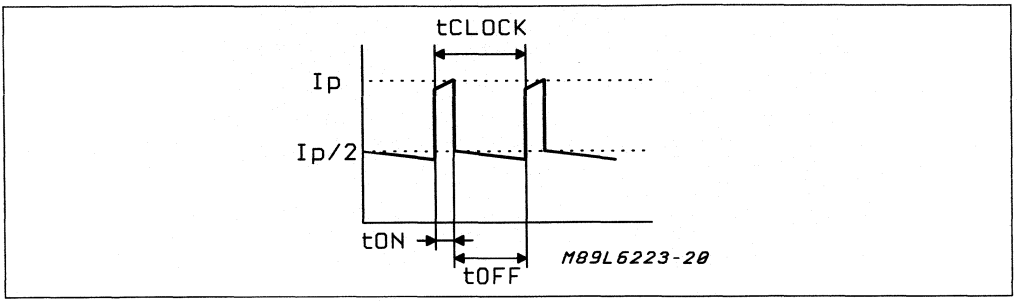


Figure 27: Simplified waveforms of the current through the phase A (winding MA) and through the phase B (winding MB). See also fig.22.

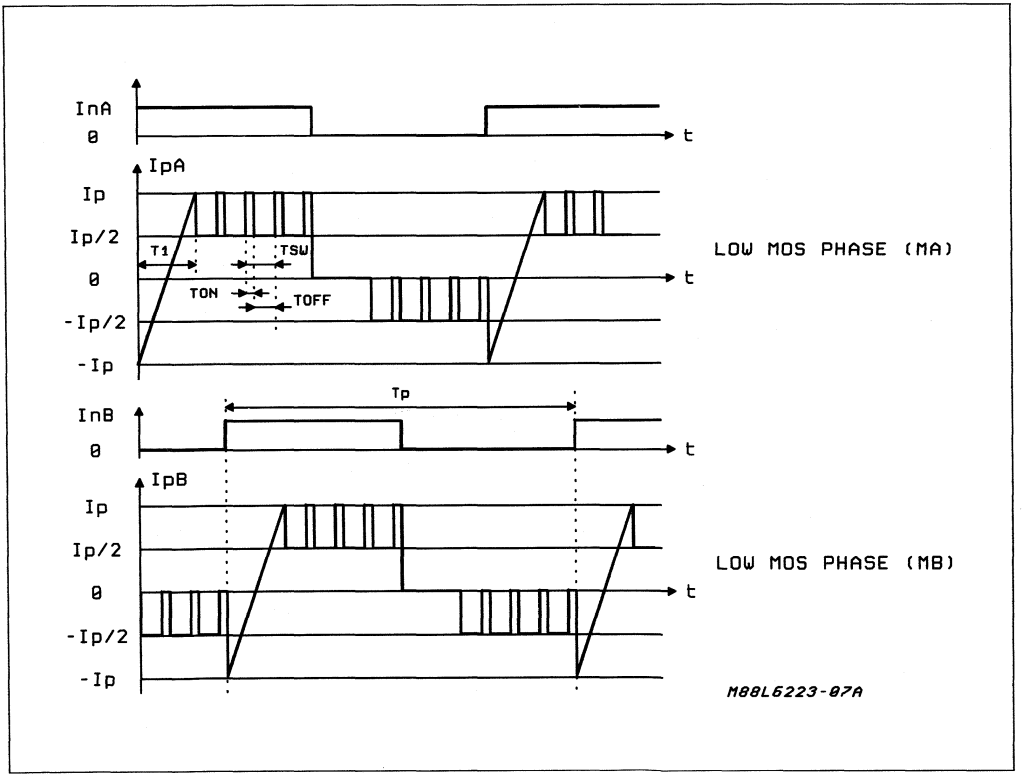


Figure 28a: Single L6223A slow speed, Application Data.

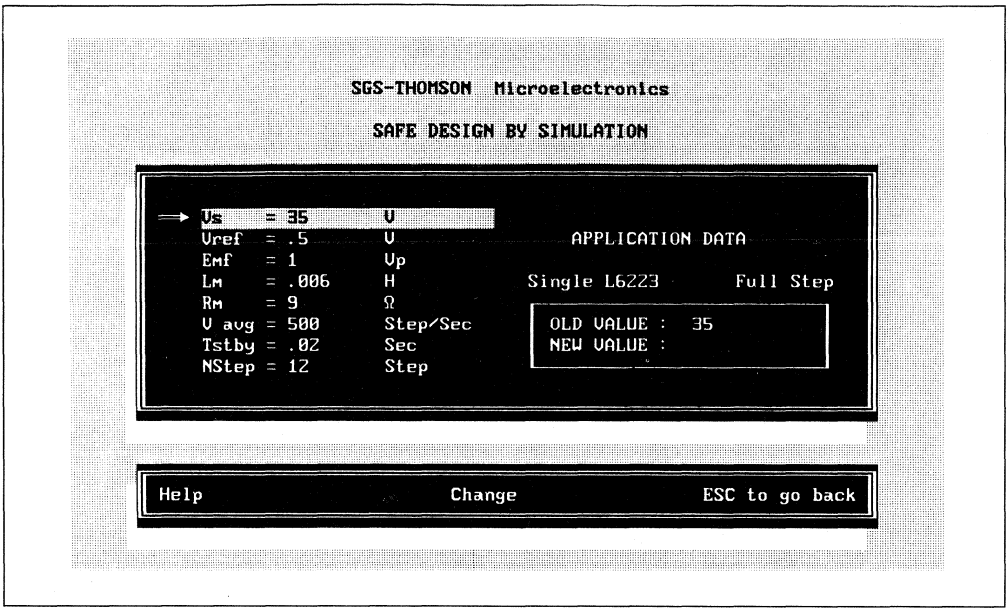


Figure 28b: Total Power Dissipation. The vertical indicator tells us the max value of the current we can supply to the windings (Ip = 0.8A). The peak current corresponding to the flat side of each of the three shown trends is not allowed

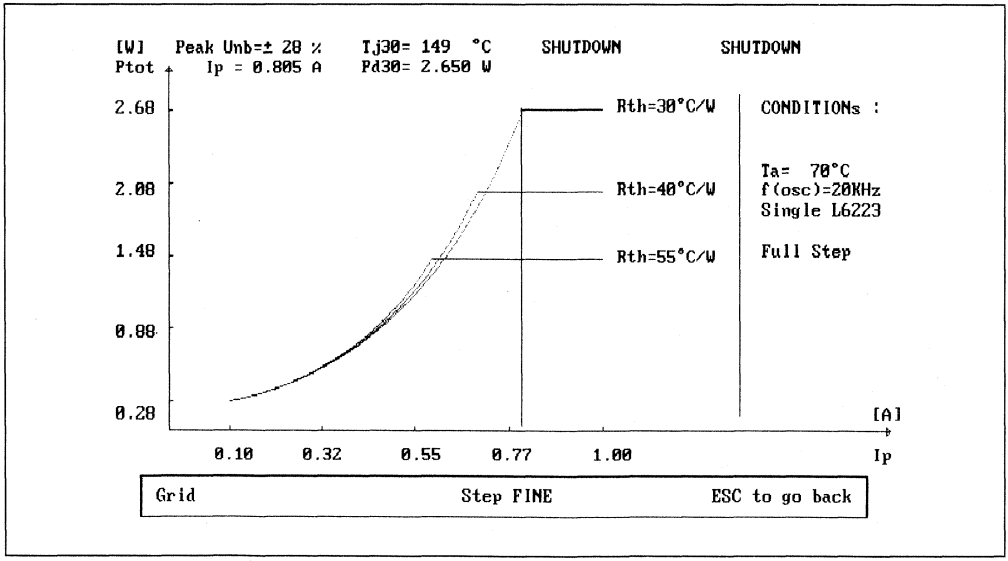


Figure 29a: Single L6223A high speed, Application Data.

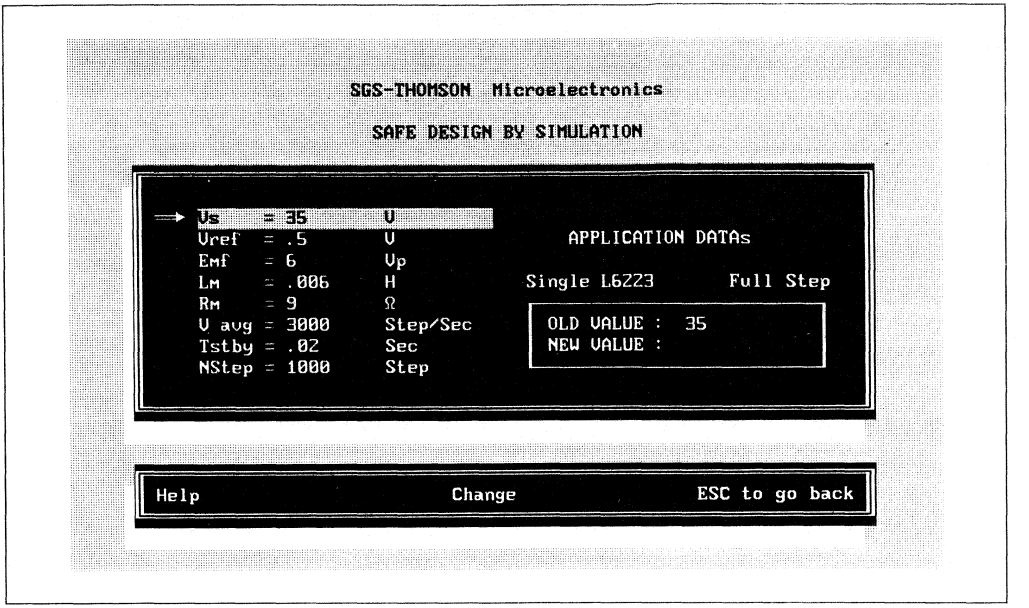


Figure 29b: Total Power Dissipation.

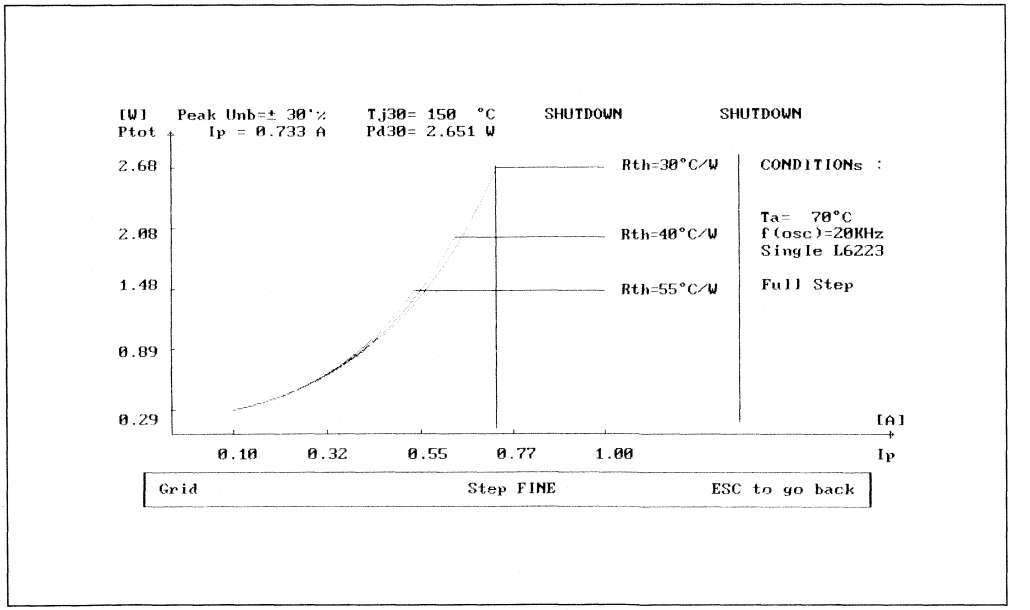


Figure 30a: Dual L6223A slow speed, Application Data.

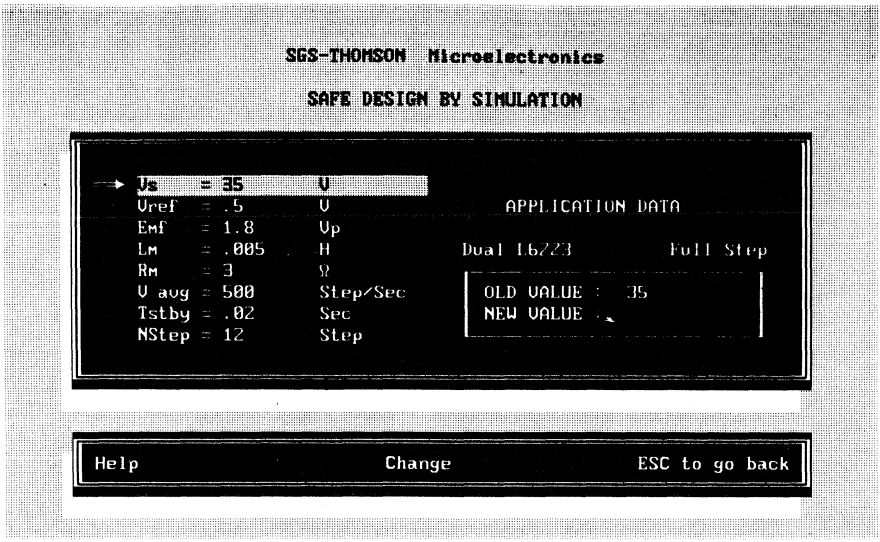


Figure 30b: Total Power Dissipation.

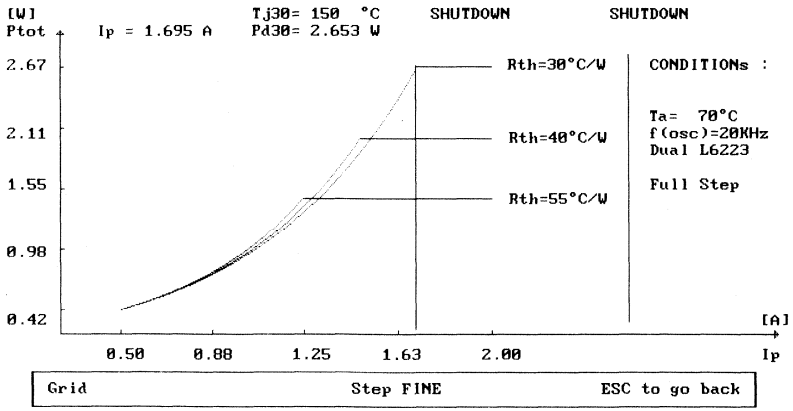


Figure 31a: Dual L6223A high speed, Application Data.

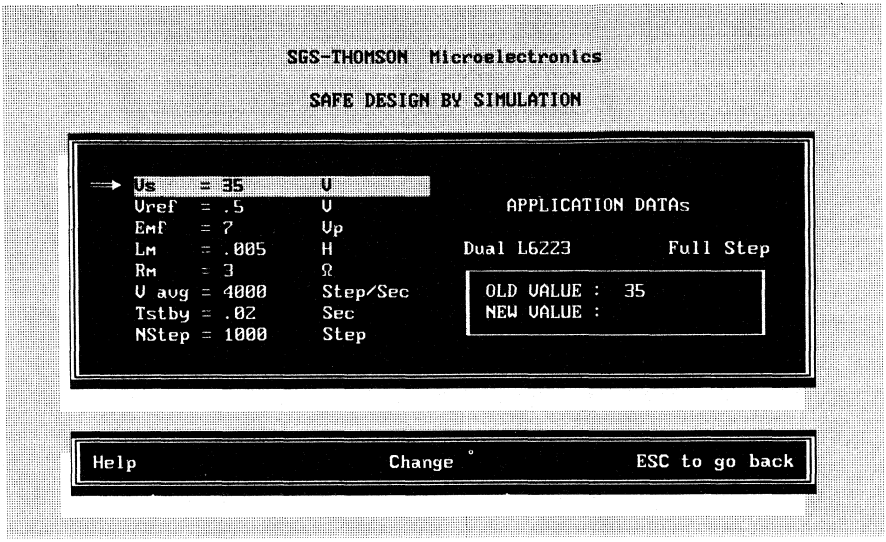
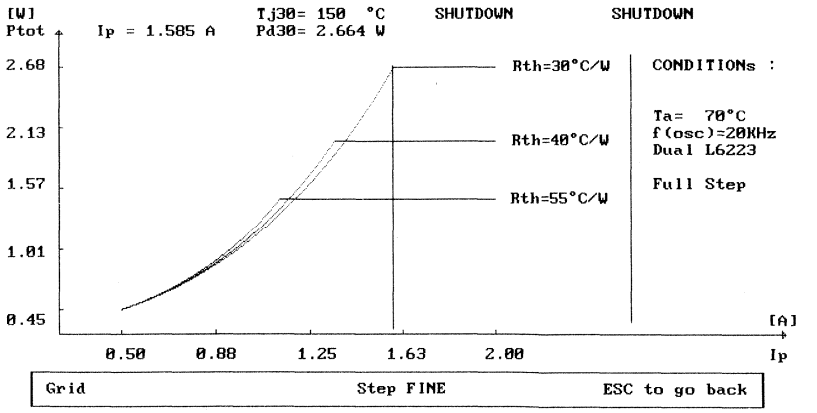


Figure 31b: Total Power Dissipation.



55°C); the copper side of 6 cm^2 ($R_{thj-amb}$ = 40°C/W - See Fig. 34) and the additional heatsink ($R_{thj-amb}$ = 30°C/W).

Matching the L6223A with the motor.
For the correct design of the application the following notes must be considered.

* For low motor resistance and high supply voltage the L6223A minimum duty cycle may limit the minimum current at a value higher than requested.
  In this case we suggest to reduce the window protection time changing the RC oscillator network. (See Fig. 21a and External RC Network).
* Only in single device application, for very low motor resistance, a large current imbalance may affect the correct motor rotation. Motor resistance value higher than 7 Ohm are generally recommended for 35V Power Supply.
* The correct motor winding execution is very important for the motor and the L6223A efficiency. A simple test is the measurement of the stray inductance between the central tap and the ends shorted together of each winding. Theoretically the inductance would be zero; values higher than 50μH may show poor motor quality.

Computer Aided Development Board
An improvement in the application development and in system debugging can be obtained by means of the Personal Computer.
Interfacing the appliction with the PC, the motor can be driven directly by this in real time operation. This permits the testing in very short time and a lot of different motion configurations, during application debugging and optimization. Moreover, by paralleling more application boards, an efficient reliability test can be implemented.
The development board designed to drive L6223A in Single and Dual Device configuration is shown in Fig. 32a-b. Fig. 33 is the corresponding electrical circuit. On the board are mounted three L6223A: two for the Dual Device configuration and one for the Single Device. The three connectors J1, J2, J3 allow the application board to be interfaced with the PC and to be paralleled with another one. The remaining connectors provide the interface with the motor and the power

Figure 32a: L6223A p.c.b. (components side).

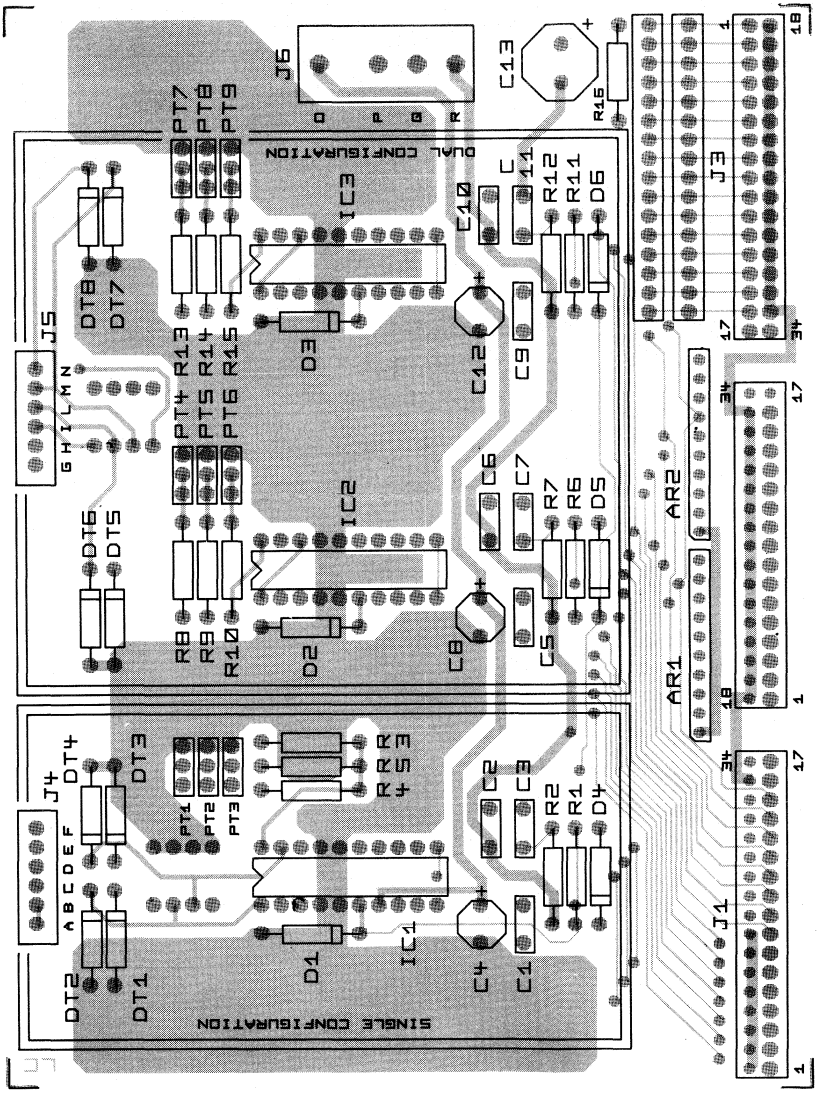


Figure 32b: L6223A p.c.b. (back side).

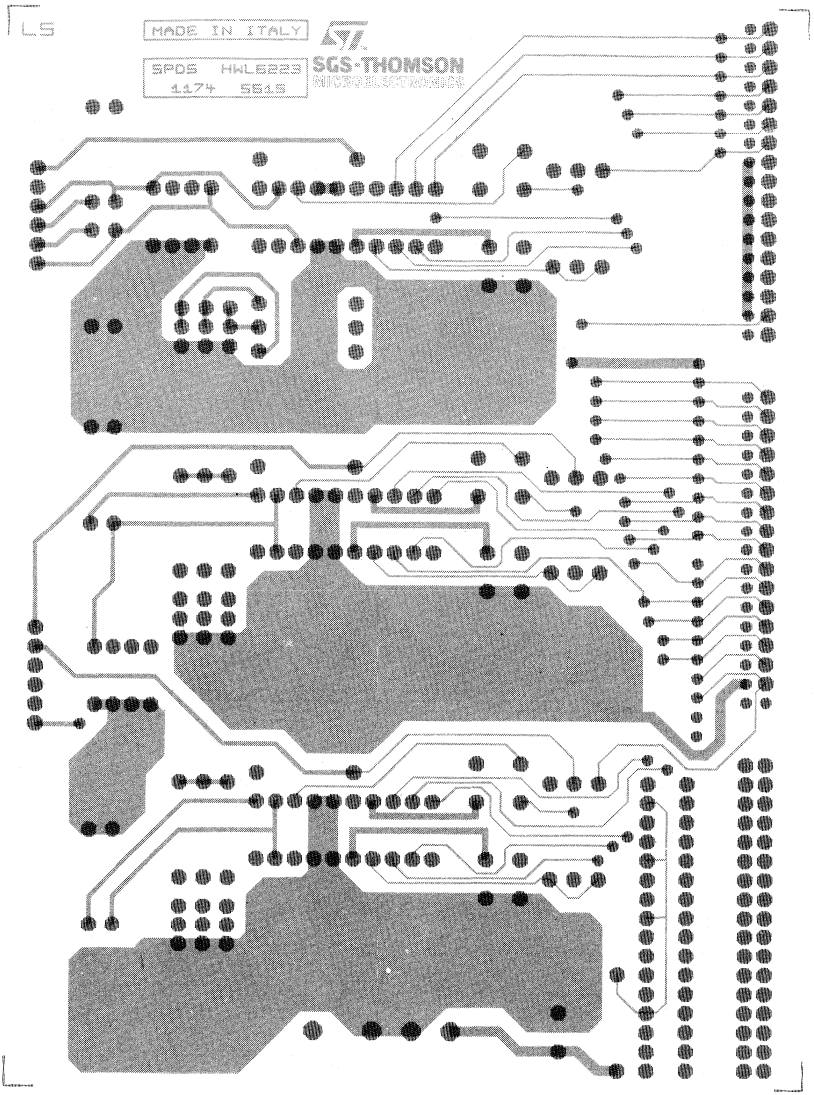


Figure 33: L6223A Development Board schematic diagram.

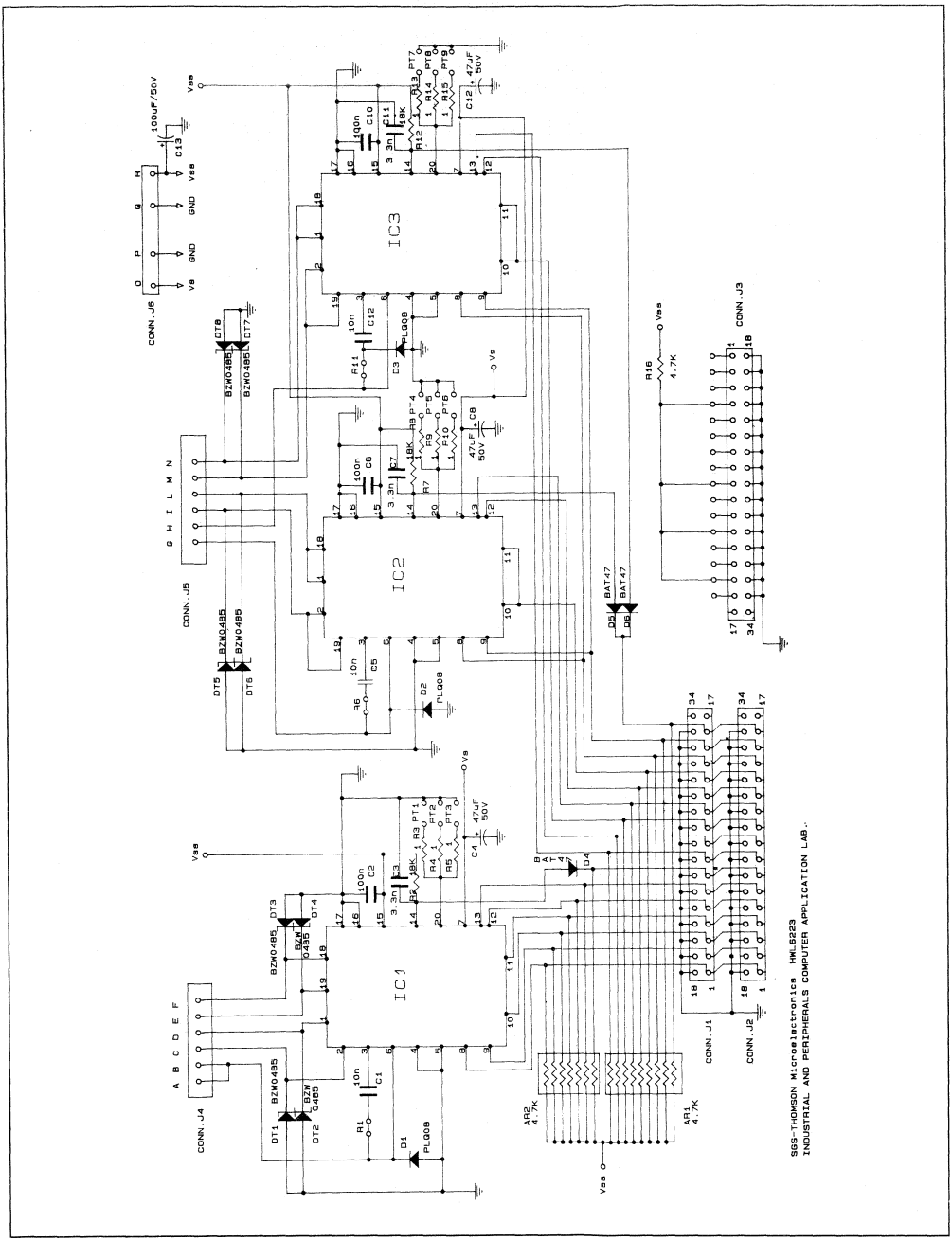


Figure 34: R_{th} with two "on board" square heatsink vs. side l.

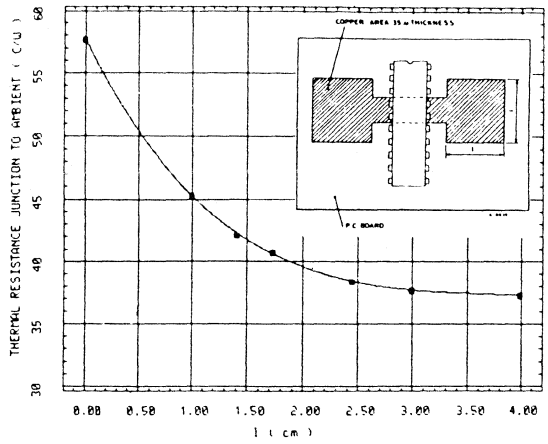
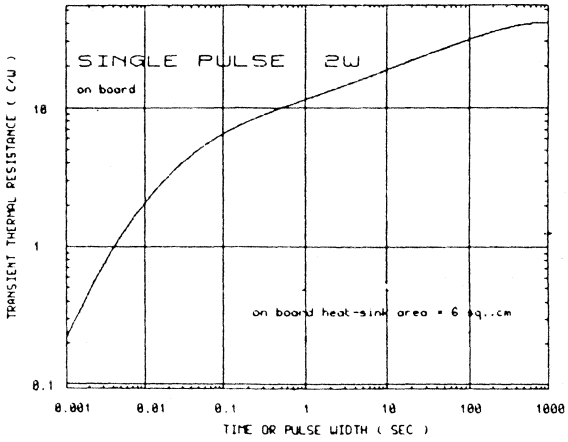
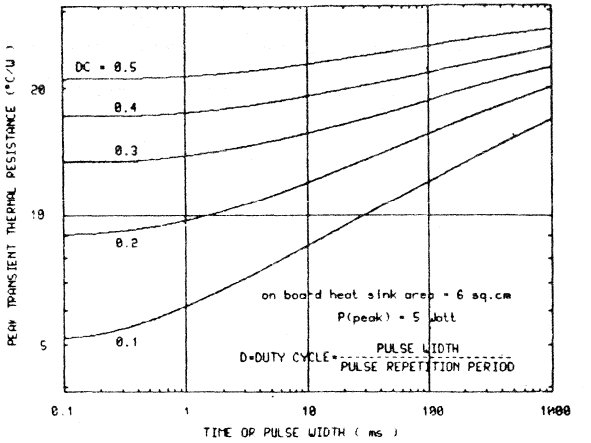


Figure 35: Transient thermal resistance for single pulses



Thermal characteristics.
The p.c.b. copper size needed for a defined thermal resistance between junction and ambient is shown in Fig. 34. Fig. 35 and Fig. 36 are useful to estimate the typical thermal resistance junction to ambient for a single pulse of peak power and for a repetetive peak respectively.

Figure 36: Peak transient Rth pulse width and Duty Cycle.



Notes on the p.c.b. design.

We recommend to observe the following layout rules to avoid application problems associated with ground loops and anomalous recirculation currents. The by-pass capacitors for the power and logic supply must to be kept as close to the IC as possible.

It's important to separate on the PCB board the logic and the power grounds avoiding that grounds traces of the logic signals cross the ground traces of the power signals. The starpoint grounding, the point of the board in which the logic ground meets the power ground. should be kept far enough away from where the power ground traces terminate to ground (sense resistors and protection zener diodes traces). This avoids interference with the logic signals. Because the IC uses the board as a heatsink the dissipating copper area must be sized in accordance with the required value of $R_{thj\text{-}amb}$. It's important to provide a good filter for the logic supply, especially for the resistor of the oscillator network. In addition, the capacitor ground of the RC network must be as clean as possible. When the ground is used also to heatsink, it is helpful to use either a polistyrin capacitor or one with a low temperature coefficient. The value of the bootstrap capacitor is not a critical parameter, nevertheless the use of a capacitor of 10nF±20% is recommended. A non-inductive resistor is the best way to implement the sensing, but when that is not possible, more metalfilm resistors of the same value can be paralleled.

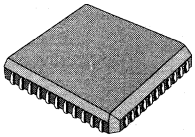
SGS-THOMSON MICROELECTRONICS

L6232A

SPINDLE DRIVER

ADVANCE DATA

- 2.5A MAXIMUM PEAK CURRENT
- CONTROLLED SLEW RATE
- CENTRAL CHARGE PUMP
- PWM AND LINEAR MODES
- CUTOFF TIME USER CONFIGURABLE
- FAST, FREE-WHEELING DIODES ON CHIP
- OVER-TEMPERATURE PROTECTION
- BRAKE FUNCTION INPUT

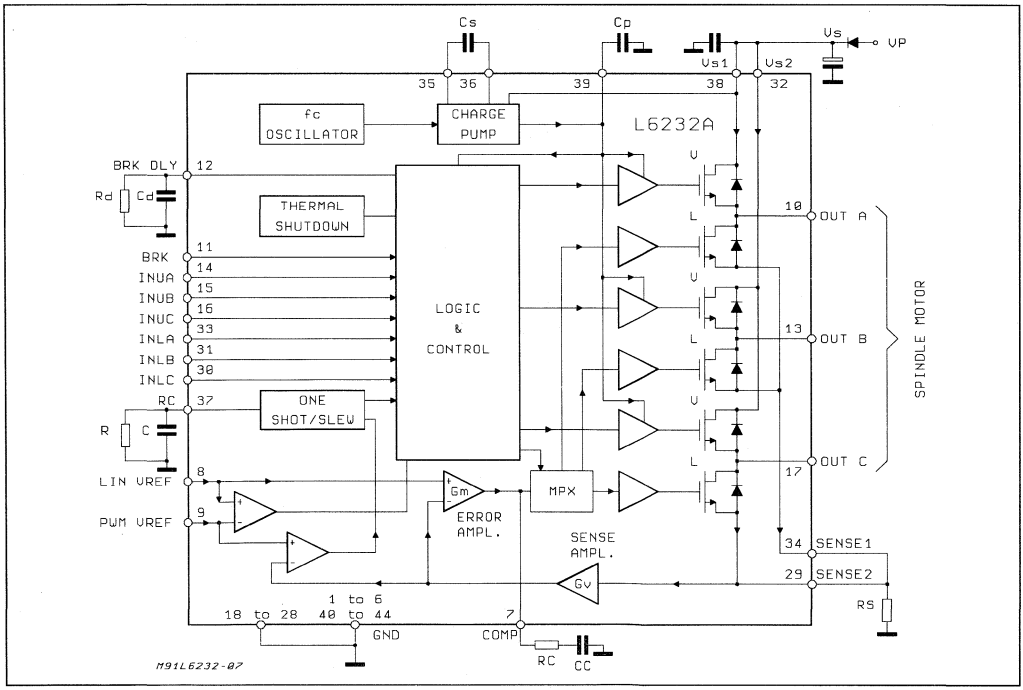


PLCC44
ORDERING NUMBER: L6232A

DESCRIPTION

The L6232A is a triple half bridge driver intended for use in brushless DC motor applications. This part can be used to form the power stage of a three-phase, brushless DC motor control loop, and is especially useful for disk drive applications. Power drivers are Integrated DMOS transistors and feature fast recirculating diodes as an integral part of their structure. The logic inputs are TTL-level compatible, with internal pull-up, allowing interfacing to open collector outputs. All necessary circuitry to perform PWM and linear motor speed control is included. A central charge pump is utilized to drive the upper DMOS transistors, and also to power the braking function. The L6232A is packaged in PLCC44.

BLOCK DIAGRAM

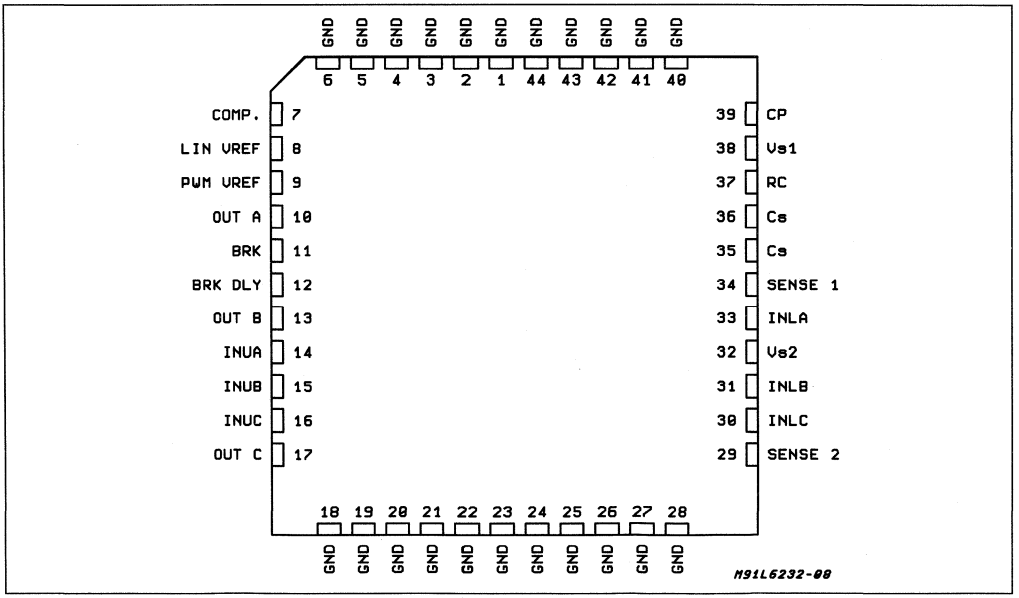


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Name	Function
1 to 6	GND	Common Ground. Also provides heat-sink to PCB.
7	COMP	External compensation for error amplifier.
8	LIN Vref	Input for Reference Control voltage in LIN mode.
9	PWM Vref	Input for Reference Control in PWM mode.
10	OUTA	DMOS Half-bridge A Out.
13	OUTB	DMOS Half-bridge B Out.
17	OUTC	DMOS Half-bridge C Out.
11	BRK	Active LOW logic input that triggers the delayed brake.
12	BRK DLY	External RC network for the brake delay.
14	INUA	Logic Inputs to turn on the upper drivers (Active Low).
15	INUB	
16	INUC	
18 to 28	GND	Common Ground. Also provides heat-sink to PCB.
29, 34	SENSE	Output for current sense resistors.
30	INLC	Logic inputs to turn on the lower drivers (Active High).
31	INLB	
33	INLA	
32, 38	V_S	Supply Voltage.
35, 36	C_S	External Charge Pump Capacitor.
37	RC	Cutoff Time RC Network in PWM mode. The Resistor value is also used to define the slew-rate in linear mode (LIN).
39	C_P	External Main Charge Pump capacitor.
40 to 44	GND	Common Ground. Also provides heat-sink to PCB.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DS\ sus}$	Peak Output Sustaining Voltage	18	V
V_S	Supply Voltage	15	V
$V_{O\ peak}$	Output Peak Voltage (t_{pK} = 5 µsec; 10% d.c.)	18	V
V_{Cp}	Charge Pump Input Voltage	30	V
V_i	Logic Input Voltage	-0.3 to 7	V
V_{REF}	PWM VREF--LIN VREF Input Voltage	-0.3 to 7	V
V_{is}	Sense Input Voltage	-1 to 7	V
I_p	Sink-Source Peak Output Current(*)	3.5	A
I_O	Sink-Source DC Output Current	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 60°C)	1.8	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (**)	Max.	50	°C/W

Notes
(*) Pulse width limited only by junction temperature and by the transient thermal resistance
(**) Mounted on board with minimized dissipating copper area

ELECTRICAL CHARACTERISTICS (See the block diagram, V_S =12V, R = 100KΩ; C = 180pF; T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10.5	12	13.5	V
I_S	Quiescent Supply Current	BRK = L; INUA = INUB = INUC = L; INLA = INLB = INLC = H; Table 1		0.3	0.5	mA
		BRK = H; INUA = INUB = INUC = H; INLA = INLB = INLC = L; Table 1		4	6	mA
I_{OL}	Output Leakage Current	V_O = V_S = 13.5V			1	mA
R_{DSon}	Sink Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
R_{DSon}	Source Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
V_F	Body Diode Forward Drop (sink and source)	I_{DS} = 1A (see Fig. 6)		1	1.5	V
$t_{d(BRK)}$	Brake Delay Time	See Fig. 1, 3; note1		210		ms
T_{BRK}	Braking Time		10			s
$I_{B(LIN)}$	LIN Vref Input Bias Current	LIN V_{ref} = 0.4 to 5.5V		400	800	nA
$I_{B(PWM)}$	PWM Vref Input Bias Current	PWM V_{ref} = 0.4 to 5.5V		400	800	nA
LIN V_{ref}	Reference Voltage Input	Note 2; R_S = 0.5Ω I_{motor} (PWM) = 1A I_{motor} (LIN) = 200mA		2		V
PWM V_{ref}				0.4		V
G_v	Sense Amplifier Voltage Gain	PWM V_{ref} = 2.5V, LIN V_{ref} = 0.4V, R_S = 0.5Ω; Note 2	3.8	4	4.2	V/V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_m	LIN Error Amplifier Transconductance			0.8		mA/V
Zout	Error Amplifier Output Impedance			2		MΩ
V_{INH}	Logic Input Voltage BRK; INUA; INUB; INUC; INLA; INLB; INLC		2			V
V_{INL}					0.8	V
$I_{INH(leak)}$	Logic Input Current BRK; INUA; INUB; INUC; INLA; INLB; INLC	V_i = 2.7V			-1	mA
I_{INL}		V_i = 0.4V			-0.1	mA
t_{donU}	Upper/Lower Turn-on Delay	Table 1 see Fig. 3		0.7		µs
t_{donL}				0.15		µs
t_{doffU}	Upper/Lower Turn-off Delay			15		µs
t_{doffL}				0.5		µs
dV/dt	Source DMOS Slew-Rate (PWM)	see Fig. 3	10			V/µs
dV/dt	Source DMOS Slew-Rate (LIN)	see Fig. 3			1	V/µs
dV/dt	Sink DMOS Output Turn-off Slew-Rate	Note 3; R = 100KΩ		0.1		V/µs
F_C	Internal Clock Frequency			380		KHz
T_{off}	PWM Cutoff Time	R=100KΩ; C=180pF, Note 4; see Fig. 2		12		µs
T_{sd}	Shutdown Temperature			160		°C
T_{sdr}	Recovery Temperature			120		°C

Notes:

1) The Head Park time must be shorter than the Brake Delay time $t_{d(BRK)} = R_d C_d$
2) Both in PWM and in LIN mode the Ref. Voltage must agree to $V_{ref}=G_V R_S I_{motor}$
3) The resistance of the RC network defines the dv/dt value.
4) $t_{off} = 1.8RC + 6 \cdot 10^{-6}$

Table 1

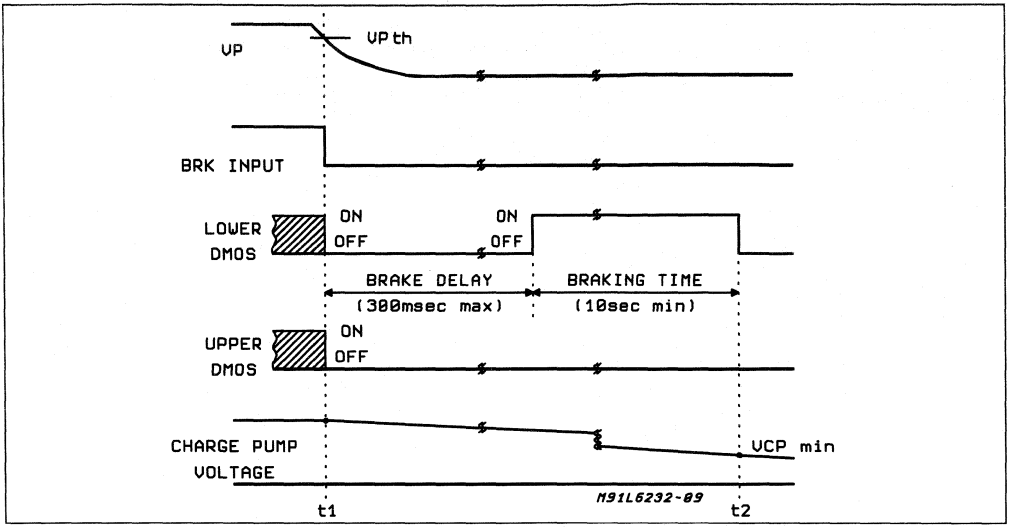
INPUT STATE						OUTPUT STATE		
INUA	INUB	INUC	INLA	INLB	INLC	A	B	C
L	L	L	H	H	H	*	*	*
L	L	L	L	L	L	H	H	H
H	H	H	L	L	L	*	*	*
H	H	H	H	H	H	L	L	L

H = The Upper DMOS is ON

L = The Lower DMOS is ON

* = Tristate condition

Figure 1: Brake Delay and Braking timing of the L6232A. At the time t1 a VP Powerdown threshold detector drives low the BRK input; at time t2 the Charge Pump voltage becomes inadequate to maintain ON the lower DMOS.



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The commutation sequence is provided by the user via six inputs. INUA,INUB,INUC turn on the three upper DMOS drivers when held at logic LOW, and inputs INLA,INLB,INLC turn on the three lower DMOS drivers when held at logic HIGH.

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in wich Gv is the voltage gain of the sense amplifier. In linear mode, the current is regulated by a linear control loop wich drives the lower DMOS. Compensation of the linear control loop is achieved by connection of a series network (Rc,Cc) from the transconductance amplifier output (Gm) and ground. Control is passed to each lower DMOS in succession during the commutation sequence(MPX).

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A typical application configuration of the L6232A driving a three-phase brushless DC motor is shown in Fig.3. The spindle motor is a 4 ohm-2mH per phase, star connected. This load requires a suitable compensation of the linear control loop that can be achieved by Rc= 10 Kohm and Cc= 10nF (R3;C8). Changing the motor characteristics, the RcCc network would be modified for the best performances of the system. At the start-up the spindle is driven in PWM mode fixed toff time.

The off-time is calculated by the formula :

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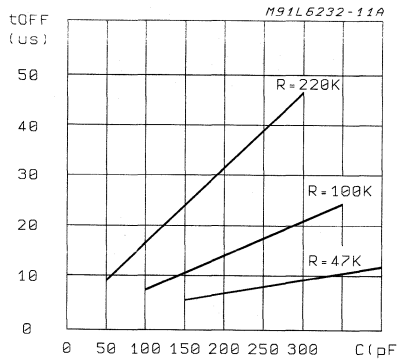
See fig.2 for a quick choice of the needed capacitor, after the resistor has been fixed. The value of the resistor defines the rate at which the upper and lower drivers turn-off during linear mode operation to avoid EMI effects. During turn-off, the slew rate is constant for the sink stage, while it has a varying slope for the source stage because of the non linear change of the gate to source impedance of the DMOS transistor. Practically, the

Figure 2: Typical t_{off} vs. Capacity of C



slowest slew rate is obtained at the sink transistor switch-off time (see fig. 5), then it increases during the first period of the source transistor switch-off (source,1st) and it becomes the fastest during the final portion of the turn-off duration (source, 2nd). The PWM to linear mode of operation is switched by decreasing the LIN Vref level under the PWM Vref value that could be fixed and calculated by:

$$PWM\ Vref = 4\ Rs\ Ip$$

where Ip is the peak chopping current in the motor windings. Of course, when the required RPM is reached, it become of no need a strong torque and the LIN Vref starting from a value higher than the calculated PWM Vref, decreases to the value :

$$LIN\ Vref = 4\ Rs\ Im$$

where Im, smaller than Ip, is the needed motor current to keep constant spin. This last reference voltage is generally a PLL output driven by speed transducers coupled to the spindle (like Hall effect sensors or BEMF processors). To drive the upper DMOS and during the brake function a voltage higher than the supply Vs is needed. The charge pump integrated in the L6232A keeps C3 at the correct voltage. To guarantee efficient braking of the motor , C3 must be chosen of adeguate quality (very high equivalent parallel resistance). C4 can be a ceramic disk capacitor . The typical application od the L6232A is in HDD systems on which there is the need to park the Read-Write Heads before the motor braking. This behavior is possible with the circuit of Fig.3. At Power Supply switch-off (see Fig. 1), VP falls down and drives down the BRK input (Active Low). D1 insulates the L6232A from the power suppy output while the power output stage is switched in a high impedance state. The spindle motor acting as a three-phase alternator supplies the Heads voice coil motor driven through integrated diodes that rectifie the EMF. After a delay longer than the parking time, the lower output DMOS are switched-on and the spindle motor is braked. The brake delay time is tipically

150 msec and it is defined by :

$$td(BRK) = 1.4\ R1\ C6$$

The sensing resistor value is generally lower than 1ohm, but a wire wounded type must be avoided. In Fig.3 the 0.33 ohm sensing resistor is shown as three parallel 1ohm metal film resistors. Care must be taken in the PC Board design particularly about ground loops and ground copper area. The typical Thermal Resistance junction to ambient versus PC Board copper area (Fig.7) is shown in Fig 8. For Transient Thermal Resistance see Fig. 9.

Figure 3: Typical Application Circuit

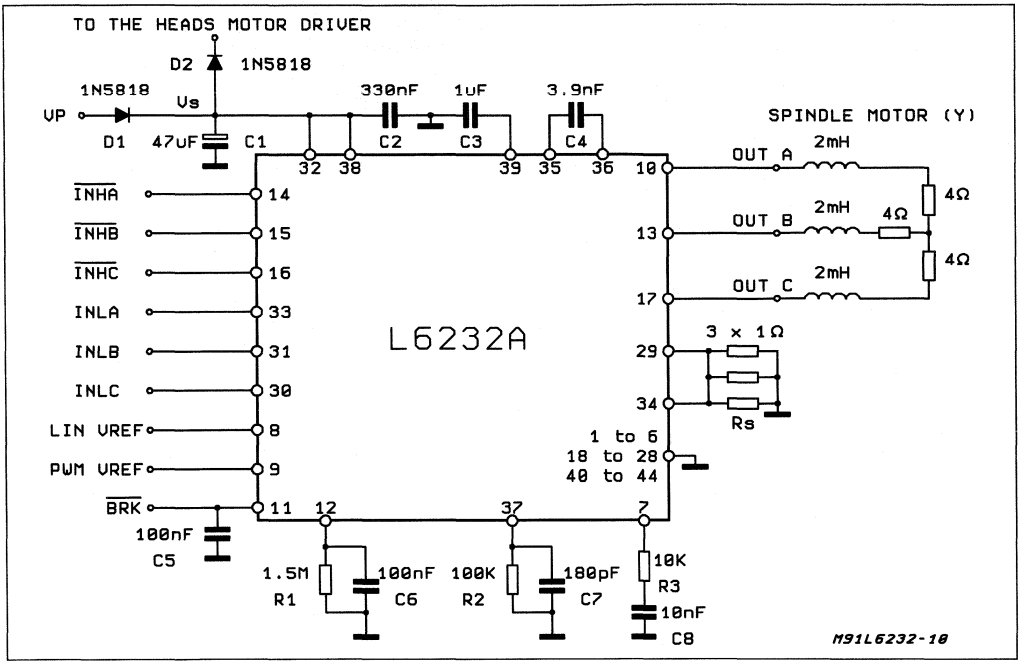


Figure 4: Typical Normalized $R_{DS\,(on)}$ vs. Junction Temperature

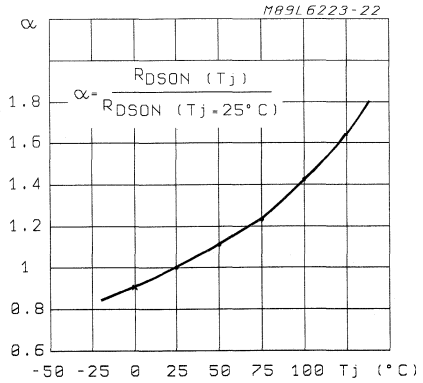


Figure 5: Output Voltage Slew Rate Control vs. $1/R_2$ Value

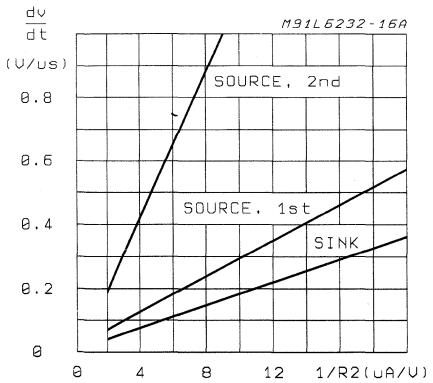


Figure 6: Typical Body Diode Forward Drop vs. Drain to Source Current.

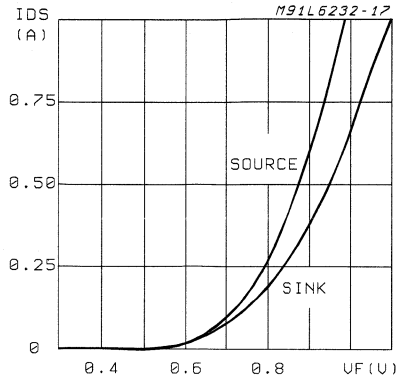


Figure 7: On Board Dissipation Copper Area Size

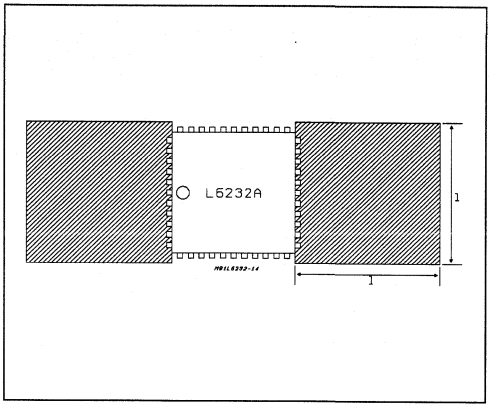


Figure 8: Typical $R_{th\ j\text{-}amb}$ vs. On-Board Heatsink Side l.

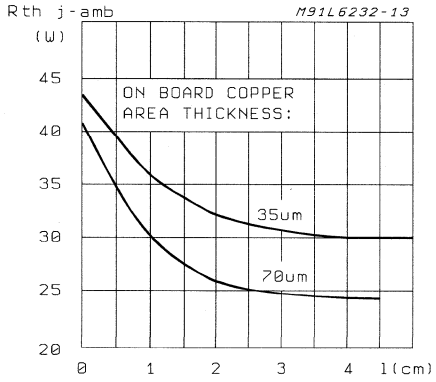
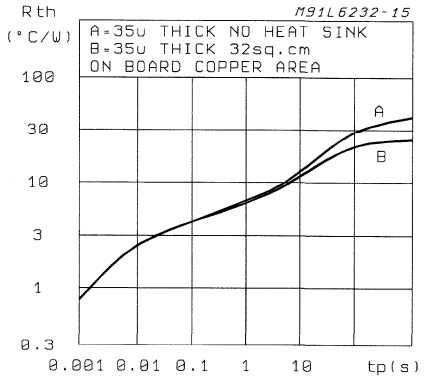


Figure 9: Typical Transient R_{th} in Single Pulse Condition.



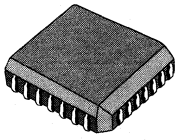
SGS-THOMSON MICROELECTRONICS

L6232B

SPINDLE DRIVER

ADVANCE DATA

- 1.5A MAXIMUM PEAK CURRENT
- CONTROLLED SLEW RATE
- CENTRAL CHARGE PUMP
- PWM AND LINEAR MODES
- CUTOFF TIME USER CONFIGURABLE
- FAST, FREE-WHEELING DIODES ON CHIP
- OVER-TEMPERATURE PROTECTION
- BRAKE FUNCTION INPUT

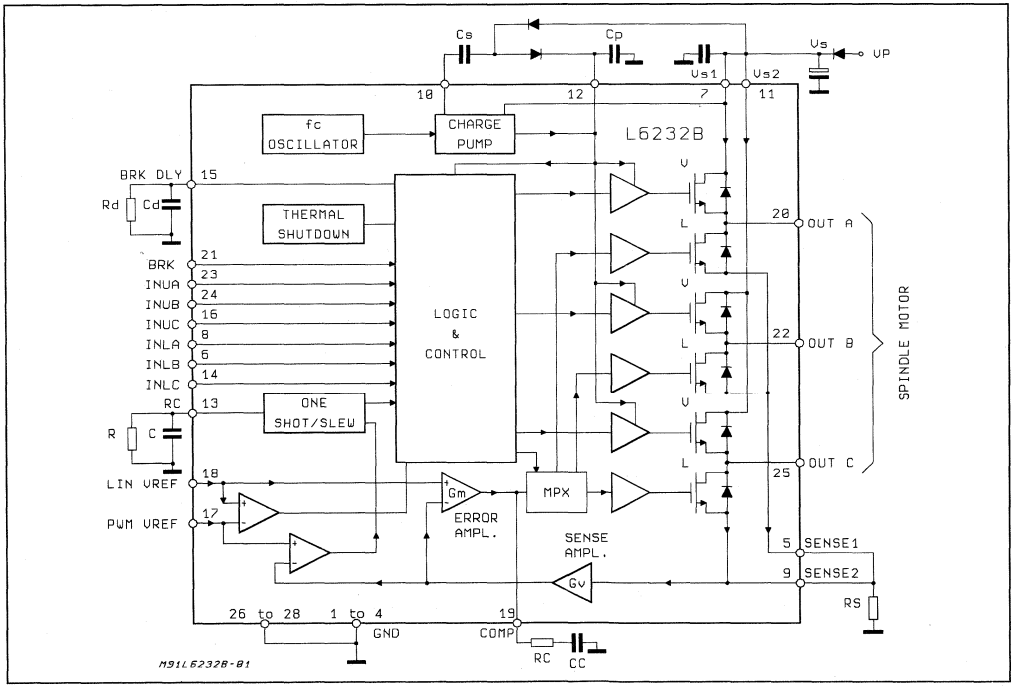


PLCC21+7
ORDERING NUMBER: L6232B

DESCRIPTION

The L6232A is a triple half bridge driver intended for use in brushless DC motor applications. This part can be used to form the power stage of a three-phase, brushless DC motor control loop, and is especially useful for disk drive applications. Power drivers are Integrated DMOS transistors and feature fast recirculating diodes as an integral part of their structure. The logic inputs are TTL-level compatible, with internal pull-up, allowing interfacing to open collector outputs. All necessary circuitry to perform PWM and linear motor speed control is included. A central charge pump is utilized to drive the upper DMOS transistors, and also to power the braking function. The L6232B is packaged in PLCC28.

BLOCK DIAGRAM

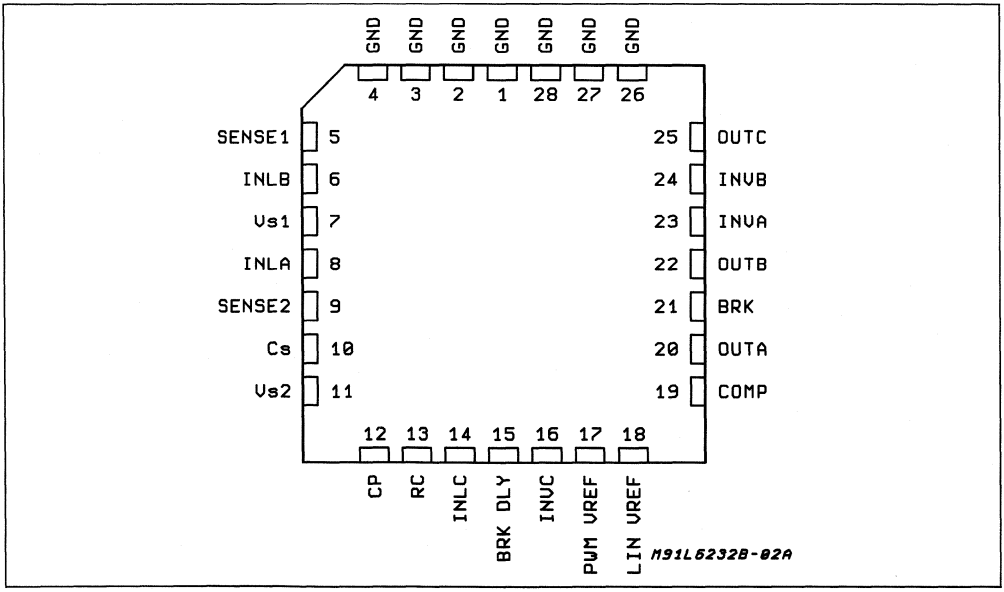


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Name	Function
1 to 4	GND	Common Ground. Also provides heat-sink to PCB.
5, 9	SENSE	Output for current sense resistors.
6	INLB	Logic Input to turn on the lower driver (Active High).
7, 11	V_S	Supply Voltage.
8	INLA	Logic input to turn on the lowey driver (Active High).
10	C_S	External Charge Pump Capacitor.
12	C_P	External Main Charge Pump capacitor.
13	RC	Cutoff Time RC Network in PWM mode. The Resistor value is also used to define the slew-rate in linear mode (LIN).
14	INLC	Logic input to turn on the lower driver (Active High).
15	BRK DLY	External RC network for the brake delay.
16	INUC	Logic Input to turn on the upper driver (Active Low).
17	PWM Vref	Input for Reference Control in PWM mode
18	LIN Vref	Input for Reference Control voltage in LIN mode
19	COMP	External compensation for error amplifier
20	OUTA	DMOS Half-bridge A Out.
21	BRK	Active LOW logic input that triggers the delayed brake.
22	OUTB	DMOS Half-bridge B Out.
23	INUA	Logic Input to turn on the upper drivers (Active Low).
24	INUB	Logic Input to turn on the upper drivers (Active Low).
25	OUTC	DMOS Half-bridge C Out.
26 to 28	GND	Common Ground. Also provides heat-sink to PCB.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DS\ sus}$	Peak Output Sustaining Voltage	15	V
V_S	Supply Voltage	15	V
$V_{O\ peak}$	Output Peak Voltage (t_{pK} = 5 µsec; 10% d.c.)	18	V
V_{Cp}	Charge Pump Input Voltage	30	V
V_i	Logic Input Voltage	-0.3 to 7	V
V_{REF}	PWM VREF--LIN VREF Input Voltage	-0.3 to 7	V
V_{is}	Sense Input Voltage	-1 to 7	V
I_p	Sink-Source Peak Output Current (*)	3.5	A
I_O	Sink-Source DC Output Current	1.8	A
P_{tot}	Total Power Dissipation (T_{amb} = 70C)	1.5	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (**)	Max.	52	°C/W

Notes
(*) Pulse width (limited only by junction temperature and by the transient thermal resistance.
(**) Mounted on board with 16cm^2 35µm thickness copper area on board heatsink.

ELECTRICAL CHARACTERISTICS (See the block diagram, V_S =12V, R = 100KΩ; C = 180pF; T_j = 25C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10.5	12	13.5	V
I_S	Quiescent Supply Current	BRK = L; INUA = INUB = INUC = L; INLA = INLB = INLC = H; Table 1		0.3	0.5	mA
		BRK = H; INUA = INUB = INUC = H; INLA = INLB = INLC = L; Table 1		4	6	mA
I_{OL}	Output Leakage Current	V_O = V_S = 13.5V			1	mA
R_{DSon}	Sink Out ON Resistance	T_j = 25C (see Fig.4)		0.42	0.47	Ω
		T_j = 125C		0.7		Ω
R_{DSon}	Source Out ON Resistance	T_j = 25C (see Fig.4)		0.42	0.47	Ω
		T_j = 125C		0.7		Ω
V_F	Body Diode Forward Drop (sink and source)	I_{DS} = 1A (see Fig. 6)		1	1.5	V
$t_{d(BRK)}$	Brake Delay Time	See Fig. 1, 3; note1		210		ms
T_{BRK}	Braking Time		10			s
$I_{B(LIN)}$	LIN Vref Input Bias Current	LIN V_{ref} = 0.4 to 5.5V		400	800	nA
$I_{B(PWM)}$	PWM Vref Input Bias Current	PWM V_{ref} = 0.4 to 5.5V		400	800	nA
LIN V_{ref}	Reference Voltage Input	Note 2; R_S = 0.5Ω I_{motor} (PWM) = 1A I_{motor} (LIN) = 200mA		2		V
PWM V_{ref}				0.4		V
G_v	Sense Amplifier Voltage Gain	PWM V_{ref} = 2.5V, LIN V_{ref} = 0.4V, R_S = 0.5Ω; Note 2	3.8	4	4.2	V/V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_m	LIN Error Amplifier Transconductance			0.8		mA/V
Zout	Error Amplifier Output Impedance			2		MΩ
V_{INH}	Logic Input Voltage BRK; INUA; INUB; INUC; INLA; INLB; INLC		2			V
V_{INL}					0.8	V
$I_{INH(leak)}$	Logic Input Current BRK; INUA; INUB; INUC; INLA; INLB; INLC	V_i = 2.7V			-1	mA
I_{INL}		V_i = 0.4V			-0.1	mA
t_{donU}	Upper/Lower Turn-on Delay	Table 1 see Fig. 3		0.7		µs
t_{donL}				0.15		µs
t_{doffU}	Upper/Lower Turn-off Delay			15		µs
t_{doffL}				0.5		µs
dV/dt	Source DMOS Slew-Rate (PWM)	see Fig. 3	10			V/µs
dV/dt	Source DMOS Slew-Rate (LIN)	see Fig. 3			1	V/µs
dV/dt	Sink DMOS Output Turn-off Slew-Rate	Note 3; R = 100KΩ		0.1		V/µs
F_C	Internal Clock Frequency			380		KHz
T_{off}	PWM Cutoff Time	R=100KΩ; C=180pF, Note 4; see Fig. 2		12		µs
T_{sd}	Shutdown Temperature			160		C
T_{sdr}	Recovery Temperature			120		C

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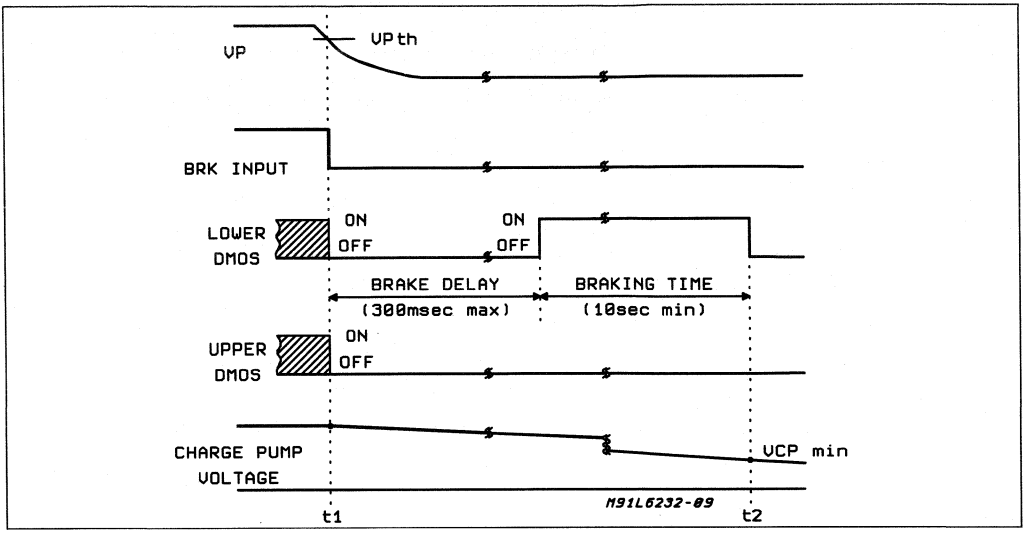

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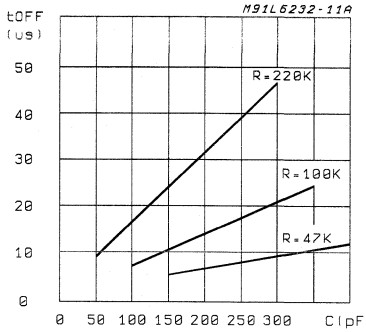
Figure 2: Typical t_{off} vs. Capacity of C



$$PWM\ Vref = 4\ Rs\ Ip$$

where Ip is the peak chopping current in the motor windings. Of course, when the required RPM is reached, it become of no need a strong torque and the LIN Vref starting from a value higher than the calculated PWM Vref, decreases to the value :

$$LIN\ Vref = 4\ Rs\ Im$$

where Im, smaller than Ip, is the needed motor current to keep constant spin. This last reference voltage is generally a PLL output driven by speed transducers coupled to the spindle (like Hall effect sensors or BEMF processors). To drive the upper DMOS and during the brake function a voltage higher than the supply Vs is needed. The charge pump integrated in the L6232B keeps C3 at the correct voltage. To guarantee efficient braking of the motor , C3 must be chosen of adeguate quality (very high equivalent parallel resistance). C4 can be a ceramic disk capacitor . The typical application od the L6232B is in HDD systems on which there is the need to park the Read-Write Heads before the motor braking. This behavior is possible with the circuit of Fig.3. At Power Supply switch-off (see Fig. 1), VP falls down and drives down the BRK input (Active Low). D1 insulates the L6232B from the power suppy output while the power output stage is switched in a high impedance state. The spindle motor acting as a three-phase alternator supplies the Heads voice coil motor driven through integrated diodes that rectifie the EMF. After a delay longer than the parking time, the lower output DMOS are switched-on and the spindle motor is braked. The brake delay time is tipically 150

msec and it is defined by :

$$td(BRK) = 1.4\ R1\ C6$$

The sensing resistor value is generally lower than 1ohm, but a wire wounded type must be avoided. In Fig.3 the 0.33 ohm sensing resistor is shown as three parallel 1ohm metal film resistors. Care must be taken in the PC Board design particularly about ground loops and ground copper area. The typical Thermal Resistance junction to ambient versus PC Board copper area (Fig.7) is shown in Fig 8. For Transient Thermal Resistance see Fig. 9.

Figure 3: Typical Application Circuit

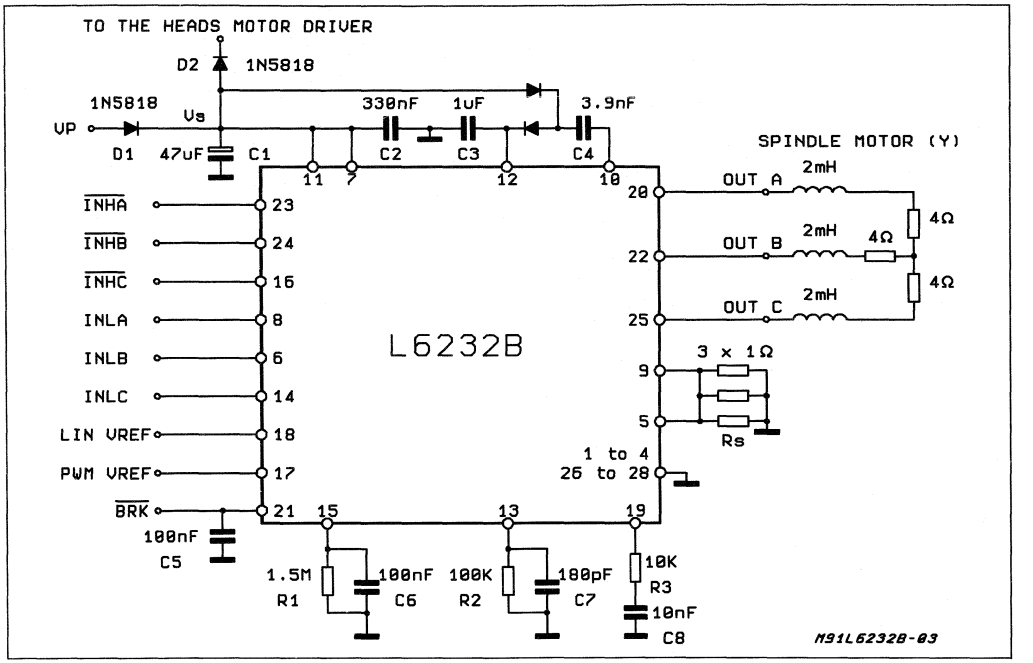


Figure 4: Typical Normalized $R_{DS\ (on)}$ vs. Junction Temperature

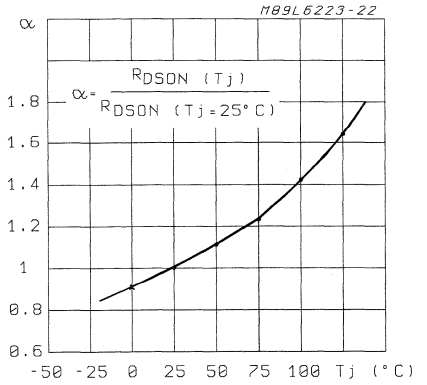


Figure 5: Output Voltage Slew Rate Control vs. $1/R_2$ Value

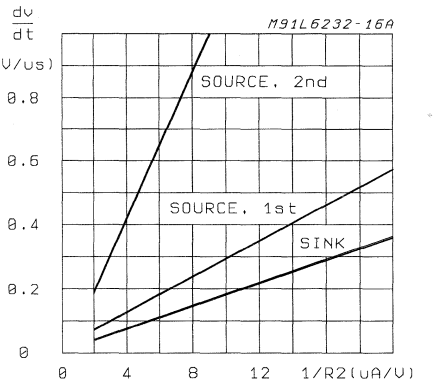


Figure 6: Typical Body Diode Forward Drop vs. Drain to Source Current.

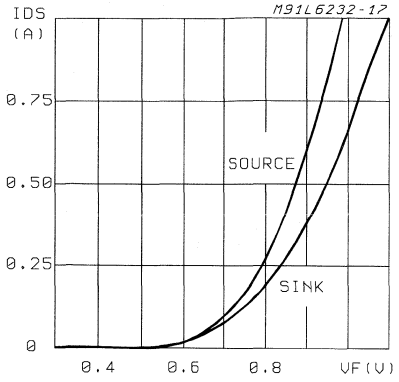


Figure 7: On Board Dissipation Copper Area Size

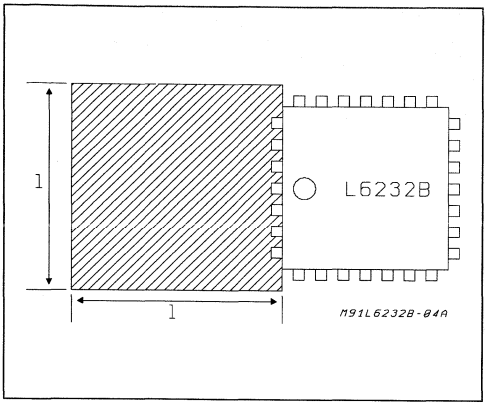


Figure 8: Typical $R_{th\ j\text{-}amb}$ vs. On-Board Heatsink Side l.

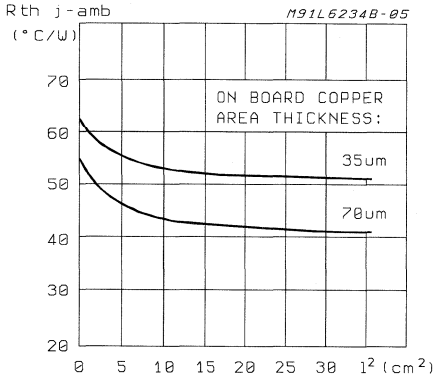
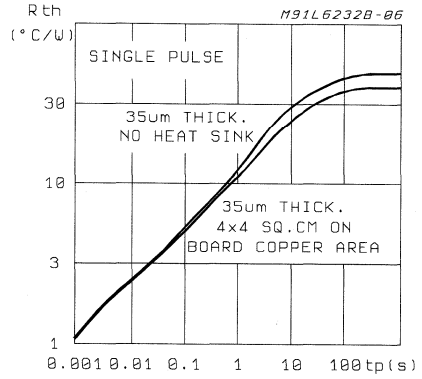


Figure 9: Typical Transient R_{th} in Single Pulse Condition.



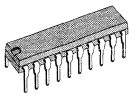
SGS-THOMSON MICROELECTRONICS

L6234

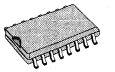
THREE PHASE MOTOR DRIVER

ADVANCE DATA

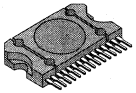
- SUPPLY VOLTAGE FROM 8 TO 52V
- 5A PEAK CURRENT
- DC MAX CURRENT T_{case} = 70°C
  - 1.5A (SO16+2=2)
  - 2A (DIP 16+2+2)
  - 4A (FLEXIWATT 21)
- $R_{DS\ ON}$ 0.3Ω TYP VALUE AT 25°C
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVER
- OPERATING FREQUENCY TO 50KHz
- THERMAL SHUTDOWN
- INTRINSIC FAST FREE WHEELING DIODES
- INPUT AND ENABLE FUNCTION FOR EVERY HALF BRIDGE
- INTERNAL LOGIC SUPPLY



Powerdip 16+2+2
(L6234)



SO 16+2+2
(L6234D)



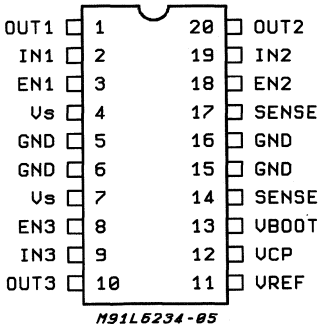
Flexiwatt 21
(L6234F)

ORDERING NUMERS: L6234
L6234D
L6234F

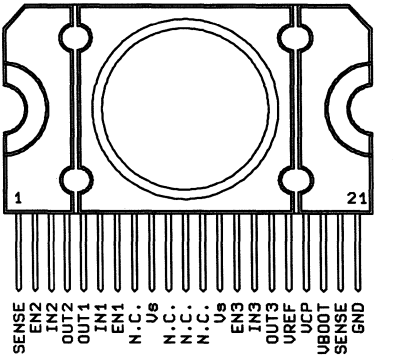
DESCRIPTION

The L6234 is a triple half bridge to drive a brushless motor.
It is realized in Multipower BCD technology wich combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip.
By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performances.
The output DMOS transistors can sustain a very high current due to the fact that the DMOS structure is not affected by the second breakdown effect, the maximum RMS maximum current is practically limited by the dissipation capabilies of the package. All the logic inputs are TTL, CMOS and µP compatible. Each channel is controlled by two separate logic input.
L6234 is available in 20 pin Powerdip (16+2+2); L6234), in 20 pin SO package (16+2+2; L6234D) (both packages have the 4 central pins to conduct heat to heatsink) and in Flexiwatt (L6234F).

PINS CONNECTIONS (Top view)



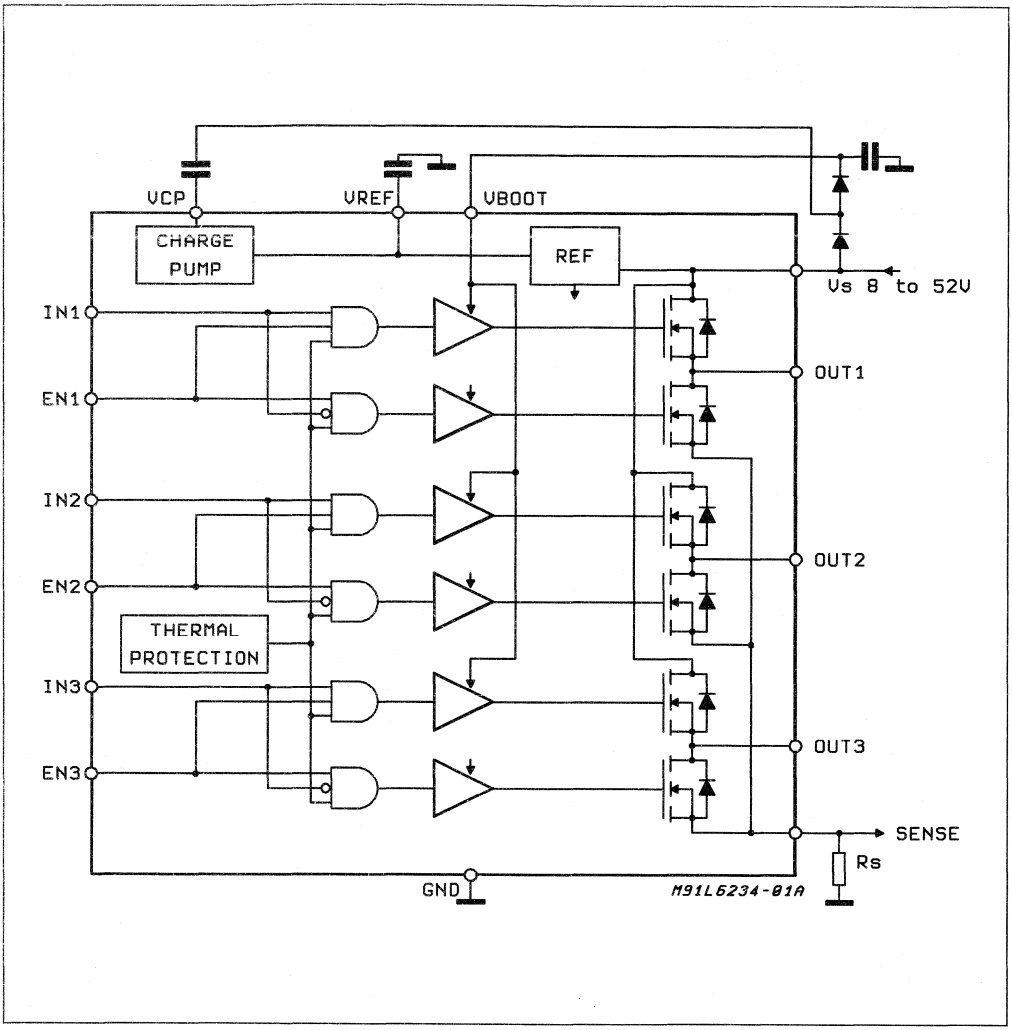
DIP and SO



Flexiwatt

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_P	Power Supply Voltage	52	V
V_{IN}, V_{EN}	Input Enable Voltage	– 0.3 to 7	V
I_{peak}	Pulsed Output Current (note) **L6234D** **L6234** **L6234F**	2.5 4 5	A A A
V_{SENSE}	Sensing Voltage	-1 to 4	V
V_b	Bootstrap Peak Voltage	60	V
V_{OD}	Differential Output Voltage (between any of the 3 OUT pins)	60	V
P_{tot}	Total Power Dissipation **L6234D** T_{pins} = 90°C **L6234** T_{pins} = 90°C **L6234F** T_{case} = 90°C	3.3 4.3 20	W W W
P_{tot}	Total Power Dissipation **L6234D** T_{amb} = 70°C **L6234** T_{amb} = 70°C	0.9 (*) 1.5 (*)	W W
T_{stg}, T_j	Storage and Junction Temperature Range	-40 to 150	°C

Note 1: Pulse width limited only by junction temperature and the transient thermal impedance
(*) Mounted on board with minimized copper area

THERMAL DATA

Symbol	Description	L6234	L6234D	L6234F	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	14	18		°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case			3	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	(*)55	(*)90	(**)45	°C/W

(*) Mounted on board with minimized copper area
(**) Mounted in air with no heatsink

PIN FUNCTIONS

DIP/SO	Flexiwatt (*)	Name	Function
1 20 10	5 4 16	OUT 1 OUT 2 OUT 3	Output of the channels 1/2/3.
2 19 9	6 3 15	IN 1 IN 2 IN 3	Logic input of channels 1/2/3. A logic HIGH level (when the corresponding EN pin is HIGH) switches ON the upper DMOS Power Transistor, while a logic LOW switches ON the corresponding low side DMOS Power.
3 18 8	7 2 14	EN 1 EN 2 EN 3	Enable of the channels 1/2/3. A logic LOW level on this pin switches off both power DMOS of the related channel.
4,7	9,13	V_S	Power Supply Voltage.
14,17	1,20	SENSE	A resistance Rsense connected to this pin provides feedback for motor current control (the two pins must be connected together).
11	17	V_{ref}	Internal Voltage Reference. A capacitor connected from this pin to GND increases the stability of the Power DMOS drive circuit.
12	18	V_{cp}	Bootstrap Oscillator. Oscillator output for the external charge pump.
13	19	V_{BOOT}	Overvoltage input to drive the upper DMOS
5,6 15,16	21	GND	Common Ground Terminal. In Powerdip and SO packages these pins are used to dissipate the heat forward the PCB.

(*) Pins 8, 10, 11, 12 are Not Connected.

ELECTRICAL CHARACTERISTICS (V_S = 42V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		8		48	V
V_{ref}	Reference Voltage			10		V
I_S	Quiescent Supply Current			2		mA
f_C	Commutation Frequency				50	KHz
T_S	Thermal Shutdown		150			°C
T_D	Dead Time Protection			300		ns

OUTPUT DMOS TRANSISTOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DSS}	Leakage Current				1	mA
$R_{DS\ (ON)}$	ON Resistance			0.3		Ω
V_{sense}	Sensing Voltage		-1		4	V

SOURCE DRAIN DIODE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SD}	Forward ON Voltage	I_{SD} = 1.2A; EN = LOW		0.9		V
T_{RR}	Reverse Recovery Time	I_F = 1.2A		300		ns
T_{pr}	Forward Recovery Time			200		ns

LOGIC LEVELS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}, V_{ENL}	Input LOW Voltage		-0.3		0.8	V
V_{INH}, V_{ENH}	Input HIGH Voltage		2		7	V
I_{INL}, I_{ENL}	Input LOW Current	V_{IN},V_{EN} = L			-10	µA
I_{INH}, I_{ENH}	Input HIGH Current	VIN,V_{EN} = H		30		µA

CIRCUIT DESCRIPTION

L6234 is a triple half bridge designed to drive brushless DC motors.

Each half bridge has 2 power DMOS transistors with R_{dsON} = 0.3Ω. The 3 half bridges can be controlled independently by means of the 3 inputs IN1, IN2, IN3 and the 3 inputs EN1, EN2, and EN3. An external connection to the 3 common low side DMOS sources is provided to connect a sensing resistor for constant current chopping application.

The driving stage and the logic stage are designed to work from 8V to 52V.

Figure 1: $R_{th\ j\text{-}amb}$ of Powerdip 16+2+2 vs Side 1 for Heat Sink on the PCB Lower Side

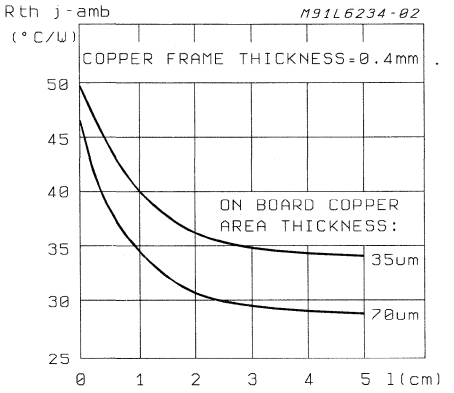


Figure 2: Dip 16+2+2 Transient Thermal Resistance for Single Pulses

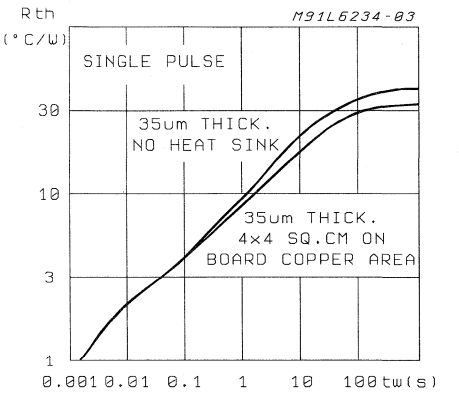
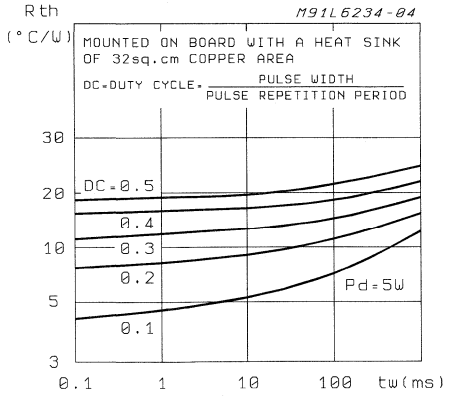


Figure 3: Dip 16+2+2 Peak Transient R_{th} vs Pulses Width and Duty Cicle



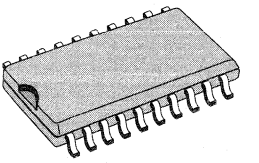
SGS-THOMSON MICROELECTRONICS

L6242

VOICE COIL MOTOR DRIVER

ADVANCE DATA

- OUTPUT CURRENT UP TO 1A
- OPERATES AT LOW VOLTAGES WITH LOW COIL RESISTANCE OF THE MOTOR
- LARGE COMMON MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- THERMAL SHUT-DOWN
- ENABLE FUNCTION
- INTERNAL CLAMP DIODES



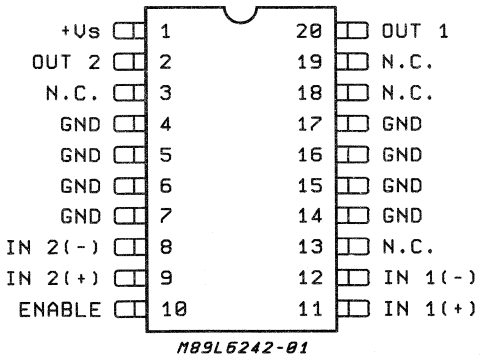
SO20

ORDERING NUMBER: L6242

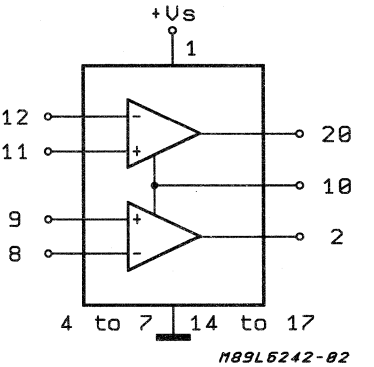
DESCRIPTION

The L6242 is a monolithic integrated circuit in SO-20 package intended for use as a dual power operational amplifier. It is particularly indicated for driving inductive loads as linear motor, and finds application in Hard Disc, Compact-Disc, etc.
The two power operational amplifiers are controlled by a common enable input.
The high gain and output power capability provide superior performance whatever a power booster is required.

PIN CONNECTION AND BLOCK DIAGRAM



M89L6242-01



M89L6242-02

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	28	V
V_i	Input Voltage	VS	V
V_i	Differential Input Voltage	$\pm V_S$	V
I_O	DC Output Current	1	A
I_P	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Maximum Power Dissipation at T_{amb} = 85°C T_{CASE} = 75°C	1 5	W W
T_{stg}, T_J	Storage and Junction Temperature Range	-40 to 150	°C

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		28	V
I_S	Quiescent Drain Current	$V_O = V_S/2$		10	15	mA
I_b	Input Bias Current			0.2	1	µA
V_{OS}	Input Offset Voltage				15	mV
I_{OS}	Input Offset Current			10	50	nA
S_r	Slew Rate			1.5		V/µs
R_i	Input Resistance		500			KΩ
G_V	Open Loop Voltage Gain	f = 100Hz	70	80		dB
CMR	Common Mode Rejection	f = 100Hz	66	84		dB
SVR	Supply Voltage Rejection	f = 100Hz R_g = 10KΩ V_r = 0.5V		54		dB
V_{drop}	High Drop Voltage	I = 100mA I = 500mA		0.7 1	 1.5	V V
V_{drop}	Low Drop Voltage	I = 100mA I = 500mA		0.3 0.6	 1	V V
T_{sd}	Thermal Shutdown Junction Temperature			145		°C
R_p	Internal Pull-up Resistor of the Enable Input				50	KΩ
V_e	Enable Low Voltage	T_J = 130°C	-0.3		1.2	V
I_{eq}	Quiescent Drain Current	En = L		2	5	mA
T_d	Enable Delay				50	µs
I_{ol}	Output Leakage Current			10		µA

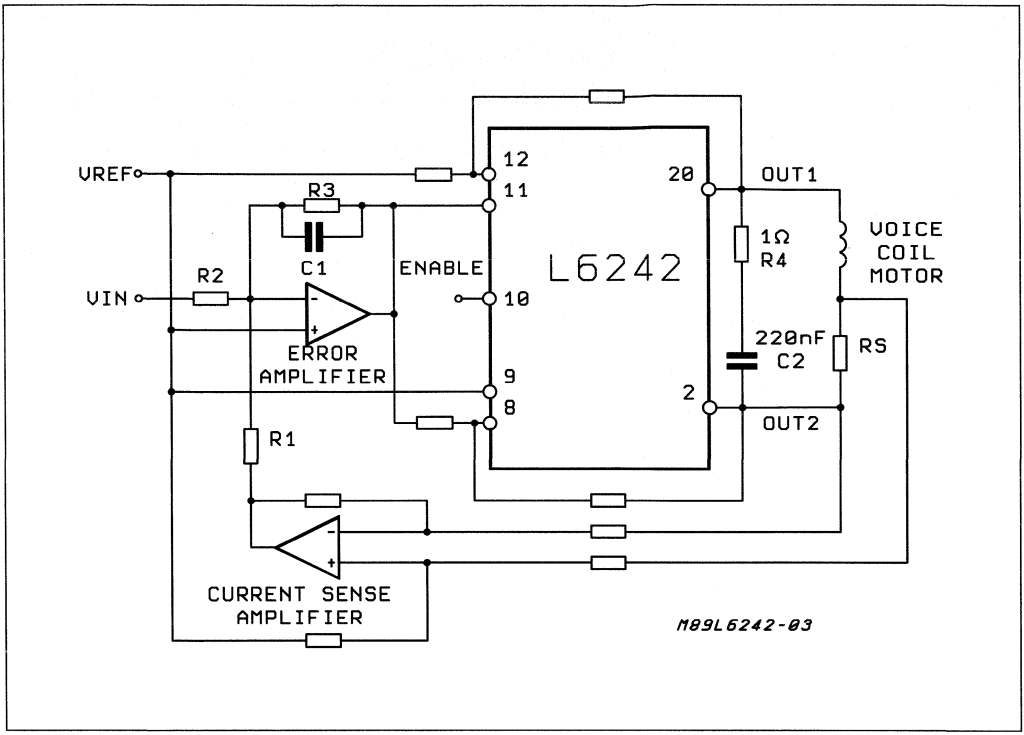
APPLICATION INFORMATIONS

Figure 1 shows the L6242 configurated as a transconductance amplifier, in order to drive linear motors as Voice Coil (VCM). The L6242 provides the power section of the Transconductance Amplifier. The two OP AMP are configurated one as inverting and the other as noninverting amplifier, with the same gain. Working in push-pull, they can be configurated as a bridge. The motor current can be controlled by means of the sense resistor (typical 1Ω) in series with the motor. The current sense amplifier provides the feedback signal, which is summed to the driving signal at the node which is the inverting input of the Error Amplifier. R1 closes the control loop. R2 converts the input voltage signal, into a current signal.

The snubber network provides the system stability, always required by the application. The network is directly connected to the output pins of the IC, OUT1 and OUT2, and in parallel with the load. R4 and C2 could be of different values, depending on the p.c.b. configuration and on the motor characteristics.

The DC transfer function may be expressed as:
gm = Iout/Vin = k • (R1/R2)
where k = 1/(Rsense • Ad)
and Ad = gain of the current sense amplifier.

Figure 1: Voice Coil Motor Control Circuit



OPTIMIZING LAYOUT

Optimizing a PC board layout involves to observe the following rules which in general can avoid application problems associated with ground loops and anomalous recirculation currents. The electrolytic capacitor for the power supply must be kept as close to the IC as possible. It is important that power grounds are close to each other on a wide enough. Copper side also, it is important to separate on the board the logic ground and the power ground in such a way that the ground traces for the logic signals and references do not cross the ground traces for the power signals. Logic ground and power ground must meet at one point on the board (startpoint grounding) far enough away from where the power ground traces terminate to ground (sense resistors and recirculation diodes). This is to avoid anomalous interface with the logic signals. It is generally a good idea to connect a non inductive capacitor (typically 100nF) between the pins VS and GND. In other cases it may be necessary to also place a by-pass capacitor between the pins Vref and GND.

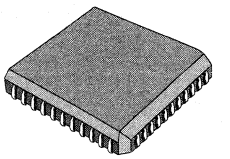
SGS-THOMSON MICROELECTRONICS

L6243
L6243D

VOICE COIL MOTOR DRIVER

ADVANCE DATA

- 12V/5V OPERATION
- PARKING FUNCTION FOR HARD DISK HEAD ACTUATOR
- OUTPUT CURRENT UP TO 2A DC, 2.5A PEAK
- LOW SATURATION VOLTAGE
- LOGIC AND POWER SUPPLY MONITOR
- LINEAR CONTROL
- THERMAL PROTECTION
- ENABLE FUNCTION
- CURRENT SENSE RESISTOR CONNECTIONS



PLCC44 **SO(24+2+2)**

ORDERING NUMBERS:

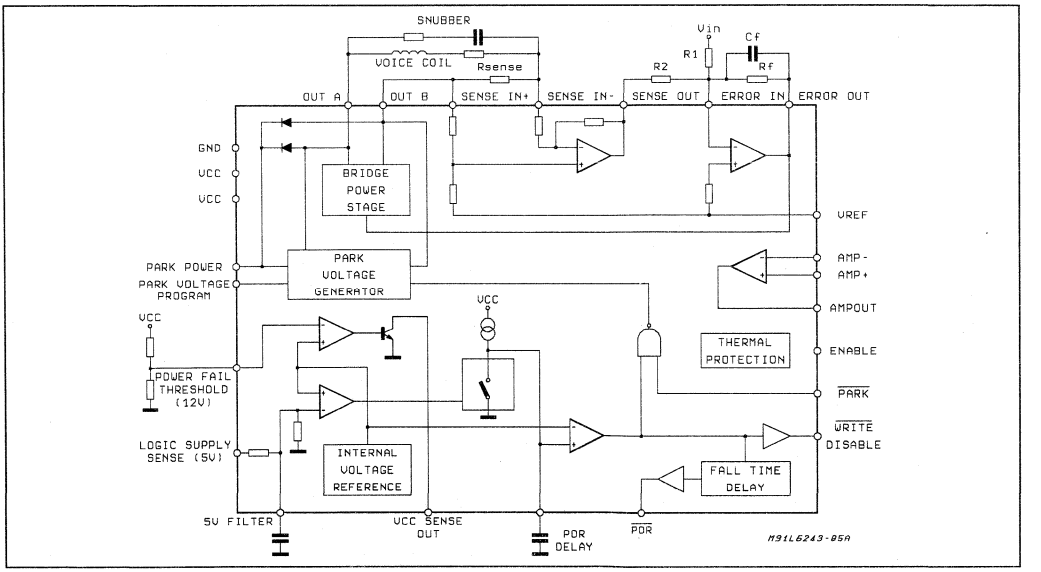
L6243 L6243D

DESCRIPTION

The L6243/D is a Bipolar IC developed for use in Hard Disk Head Actuator positioning applications. The Power Op-Amp Output Bridge, Differential Amplifier, and Error Amplifier, are controlled by TTL/CMOS, input compatible, Digital Logic, and an Analog Current Control Voltage. A simple RC compensation network, tied to the output of the Error Amp, will configure the system to work as a Transconductance Amplifier to drive a Voice Coil Motor in Linear Mode.

Additional features include Power On Reset Delay, Enable and Park, as well as a general purpose Operational Amplifier. A logic low at the Park input activates the parking function. Holding the Enable input low will disable the device by forcing the outputs into a tristate mode. Power Fail Monitors for the logic and power supplies initiate an automatic parking sequence during a power failure. A resistor programmed parking voltage enables a constant velocity head retract.

BLOCK DIAGRAM



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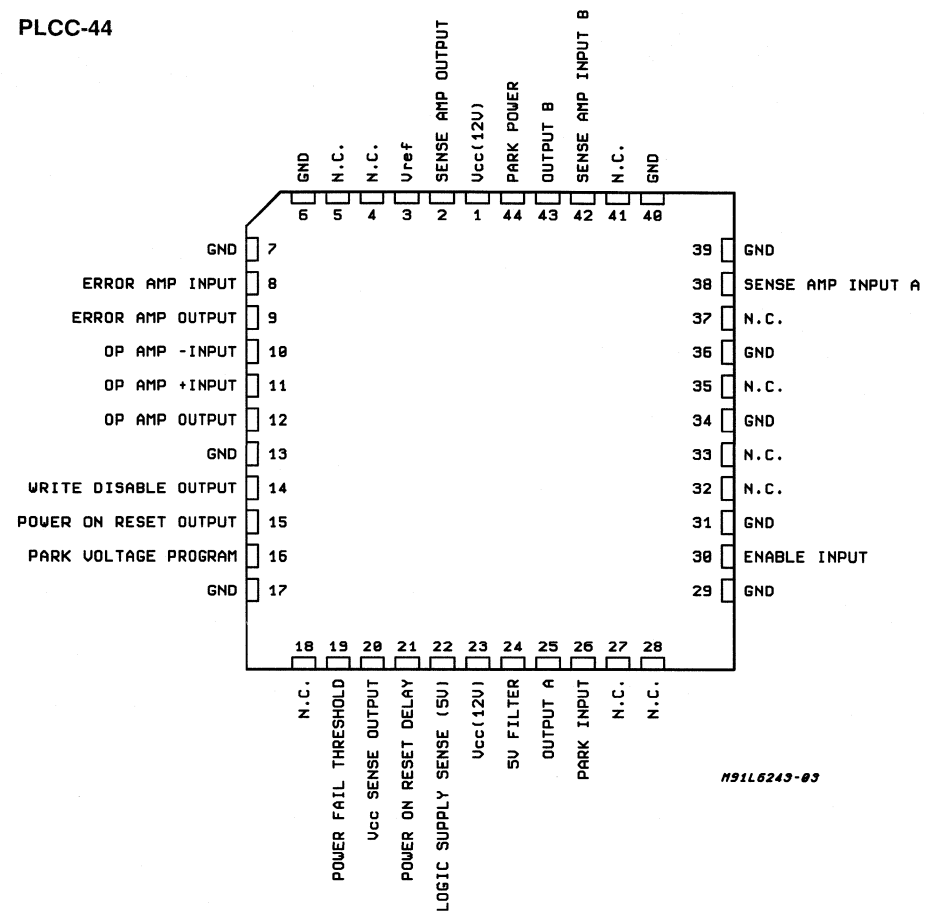
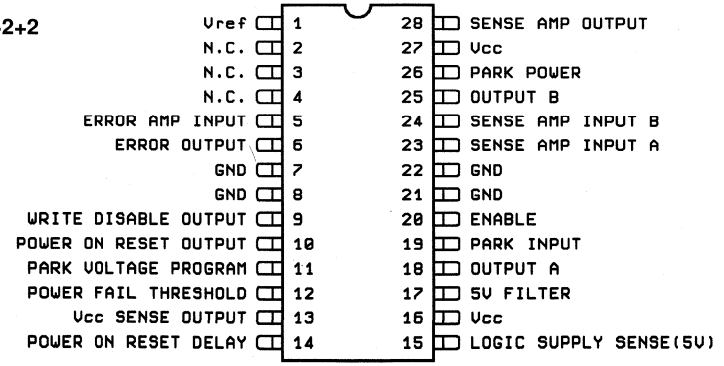
PIN CONNECTION (Top view)

PLCC-44



SO 24+2+2



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	18	V
V_{IN}	Input Voltage	0.3V to V_S	
V_{ID}	Differential Input Voltage	$\pm V_S$	
I_O	DC Output Current	2	A
I_p	Peak Output Current (non repetitive)	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 70°C) for L6243 for L6243D	2 1.2	W W
T_{stg}	Storage and Junction Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Description	L6243	L6243D	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction to pin	12	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin floating in air	62		°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin 16 cm^2 copper area on board heat sink	36	50	°C/W

PIN FUNCTIONS

Name	Function
V_{CC}	Power supply.
GND	Common Ground.
V_{ref}	Voltage Reference.
ENABLE	Input. Logic low will disable IC.
PARK POWER	Input Power supply for the parking circuit.
CURRENT SENSE OUT	Current sense operational amplifier output.
ERROR AMP IN	Error amplifier inverting input.
ERROR AMP OUT	Error amplifier output.
SENSE IN ±	Input for external sense resistors.
OUT A, B	Outputs of the two Power Operational Amplifiers Connections for Voice coil Motor.
PARK	External input for parking. Low will activate the park procedure.
PARK VOLTAGE PROGRAM	Input to set the park voltage.
POWER FAIL THRESHOLD	Supply monitor threshold setting.
LOGIC SUPPLY SENSE	Logic Supply Sense.
5V FILTER	Capacitor connection to filter the logic supply ripple.
V_{CC} SENSE OUT	Power supply failure monitor output.
POR	Power on reset output. Low will signal to the controller the failure of the logic supply.
POR DELAY	Capacitor connection to set the power on reset delay.
WRITE DISABLE	Output for write disable. Low will disable the writing mode.
AMP–	Inverting input of the additional op amp.
AMP+	Non-inverting input of the additional op amp.
AMPOUT	Output of the additional op amp.

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		4.5		13.2	V
I_d	Quiescent Drain Current			20		mA
T_j	Thermal Shutdown Junction Temperature			160		°C
ERROR AMPLIFIER						
I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
Gv	Large Signal Open Loop Voltage Gain		70			dB
GBW	Gain Bandwidth			3		MHz
G_{min}	Minimum Voltage Gain		5			
I_{O+}	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew-rate			2		V/µs
SENSE AMPLIFIER						
R_{IN}, V_{ref}	V_{ref} Input Impedance		9			KΩ
A_d	Differential Gain			8		V/V
SR	Slew-rate			1		V/µs
GBW	Gain Bandwidth Product			3		MHz
R_{in}	Sense Input Impedance		1.5			KΩ
CMRR	Common Mode Rejection Ratio		60			dB
POWER OP. AMP.						
G_V	Voltage Gain			26		dB
V_d	Total Output Voltage Drop	I_O = 250mA I_O = 500mA I_O = 1A I_O = 2A		450 750 1.15 2.30	 1.5 2.5	mV mV V V
V_{off}	Offset Voltage on Sense Resistor			5		mV
BW	Bandwidth on Resistive Load			100		KHz
GENERAL PURPOSE OP-AMP						
I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
G_V	Large Signal Open Loop Voltage Gain		70			dB
GBW	Gain Bandwidth Product			1		MHz
I_{O+}	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew Rate			1		V/µs

ELECTRICAL CHARACTERISTICS (continued)
MONITORS AND CONTROL CIRCUIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{t1}	Threshold Voltage at Logic Supply Sense		4.45	4.60	4.75	V
V_{t2}	Threshold Voltage at Power Fail Threshold Input		1.375	1.4	1.425	V
HV_{t1}	Hysteresis on V_{t1}			50		mV
HV_{t2}	Hysteresis on Vt2			15		mV
V_{ll}	Low Level Voltage	Write Disable = 2mA		250	500	mV
		Power on Reset = 2mA		250	500	mV
I_e	Enable Input Current	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
I_p	Input Current at Park	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
R_f	Equivalent Input Resistance at 5V Filter Input			6.9		KΩ
V_{enl}	Enable Low Input Voltage				0.8	V
V_{enh}	Enable High Input Voltage		2			V
V_{ph}	Parking Input High Voltage		2			V
V_{pl}	Parking Input Low Voltage				0.8	V
V_{pfl}	Power Fail Low Output Voltage	I_l = 2mA			0.5	V
V_{pfh}	Power Fail High Output Voltage	I_l = –440µA	2.4			V
I_{prog}	Parking Voltage Program Current			100		µA
I_{ch}	Power On Reset Delay Capacitor Charging			10		µA
T_d	Delay Between Write Disable and Power on Reset Falling Edges			4	10	µs

FUNCTIONAL DESCRIPTION

The VCM Driver is controlled via three control signals, ENABLE, POWER ON RESET, and WRITE DISABLE. An analog input voltage, ERROR AMP IN, controls the polarity and amplitude of the VCM driving current.

Refer to figure two. This diagram is a representation of the function of the VCM System. Note that the signals with the bars represent the "not true", or "non asserted" condition. From initial power up, the system is held in the Park Mode. Upon completion of the POWER UP RESET DELAY the machine moves to Tristate Mode or Run Mode, depending upon the condition of the ENABLE input. If ENABLE is asserted, the machine moves directly to Run Mode. If ENABLE is not asserted, the machine moves to Tristate Mode.

POWER ON RESET is an asynchronous output. Additionally it affects the internal logic as a hard wired reset and therefore if a supply failure occurs during Tristate or Run state, the machine moves directly back to the Park Mode. A WRITE DISABLE occurs a few to ten microseconds prior to the POWER ON RESET in order for the system to halt any read/write activity before a head retract begins.

While in Tristate Mode, the assertion of ENABLE will move the machine to the Run Mode. Run Mode will typically be the steady running state. The deassertion of the ENABLE signal causes the machine to move into Tristate. If it is desired to perform an active Parking function, the PARK input must be driven low by the external hardware, or the the VCM can be driven to the Park position via the ERROR AMP IN control voltage

FUNCTIONAL DESCRIPTION (continued)

Function	Description
V_{CC} input	This is the Power Supply input.
POWER FAIL THRESH	Input for the V_{CC} supply monitor. The Threshold can be externally set via a voltage divider.
V_{CC} SENSE OUT Output	TTL compatible signal indicating the V_{CC} supply has dropped below the POWER FAIL THRESHOLD.
LOGIC SUPPLY SENSE input	This input is used to monitor the Five Volt Logic Supply for the external control and other support IC's. The LOGIC SUPPLY SENSE operates independently of the 12V Power Supply. When a 5V supply failure is detected a POWER ON RESET is generated.
5V FILTER input	This pin allows for the application of filter circuitry in order to avoid false triggering.
PARK POWER input	This input is used during the Power Down/Power Fail Parking operation. When the supply goes down, a typical Spindle Driver Circuit automatically tristates its output stages. During this time the spindle motor spins freely and the stored energy is used to drive the VCM to the park position. The generated BEMF is rectified and filtered across an external PARKING CAPACITOR.
PROGRAMMABLE PARK VOLTAGE input	Used to set the voltage applied to the VCM during an Automatic Parking Operation.
PARK input	Logic signal asserted low, activates parking.
POWER ON RESET output	Indicates an error condition to the external control and support circuitry. A Logic Supply Fail condition automatically initiates a POWER ON RESET.
POWER ON RESET DELAY input	The intent of this input is to provide a time delay at power up. During this time, the POWER ON RESET line will be asserted (low). A POWER ON RESET, will hold the system in the PARK mode. Once the delay has timed out, the POWER ON RESET will be removed to allow the external system to assume control. When applied in a Disk Drive Application, the POWER ON RESET DELAY will be required to have a minimum duration which will ensure that the Read/Write Heads can be fully parked.
WRITE DISABLE output	Becomes asserted a few microseconds prior to the assertion of POWER ON RESET.
ENABLE input	This signal originates at the external controller and, when asserted, allows the VCM Drivers to operate. When deasserted the VCM Driver is forced into Tristate mode. During a POWER ON RESET condition however, the parking operation is automatic and takes priority over the ENABLE function. Only at the end of the POWER ON RESET DELAY will the ENABLE input become active. If active parking is desired, it will be accomplished under control of the V_{IN} signal, otherwise it is an automatic function at power down.
V_{REF} input	The reference voltage input is basically that voltage, at which the output current is zero.
ERROR AMP IN input	Inverting input of error amplifier. The non inverting one is internally tied to V_{ref}.
ERROR AMP OUT output	Error amplifier output pin.
OUTPUT A power output	Voice Coil power output.
OUTPUT B power output	Voice Coil power output.
SENSE AMP IN A/B signal input	Sense amplifier input pins. The sense resistor is connected across these pins.
SENSE AMP OUT signal output	Output pin of sense amplifier.
AMPOUT output	Output of an internal op-amp for general application.
AMP+ input	General purpose op-amp non inverting input.
AMP- input	General purpose op-amp inverting input.

BLOCK DESCRIPTION

OUTPUT STAGE

It consists of two Power Op Amps connected in bridge configuration.

CURRENT SENSE AMPLIFIER

Differential amplifier whose inputs are connected to the sense lines and whose output is accessible externally. Closing the loop will transform the differential voltage signal from the sense lines into a current signal for the Error Amplifier.

ERROR AMPLIFIER

Error amplifier which drives the output stage. The input and the output pins are accessible externally.

POWER SUPPLY MONITOR OPERATION

The circuit monitors the logic supply voltage input (typ 5V) and activates Power on Reset and Write Disable output when such a supply drops below the safe operating limit. After the logic supply voltage reaches its nominal value a delay capacitor has to be charged [Tdelay=3x10e5 x C sec] before Power on Reset and Write Disable outputs change from low to high level. Falling edges of Write Disable and Power on Reset are delayed (typ 4µs) in order to disable the writing on the disk before the Power on Reset is activated. An additional supervisor circuit is present in the IC with a programmable threshold, which is set by an external resistive divider. The TTL compatible output can be used separately or connected to Park input in order to park the head.

The V_{CC} sense output pin can also be connected to 5V filter input in order to implement a POWER ON RESET function sensitive both to 5V and V_{CC}.

PARKING CIRCUIT OPERATIONT

The voice coil driver is switched into the parking condition when Power on Reset output or Park input are low. In such a condition a fixed voltage is superimposed on the load and the value of such a voltage is set by connecting an external resistor between Park Voltage Program input and ground: (Vpark=Rext x Iref, Iref=100µA typ). Connecting ENABLE input to GND the driver will be disabled (outputs in high impedance mode).

THERMAL SHUTDOWN

It will disable the IC when the junction temperature exceeds the threshold value above which the device could be damaged.

Figure 1: Application Circuit (The pinout refers to the L6243)

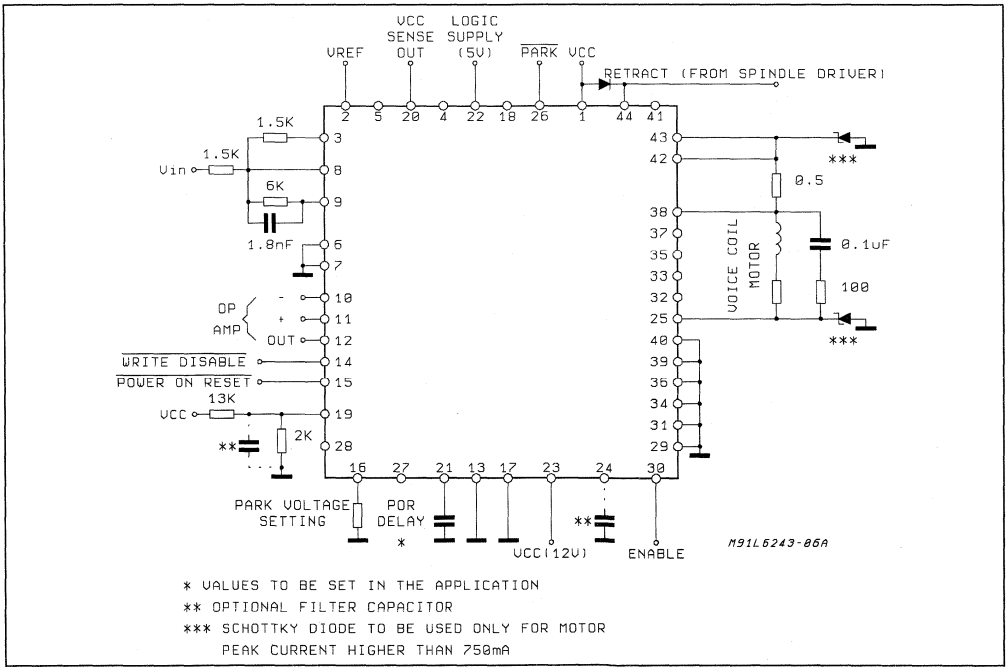
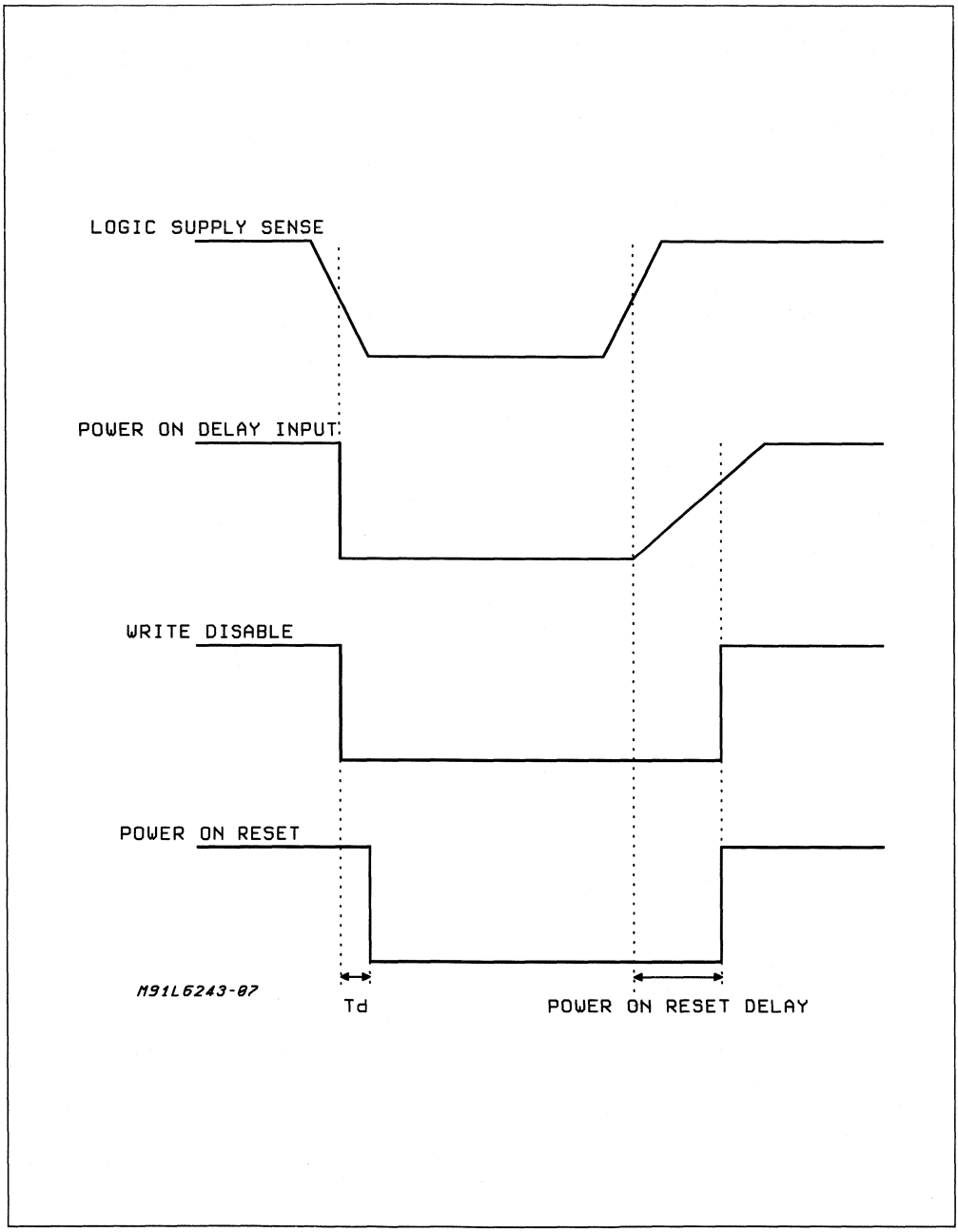


Figure 2: Waveforms



THERMAL CHARACTERISTICS

Figure 3: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power

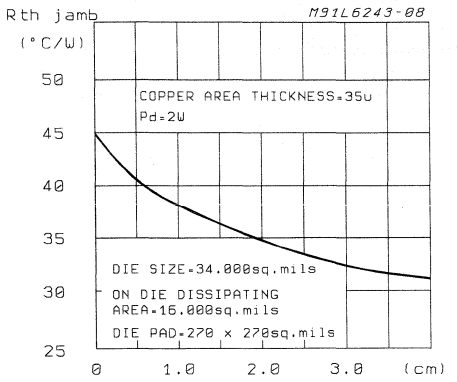
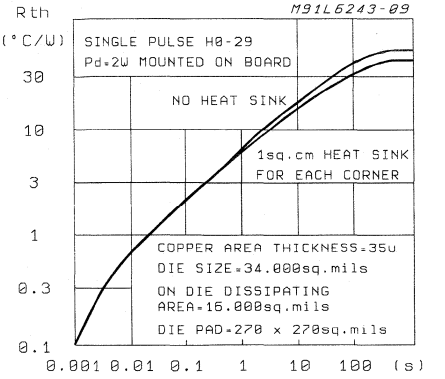


Figure 4: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power

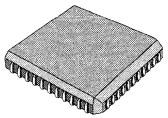


THREE CHANNELS MULTIPOWER DRIVER SYSTEM

ADVANCE DATA

- PROGRAMMABLE CONFIGURATION (CHANNELS 1 AND 2)
- OUTPUT CURRENT UP TO 1A (CHANNELS 1 AND 2)
- 1 SENSE PER CHANNEL
- OUTPUT CURRENT CHANNEL 3 UP TO 3A
- DIRECT INTERFACE TO MICROPROCESSOR
- C-MOS COMPATIBLE INPUT
- INTERNAL DC-DC CONVERTER FOR LOGIC SUPPLY (+5V)
- POWER FAIL
- WATCHDOG MANAGEMENT
- THERMAL PROTECTION
- VERY LOW DISSIPATED POWER (SUITABLE FOR USE IN BATTERY SUPPLIED APPLICATIONS)

MULTIPOWER BCD TECHNOLOGY



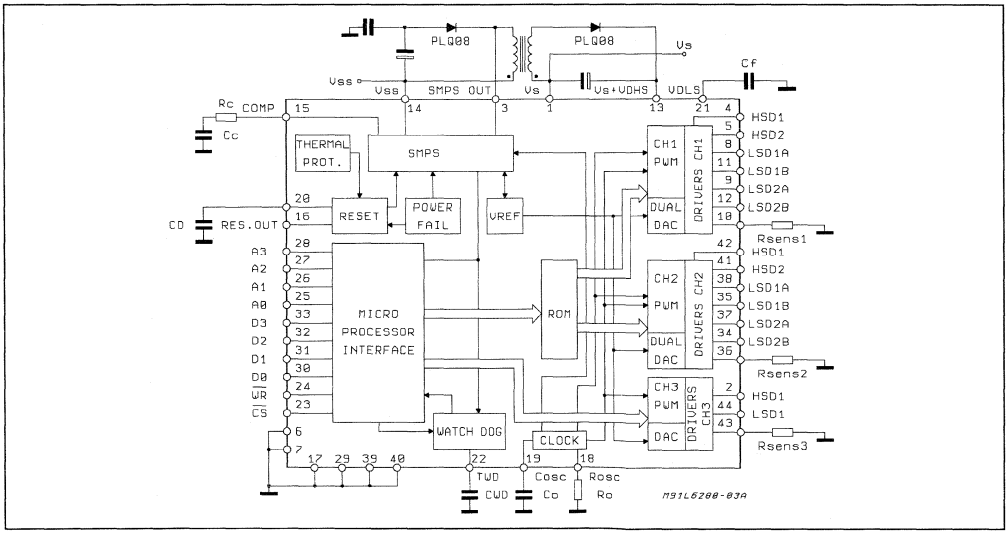
PLCC44

ORDERING NUMBER: L6280

DESCRIPTION

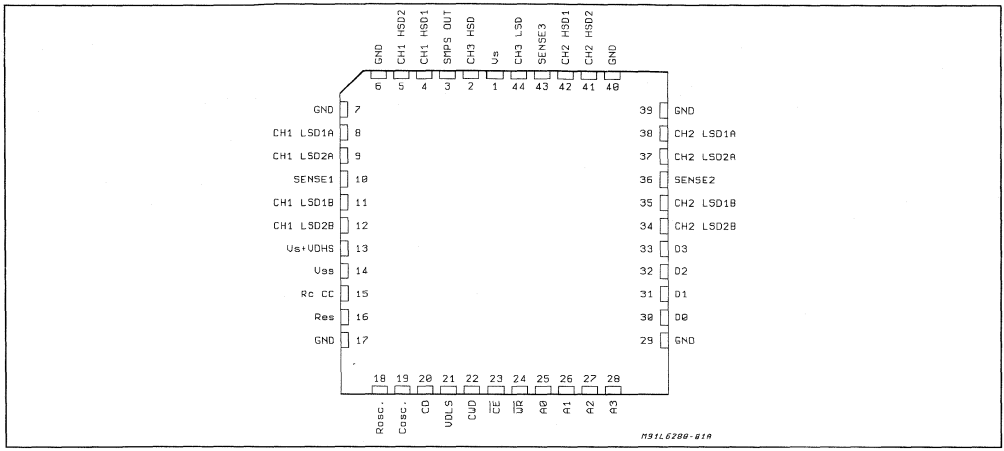
The L6280 is a multipower driver system for motor and solenoid control applicatios that connects directly to a microprocessor bus. Realized in Multipower BCD technology -- which combines isolated DMOS transistors, CMOS & bipolar circuits on the same chip -- it integrates two 1A motor drivers (channels 1 & 2) a 3A solenoid driver (channel 3) and a 5V switchmode power supply.
All of the drivers in the L6280 are controlled by a microprocessor which loads commands and reads diagnostic information, treating the device as a peripheral. Channels 1 and 2 feature a programmable output DMOS transistor configuration that can be set during the initialization phase.
Thanks to very low dissipation of its DMOS power stages the L6280 needs no heatsink and is packaged in a 44-lead PLCC package.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage (Note A)	35	V
V_{SS}	Logic Supply Voltage	7	V
V13	Pin 13 Input Voltage (Note B)	60	V
V_{DHS}	High Side Out Transistor Driving Voltage (Note B,C)	18	V
V_O	Output Voltage. CH1; CH2: Unipolar Motor Drive (Note D) CH3	60 60	V V
V_{OD}	Differential Output Voltage CH1; CH2; Full Bridge Configuration (Note E)	60	V
V_{sense}	Sensing Voltage	-1 to 2	V
V_I	Logic Input Voltage	-0.3 to V_{SS} +0.3	V
I_{LSD}	Low Side Driver Input Current CH1; CH2 DC Operation Peak (Note F) CH3 DC Operation Peak (Note G)	 0.7 2 3 4.4	 A A A A
I_{HSD}	High Side Driver Onput Current CH1; CH2 DC Operation Peak (Note F) CH3 DC Operation Peak (Note G)	 1 2 3 4.4	 A A A A
I_{SSOUT}	SMPS Output Current (Continuous) (Peak; TON < 5ms)	1 2	A A
I_{RES}	Reset Output Open Drain Input Current	16	mA
P_{tot}	Total Power Dissipation atTamb = 70°C (Note H)	1.6	W
T_{stg}; T_j	Storage an Junction Temperature Range	-40 to 150	°C

Notes: A) D0 = D1 = D2 = D3 =0; B) V13 = V_S + V_{DHS}; C) At 20V > V_{DHS} > 17V the input current at pin 13 must be < 30mA;
D) D0 = 1; D1 = D2 = D3 = 0; E) D1 = 1; D0 = X; D2 = D3 = 0; F) The pulse width must be < 5ms and the Duty Cycle must be < 10%
G) The pulse width must be <5ms and the Duty Cycle must be < 6%; H) mounted on board with minimized dissipating copper area.

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max.	50	°C/W

(*) Mounted on board with minimized dissipating copper area.

PIN DESCRIPTION

PINS	NAME	FUNCTIONS
1	V_S	Power Supply Voltage Input
2	HSD 1	High Side CH 3 Power Output
3	SMPS OUT	Output of Switchmode Power Supply
4	HSD 1	High Side CH 1 Power Output
5	HSD 2	High Side CH 1 Power Output
6, 7, 17, 29, 39, 40	GND	Common Grounded Terminal
8	LSD 1A	Low Side CH 1 Power Output
9	LSD 2A	Low Side CH 1 Power Output
10	SENSE 1	A Resistor Rsense, connected to this pin allows load current control for CH 1
11	LSD 1B	Low Side CH 1 Power Output
12	LSD 2B	Low Side CH 1 Power Output
13	$V_S + V_{DHS}$	Input Voltage for the HSD Gates Drive
14	V_{SS}	Logic Supply Voltage Input
15	Comp.	An RC series network allows the compensation of the SMPS regulation loop
16	RES OUT	The reset open drain output can be used to warn the microprocessor about V_S and V_{SS} status
18	R_{OSC}	Together with C_{OSC}, sets the cycle time of the SMPS $t = 1.1\ R_O C_O$
19	C_{OSC}	Together with C_{OSC}, sets the cycle time of the SMPS $t = 1.1\ R_O C_O$ and sets the minimum ON time in the PWM current control loop
20	C_D	The value of this capacitor sets the reset delay $t_D = 7 \times 10^4\ C_D$
21	V_{DLS}	By-pass Capacitor of the LSD Gates Voltage drive
22	t_{WD}	The value of this CWD sets the duration of the watchdog monostable $t_{WD} = 3 \times 10^4\ C_{WD}$. If no watchdog signal is generated into the TWD time the device is automatically switched off.
23	$\overline{CS}$	Enable Input (active when low)
24	$\overline{WR}$	Write Input. When $\overline{WR}$ is low the data is loaded into the µP interface
25	A0	Operation Selection (see programming sequence).
26	A1	Operation Selection (see programming sequence).
27	A2	Channel Selection (see programming sequence).
28	A3	Channel Selection (see programming sequence).
30	D0	Data (see programming sequence).
31	D1	Data (see programming sequence).
32	D2	Data (see programming sequence).
33	D3	Data (see programming sequence).
34	LSD 2B	Low Side CH 2 Power Output
35	LSD 1B	Low Side CH 2 Power Output
36	SENSE 2	A Resistor R_{sense}, connected to this pin allows load current control for CH 2
37	LSD 2A	Low Side CH 2 Power Output
38	LSD 1A	Low Side CH 2 Power Output
41	HSD 2	High Side CH 2 Power Output
42	HSD 1	High Side CH 2 Power Output
43	SENSE 3	A Resistor R_{sense}, connected to this pin allows load current control for CH 3
44	LSD 1	Low Side CH 3 Power Output

ELECTRICAL CHARACTERISTICS (V_S = 20V; T_j = 25°C; V_{SS} = 5V; V_{DHS} =15V; R_O =165KΩ; C_O =680pF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DSS}	Leakage Current	Fig. 1 V_{DS} = 60V			2	mA
V_s	Power Supply Voltage	Note 1,2	>V_{PF}		48	V
V_{INL}	Low Level Input Voltage		-0.3		1.35	V
I_{INL}	Low Level Input Current				-10	µA
V_{INH}	High Level Input Voltage		3.15		V_{SS}	V
I_{INH}	High Level Input Current				10	µA
V_{ROUT}	Low Level Reset Out	I16 = 1.5mA			0.8	V
V_{PF}	Power Supply Fail Voltage	(Fig. 2)			13	V
I_S	Quiescent Supply Current	V_S = 12V	4.5	6	7.5	mA
V_{SS}	Logic Supply Voltage		4.75	5	5.25	V
$I_{SS(IN)}$	Logic Supply Current		4.5	6	7.5	mA
$I_{SS(OUT)}$	SMPS Out Current Range	Note 3			800	mA
f_{osc}	Oscillator Frequency		64	80	96	KHz
f_1	SMPS and CH3 Frequency			f_{osc}		KHz
f_{1max}	Max SMPS Switching Frequency				120	KHz
f_2	PWM Frequency			fosc/2		KHz
f_3	High Side Driver Switching Frequency			fosc/4		KHz
TSD	Thermal Shutdown		125	150		°C
t_{WD}	Monostable Watchdog Time	CWD = 0.22µF (Note 4)		6.6		ms
t_D	Reset Delay Time	C_D = 0.22µF; Fig.2 (Note 5)		15.4		ms
R_{ON}	ON State Drain Resistance Transistor LSD CH1 - CH2 HSD CH1 - CH2 LSD CH3 HSD CH3 SMPS	Fig 3; 4ab		 2 1.1 0.5 0.5 1	 2.4 1.4 0.8 0.8 1.2	 Ω Ω Ω Ω Ω
SENSE	Internal Sense LOW-Pass Filter			300	500	ns
V_{ref}	DAC Reference Voltage	D0=D1=D2 =1 (Table 1)		1		V
DAC	DAC Resolution (3 Bit)	(See Table 1)		Vref/8		V
t_C	Discarge Time of Cosc Capacitor (Minimum TON)	(Note 6)		0.4		µs
V_{DHS}	HSD Gates Voltage Drive		13	15	17	V
I_{DHS}	Pin 13 Overage Input Current			3		mA
$I_{SS\ (OUT)\ max}$	SMPS Overload Protection Current		1.2			A
V_{DLS}	Pin 21 Overage Input Voltage			12		V
V_{SSF}	Logic V_{SS} Fail Threshold Voltage	(Fig. 2)	2.6		4.1	V
$V_{FHSD\ (1;2)}$	Internal Clamp Diode Forward Voltage CH1/CH2	@ I_{DS} = 0.4A (Fig. 5)			1.2	V
$V_{FLSD\ (1AB;2AB)}$	Internal Clamp Diode Forward Voltage CH1/CH2	@ I_{DS} = 0.4A (Fig. 5)			1.4	V
V_{FHSD}	Internal Clamp Diode Forward Voltage CH3	@ I_{DS} = 1A (Fig. 5)			1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{FLSD}	Internal Clamp Diode Forward Volt. CH3	@ I_{DS} = 1A (Fig. 5)			1.1	V
t_{CW}	Chip Seletion to End of Write	(Fig. 6)	700			ns
t_{WPW}	Write Pulse Width	(Fig. 6)	700			ns
t_{SU}	Data Set-up Time	(Fig. 6)	700			ns
t_{DH}	Data Hold-up Time	(Fig. 6)	0			ns
t_{WC}	Write Cycle Time	(Fig. 6)	2.7			ms

Notes:

1) When driving a unipolar stepper motor the Power Supply Voltage must be lower than 24V.

2) A lower Supply Voltage than the Power Fail threshold disables the Step Down Power Supply (see Fig.2)

3) The minimum output current equals the half of the peak-to-peak current ripple

4) $t_{WD} \cong C_{WD} \times 1.5 / 50 \times 10^{-6}$ (sec)

5) $t_D \cong C_D \times 3.5 / 50 \times 10^{-6}$ (sec)

6) $t_C \cong C_{OSC} \times R_{int.}$ (sec); $R_{int.} = 600\Omega \pm 30\%$

Figure 1: Drain Lekage Current Equivalent Test Circuit . The Gate-to-Source Voltage VGS is below the Switch-Off Threshold.

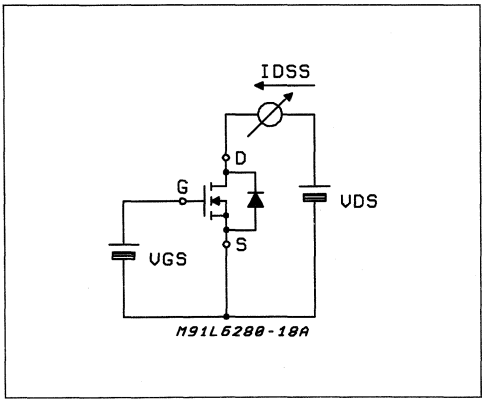


Figure 3: Typical Normalized $R_{DS(ON)}$ vs. Junction Temperature

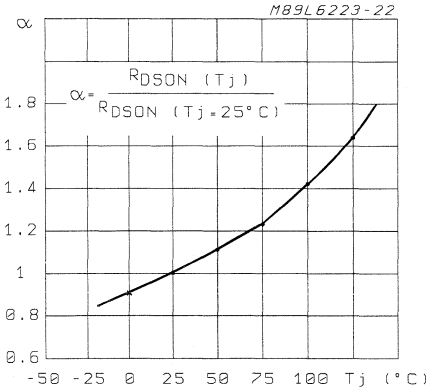


Figure 2: Reset Output Behaviour versus Power Supply Voltage V_S and/or Logic Supply Voltage V_{SS}.

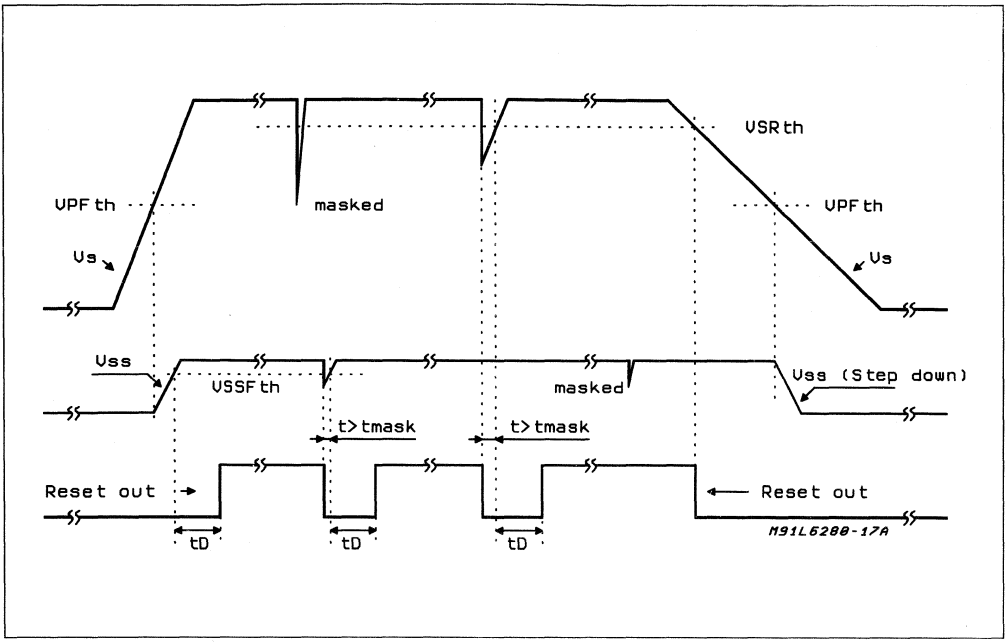


Figure 4a: Sink Output DMOS R_{ON} Equivalent Test Circuit

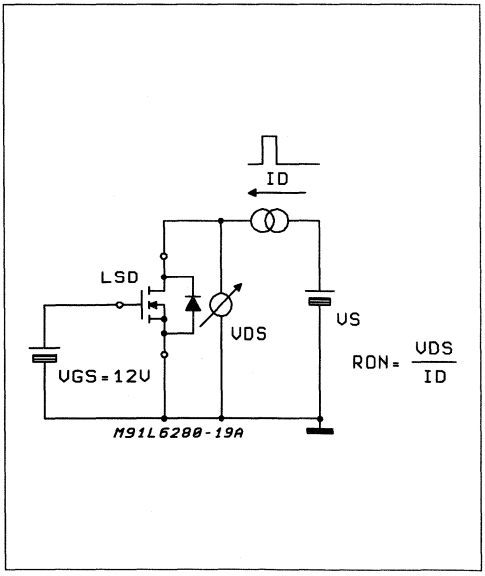


Figure 4b: Source Output DMOS R_{ON} Equivalent Test Circuit

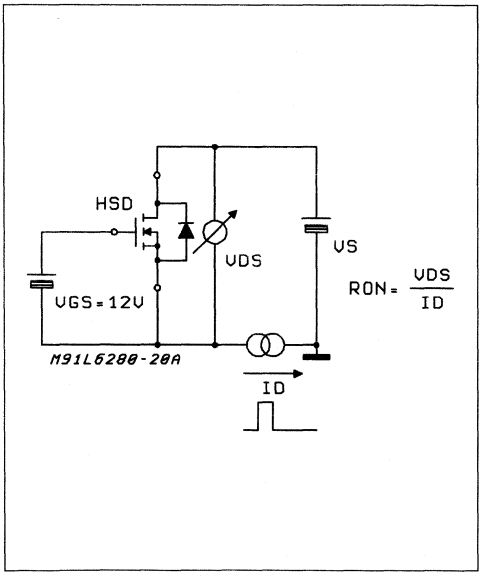


Figure 5: Possible Hardware Configurations of Power Stage (CH1 and CH2)

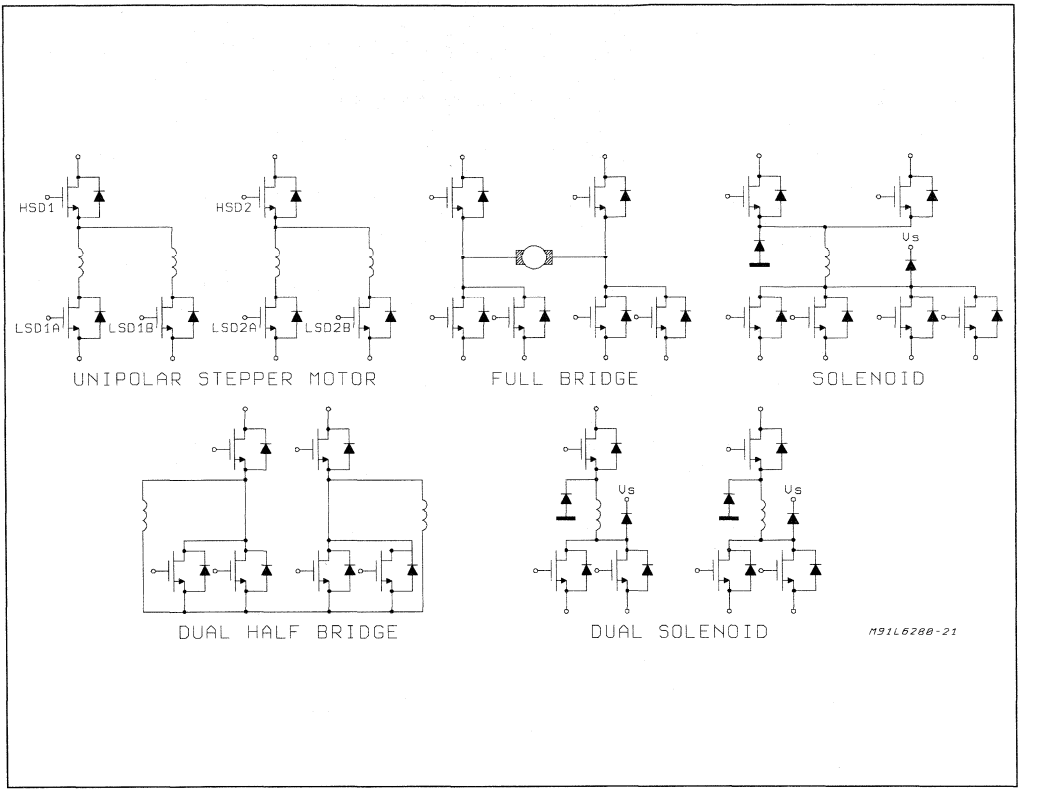
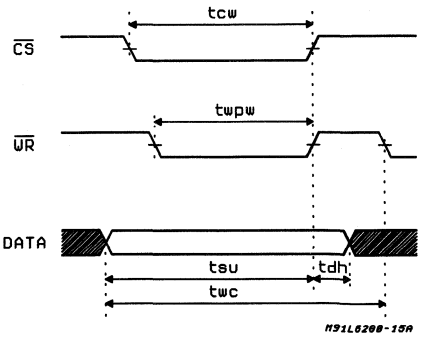


Figure 6: Write Cycle



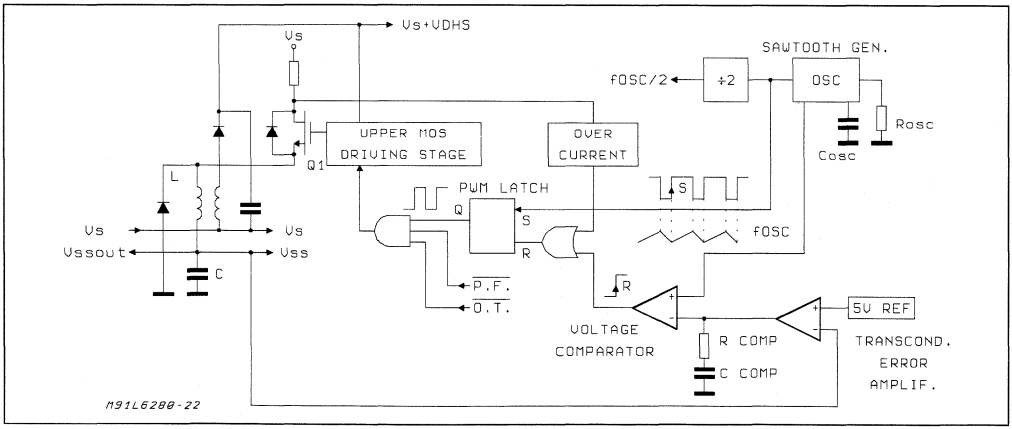
SYSTEM DESCRIPTION (Refer to the Block Diagram)

The L6280 is a single chip power microsystem which includes drives for three different loads, the associated control logic and a Switched Mode Power Supply (SMPS) at $V_{SS} = 5V \pm 5\%$.
The IC can be directly connected to a standard microprocessor because of its common I/O interface architecture. The L6280 can exchange information regarding the load driver and the control method via a 8 bit data bus. The block named microprocessor interface decodes the first four bits (A0....A3), which, depending on the content of the remaining four (D0.....D3) are used to enable the power DMOS, to activate the PWM loop, and finally to set the D/A output value.
The power stage can be divided into 3 channels. Channels1 and 2 have 6 DMOS transistors each one (2high side drivers with $R_{dson} = 1\Omega$, 4 low side drivers with $R_{dson} = 2\Omega$). Depending on the application load, these driver transistors can be connected in different ways. The microprocessor, via software, must activate the proper control loop to optimize operation of different loads and output stage configurations. Because of this programmability in the control of the output configurations, a large variety of different loads can be driven by the same integrated circuit (see possible configuration for power stage on Figure 5) giving the greater system flexibility. Current levels up to 1A are possible from CH1 and CH2, limited primarily by the power dissipation of the IC.
The third channel has a fixed configuration intended to drive a solenoid. DMOS transistors with 0.5Ω R_{dson} are used to provide 4A max load capability.
All three channels have 3 bit current D/A resolution. Some auxiliary blocks of diagnostic and protection (e.g.: The power Fail/Reset and the watchdog) are provided to protect the system from microprocessor failure or power fail.

Figure 7: SMPS Block Diagram

Step Down Switchmode Power Supply (See Figure 7).

The step down switchmode power supply contains a DMOS power stage with 1Ω R_{dson} (Q1), control circuitry, diagnostics and protection circuits; a regulated voltage (V_{SSout}) is used to drive some of the internal circuit blocks and the external microprocessor and memories. Thanks to the DMOS output stage this regulator can deliver a continuous output power of 4W (5V; 0.8A) with an efficiency betler than 90% at a typical frequency of 80kHz.
The regulation loop uses a classical pulse width modulation circuit that includes a sawtooth generator, an error amplifier, a voltage comparator and a PWM latch. A precision 5V reference is generated and trimmed on chip to guarantee a 5% tolerance. This reference is used as voltage reference for the SMPS and the reference for the DACs.
The IC also provides an extra voltage (V_S+V_{DHS}) for the correct driving of the high side drivers. These transistors require a gate voltage higher than the supply voltage Vs to obtain the minimum ON resistance. Because of the v ery low current needed to drive DMOS transistors, this auxiliary voltage is easily obtained from a second winding on the inductor of the LC output network (see Application Information).
An overcurrent protection circuit is included to turn OFF the power transistor when a current level of 1.2A is exceeded.
The SMPS block also includes a voltage sensing circuit to generate a power ON reset signal for the microprocessor. This Power Fail circuit senses the input supply voltage and the output regulated voltage and sets the Reset-out pin to the high voltage only when both the sensed voltages are correct.
Finally, the SMPS block is able to deliver $f_{OSC/2}$ used in the actuation stage for the PWM control of the current (CH1; CH2 and CH3).



Pwm Current Control Loop

The current control is achieved big a cycle of charge (T_{ON}) and discharge (T_{OFF}) of the energy stored in each couple of windings of the driven motor (MA and MB). Fig. 8 shows the windings MA of an unipolar stepper motor during T_{ON}. FF1 is setted by the clock pulse and the transistor Q_A is ON. At the moment $Q_1$is ON the current exponentially increases until $R_S \times I_P$ equals V_{REF}.

A reset pulse is produced, Q_A is switched OFF and Q_2 is switched ON (Fig. 9). Since the magnetic flux $0_{MA} = N_A I_P$ cannot suddenly change and since the coil tourus number in the discharge loop is doubled, the peak current I_P modifies it self into $I_P/2$. The OFF time is characteryzed by a slow recirculation of the current $I_P/2$ that decreases until a new clock pulse sets a new T_{ON} configuration. To control the current in two separate windings MA and MB with just one sense resistor RS and one comparator, a special PWM control loop based on a "time sharing" technique (Patented) is used (Fig. 10).

In this configuration the chopping frequency, that defines the $T_{ON} + T_{OFF}$ period of each phase, is halved by FF3 that drives ON G1 and G2 alternately. During T_{OFF} of one winding, for instance MA (and Q_A is OFF), its current does not flow throught the sensing resistor that can be used to monitor the current that flows through the second winding MB, allowed by the ON-status of Q_B.

Fig. 11 shows a simplified timing before and during the phase change from AB to $\overline{AB}$ (CCW, full step). It can be seen that before the time t_1, I_A and I_B are alternately controlled in a chopping period Tch1 of 4 oscillator periods or two clock periods. The time sharing is 50% - 50% and the chopping frequency is typically of 20KHz (f_{osc} = 80KHz).

Afther the time t_1, as soon as $I_{\overline{A}}$ is sensed, a different time sharing is generated. In fact since a Reset pulse is last after one clock pulse, FF2 can drive FF3 to change for I_B chopping only at the next clock pulse (Fig 10; Fig 11).

This means that the chopping time becomes Tch2 = 6 oscillator pulses, the frequency decreases to 16.6KHz (f_{osc} = 80 KHz) and the time sharing becomes of 67% - 33%.

At the end of the phase change period tphc the time sharing comes back to 50% - 50% again. It can be noted that this behaviour allows a faster phase change and then a higher speed of the motor. The cost of that, is the increase of the T_{OFF} of the unchanged phase B and then a small increase of the ripple of the current I_B (see $\Delta I_{B1} < \Delta I_{B2}$ in Fig. 11).

This time sharing current control method is also used when two indipendent load are driven by one single channel. when only one load is present, such as a DC motor could be, the time sharing is automatically switched OFF and the PWM frequency becomes $f_{osc}/4$ = 20KHz. Table 1 shows how the reference voltage can be modified with a three bits DAC to allow microstepping operations (see below).

Figure 8 - T_{ON} Configuration: Motor Windings MA (A; $\overline{A}$).

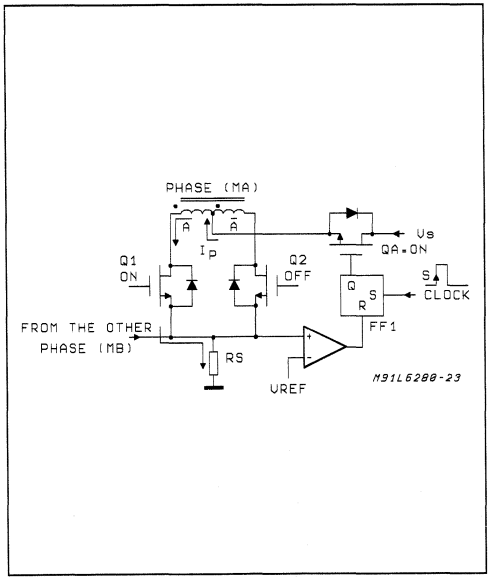


Figure 9 - T_{OFF} Configuration: Motor Windings MA (A: $\overline{A}$).

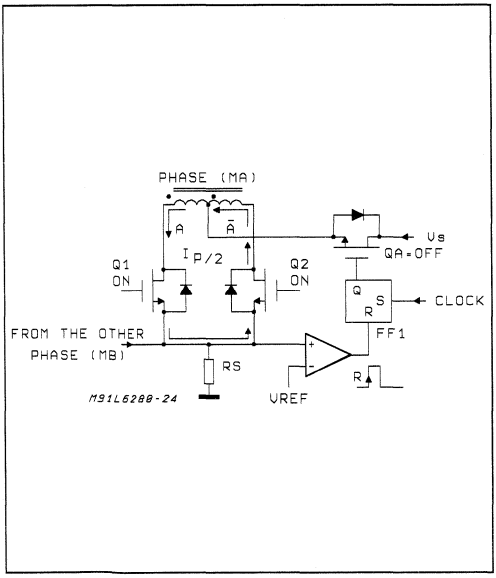


Figure 10 - PWM Current Control Loop. Time Sharing Technique.

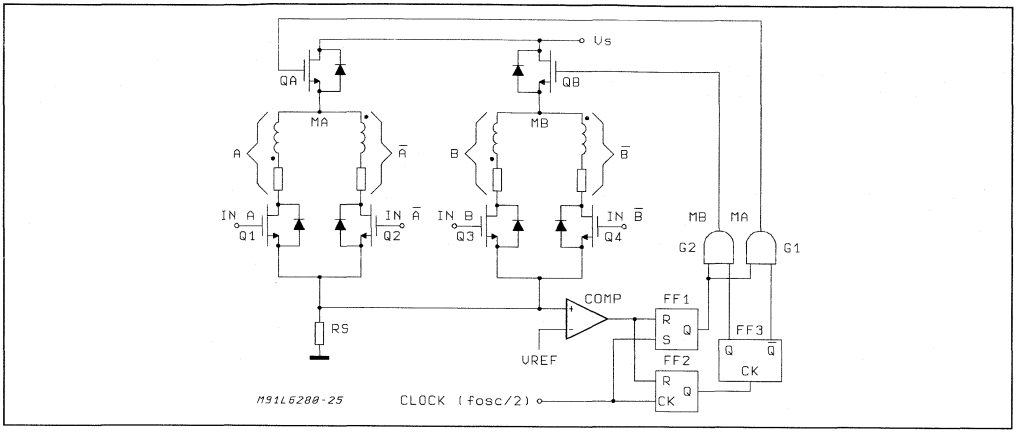
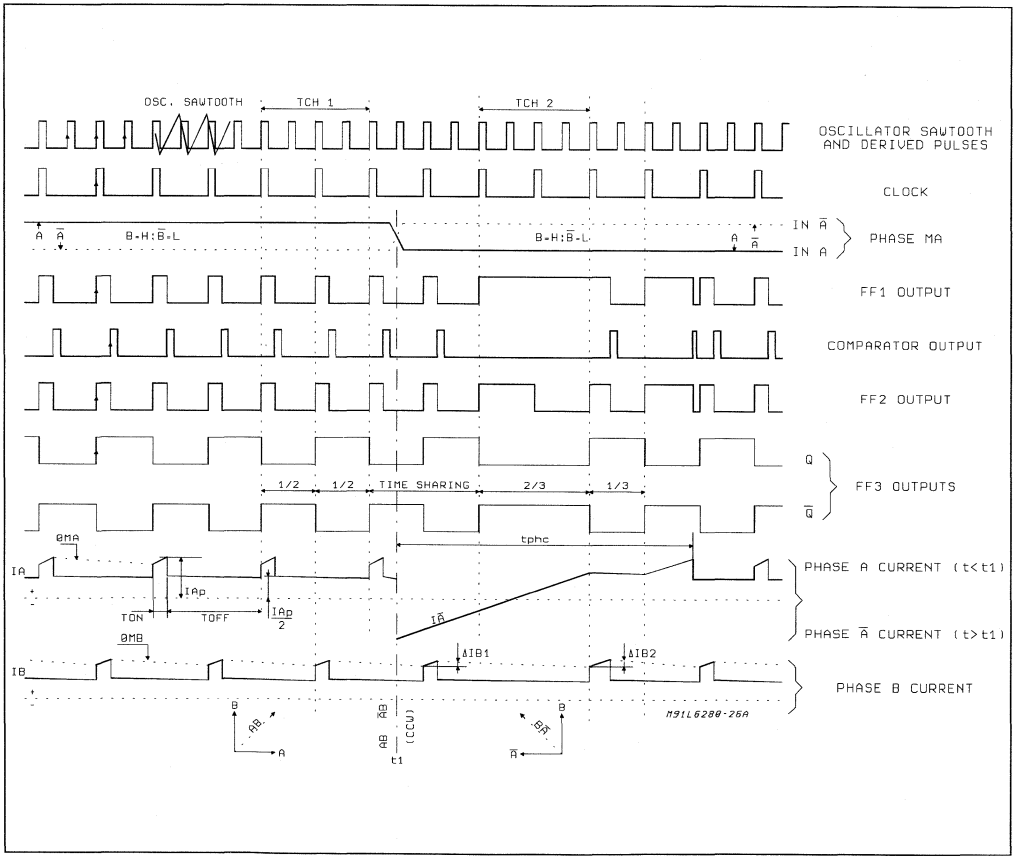


Figure 11: Chopping Characteristics (simplified)



Digital/Analog Converters (DACs)

The output current levels are programmed by 5DACs each with 3 bit resolution. Channels 1 and 2 each have 2 DACs, one for the left part of the output stage and the other for the right part. When the output stage is used to drive only one load (as with DC motors), the L6280 uses only the right register. Channel 3 has only 1 DAC.

Microstepping operation is easily performed with channels 1 and 2. The value of each DAC can be changed in two ways:

a) the new value can be directly generated by the microprocessor and then loaded into the specified DAC;
b) the value of a DAC can be incremented or decremented by 1; in this case the microprocessor during acceleration or deceleration has only to indicate the DAC on which operate and the type of the operation, reducing the CPU's burden.

The correspondence between the DAC value and the Vref level is shown in table 1.

Table 1

D2	D1	D0	V_{ref}	UNIT
1	1	1	1	V
1	1	0	0.875	V
1	0	1	0.75	V
1	0	0	0.625	V
0	1	1	0.5	V
0	1	0	0.375	V
0	0	1	0.25	V
0	0	0	0.125	V

Iload = 0 is obtained by disabling all low-side drivers.

Turn ON/OFF Characteristics and Program Sequence

During power-on the Switchmode Power Supply output stage is turned OFF till V_S reaches V_{PFth}. The pin Reset Out is held low and remains low till V_{SS} is < V_{SSFth} (the power stages and the logic of the L6280 are disabled.

Not correct signals coming from the microprocessor are then ignored; the microprocessor on the other hand, receives a low state signal from the Reset Out pin. When the V_{SS} output is stabilized during a delay t_D set by the C_D capacitor, the pin Reset Out goes to the high level; the microprocessor is enabled to work while the L6280 is in stand-by waiting for a keyword and initialization sequence. Every command that arrives before the keyword is ignored. At this time the programming sequence can start according to the flow diagram (Fig. 12).

At first the Keyword (00111010) has to be sent to the L6280 to activate the watch - dog function that begins to control the microprocessor functionality. From this moment the microprocessor must send periodically the Watch-dog word (00110101) otherwise its absence is interpreted as a microprocessor failure: to prevent any damage both in the load and in the IC, the L6280 itself disables the power stages. No reset signal is generated towards the CPU; the system must restart the sequence from Power-ON.

The next step is to set the configuration of channel 1 and channel 2 output stages by the initialization word. The configuration can be chosen to fit in the load characteristics. To do this the microprocessor generates a word with A0, A1 = 0 and where A2, A3 choose the channel to be configured, D0 to D3 choose the type of configuration (unipolar, dual half bridge or full bridge; see Data and Address decoding). Every input configuration different from the allowed initialization word is ignored.

When the initialization arrives, the L6280 sets the configuration of the output stage of the chosen channel. The initialization word has to be repeated for the other channel (CH1 or CH2 only). If two initializations arrive for the same channel, the L6280 disables the output stages while pin Reset Out goes low for a time Td to advise the mocroprocessor about the uncorrect condition. The program sequence must restart from the Keyword step. After the initialization step is succesfully completed the L6280 begins to accept commands. If a command is sent before the relative channel has been configured, the command is neglected.

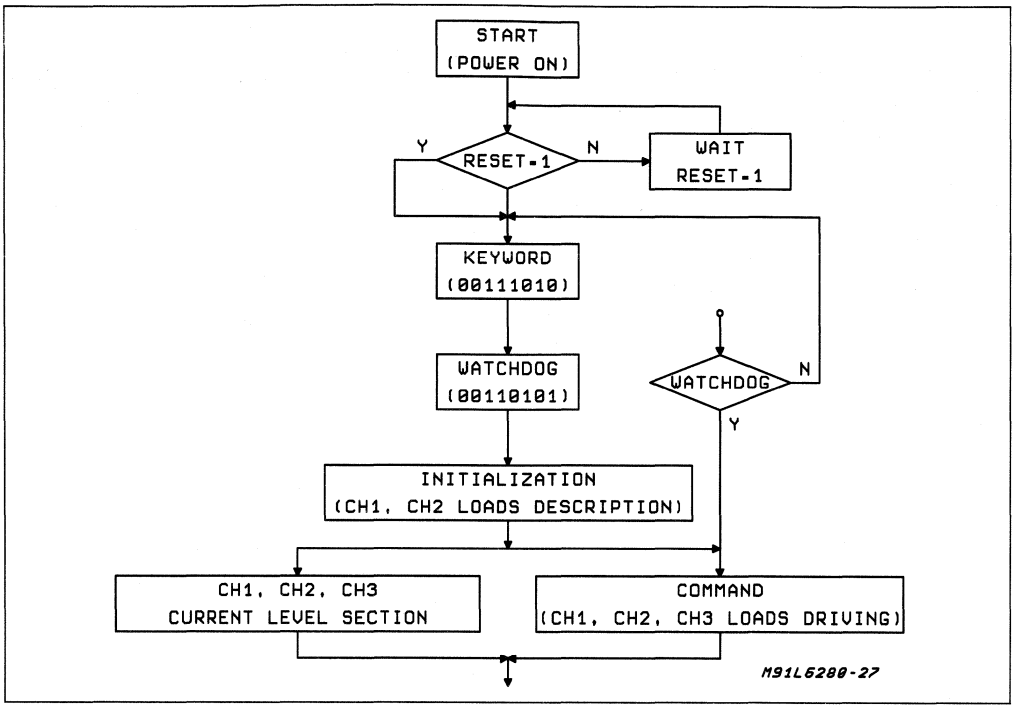
Command can be of three type:

a - selection of current level loading a DAC;
b - increment or decrement of a DAC;
c - selection of the driving strategy of a channel (e.g. half/full step, fast/slow decay and so on).

To select the current level is necessary to load a value into the appropriate DAC. The microprocessor must select the channel via A2, A3 and (only for channel 1 and 2) left or right DAC via D3; the value of D0,....D2 are loaded in the chosen DAC. There are two possibilities of changing the value of a DAC; the first one is to load directly the new value, the second one is to cause an increment or a decrement in a DAC, in this way the burden of the microprocessor can be partially decreased generating inc/dec command without calculating the value.

To increment od decrement a DAC the microprocessor must select the channel via A2,A3, left or right DAC and the operation via D0 to D3 according to truth table in Datas and Address Decoding (see below). The increment or decrement is done immediately after the arrive of the command. For every configuration of the output stages are possible different type of driving strategy explained in Datas and Address Decoding.

Figure 12: Program Sequence



Data and Address Decoding

SPECIAL WORDS

A3	A2	A1	A0	D3	D2	D1	D0
0	0	1	1	1	0	1	0

KEYWORD

This word is used during the start-up procedure to enable operations; all settings arrived before the keyword are reset.

A3	A2	A1	A0	D3	D2	D1	D0
0	0	1	1	0	1	0	1

WATCHDOG

The microprocessor must periodically generate this word; the value of the maximum period is set by the capacitor C_D. The absence of the Watchdog is interpreted by L6280 as a microprocessor failure. The maximum period is:

$$T_{WD} = C_D \times 1.5 / (50 \times 10E\text{-}6)$$

Except for special words (keyword and watchdog), the input words are organized like the following:

A0 A1 Operation selection

A2 A3 Channel selection

D0 D1 D2 D3 Datas

A0,A1 DECODING (OPERATION SELECTION)

A0,A1 select the type of operation (channel initialization, commands, DACs loading, DAC increment/decrement).

A0 A1

0 0 This configuration is used to send the information about the configuration of the vchannel specified by A3 and A2; D0 to D3 are used to specify the configuration of the channel (full bridge, dual half bridge, unipolar motor).

A0 A1

1 0 This configuration is used to change driving strategy of the output stages of the channel specified by A3 and A2 (full/half step, slow/fast decay and so on). The driving strategy is coded in D0 to D3, and depends from the configuration of the output stage.

A0 A1

0 1 This configuration is used to load the value of a DAC of the channel selected by A3 and A2. D3 indicates right and left DAC just for channel 1 and 2.

A0 A1

1 1 This configuration is used to cause an increment or a decrement of a DAC. Right or left DAC and inc/dec are selected by D0 to D3 value.

A2, A3 DECODING (Channel Selection)

Every time a command or a initialization is sent to the L6280, a channel must be selected. This is done via A2 and A3 according to the table.

A2	A3	
0	1	Select channel 2
1	0	Select channel 1
1	1	Select channel 3
0	0	Used only with keyword and watchdog

D0 to D3 DECODING (Datas)

The meaning of D0, D3 changes according to the value of A0, A1

A0 A1

0 0 When A0, A1 are in this configuration, and channel 1 or 2 is selected, the data appearing in D0 to D3 set the output power stage configuration to fit the chosed load according to the allowed Truth Table. There is no need to configure channel 3.

	D3	D2	D1	D0	Possibie configurations for channels 1 and 2
	0	0	0	0	Null (power disabled)
a	0	0	0	1	Unipolar motor
b	0	0	1	0	Full Bridge
c	0	0	1	1	Dual Half Bridge

a) Unipolar Motor Configuration

In this configuration D0 to D3 directly drive the low side drives:

D3	D2	D1	D0	Configurations	
0	0	0	0	Low side drivers 1,2,3,4 OFF	
0	0	0	1	Low side drivers 2,3,4 OFF	Low side driver 1 ON
0	0	1	0	Low side drivers 1,3,4 OFF	Low side driver 2 ON
0	1	0	0	Low side drivers 1,2,4 OFF	Low side driver 3 ON
0	1	0	1	Low side drivers 2,4 OFF	Low side drivers 1,3 ON
0	1	1	0	Low side drivers 1,4 OFF	Low side drivers 2,3 ON
1	0	0	0	Low side drivers 1,2,3 OFF	Low side driver 4 ON
1	0	0	1	Low side drivers 2,3 OFF	Low side drivers 1,4 ON
1	0	1	0	Low side drivers 1,3 OFF	Low side driver 2,4 ON

The following configurations are not allowed: the microprocessor does not to generate them otherwise they can cause faulty operations.

D3	D2	D1	D0	
0	0	1	1	Always not allowed
0	1	1	1	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	This configuration is not allowed when driving a unipolar motor and it is permitted only to drive a high current solenoid.

b) Full Bridge Configuration

In full bridge configuration D0 to D3 set the driving strategy of the bridge:

D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Chopper left, brake right
X	0	1	0	Chopper right, brake left
X	0	1	1	Brake left, brake right
X	1	0	0	Tristate left and right
X	1	0	1	Diagonal chopper
X	1	1	0	Inverted diagonal chopper
X	1	1	1	Tristate left and right

c) Dual Half Bridge Configuration

D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Brake right, chopper left
X	0	1	0	Brake right, chopper right
X	0	1	1	Brake left, brake right
X	1	0	0	Chopper left, chopper right
X	1	0	1	Tristate left, chopper right
X	1	1	0	Tristate right, chopper left
X	1	1	1	Tristate left and right

CHANNEL 3

For channel 3 only D0 has a meaning: it directly drives the low side driver DMOS. When D0 = 0 the low side driver DMOS is switched OFF and the current flows through external recirculation diodes.

A0 A1

1 0 When A0, A1 are in this configuration, D0 to D3 are used to set the strategy of the output power stages according to the output stage configuration previously selected.

A1 A0

1 0 When A0, A1 are in this configuration, D0 to D2 are loaded into left or right winding D/A converter, according to D3 value (only for channel 1 and 2)

D3

0 Left channel DAC

1 Right channel DAC

For channel 3, D0 to D2 are loaded into the unique DAC.

A1 A0

1 1 When A0, A1 are in this configuration, the value of D0 to D3 causes an increment or a decrement of the content of left/right DAC of a channel. The inc/dec operation and the DAC register selection (right or left) are selected according to the following truth table:

D3	D2	D1	D0
dec LEFT	inc LEFT	dec RIGHT	inc RIGHT

The change in DAC registers is done immediately after receiving the data.The configurations D3, D2 = 11 and D1, D0 = 11 are not allowed. (Them can cause faulty operations) Channel 3 has only one DAC; the change in its value is done according to D0,D1 value.

D1	D0
dec DAC	inc DAC

D1, D0 = 11 is not allowed (they can cause faulty operations).

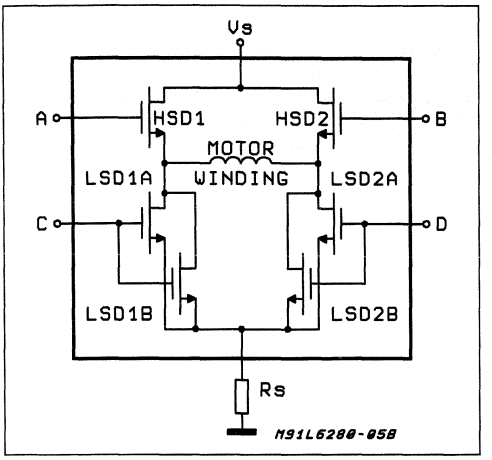
Output Operation

In full bridge and dual half bridge configurations, the output stages will operate according to D1, D2, D3 values.

FULL BRIDGE CONFIGURATION (CH1 and CH2)

In full bridge configuration the cennection between the output of the high side drivers and the corresponding low side drivers has to be made with external jumpers. The output stage diagram here below (Fig. 13) must be substituted inside the blank boxes in the following block diagrams.

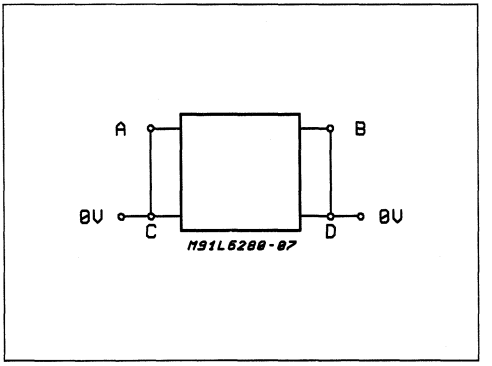
Figure 13



D0	D1	D2	D3	
X	0	0	0	Tristate left and right

All output DMOSs of the channel are OFF (Fig. 14)

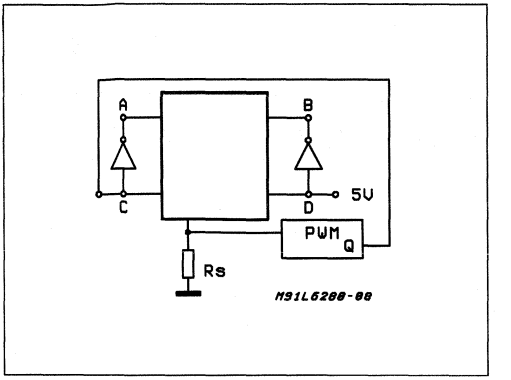
Figure 14



D0	D1	D2	D3	
X	0	0	1	Chopper left side; fixed right side (one phase chopping)

The left side of the bridge is controlled by the PWM loop while HSD2 is held OFF and LSD2A and 2B are held ON. During ON time (Q low) the current flows thrugh HSD1, motor winding and LSD2A and 2B. During OFF time the current can recirculate through LSD1A, 1B, 2A and 2B (Fig. 15)

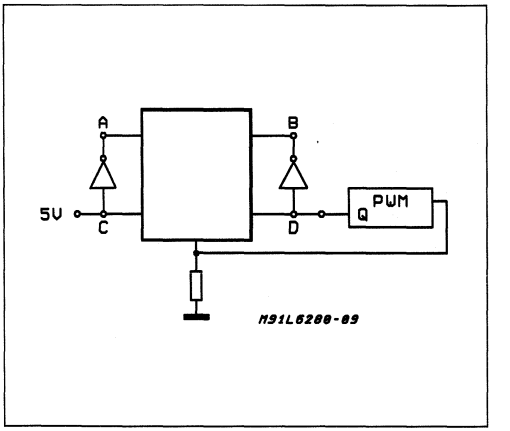
Figure 15



D0	D1	D2	D3	
X	0	1	0	hopper right side, fixed left side (one phase chopping)

As above but with the two channel exchanged each to other (Fig. 16).

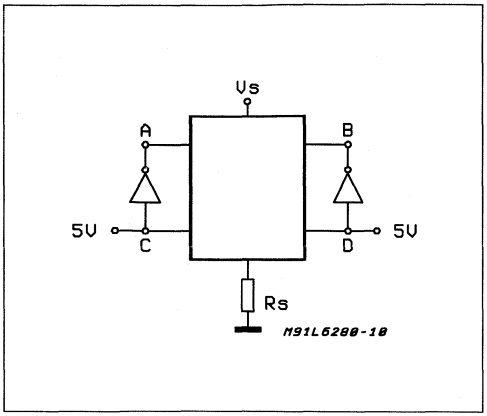
Figure 16



D0	D1	D2	D3	
X	0	1	1	Fixed both left and right (brake action)

All High side drivers are held OFF while all low side drivers are held ON. The motor winding is short circuited through the low side drivers; the motor's back EMF acts as a brake voltage (Fig. 17).

Figure 17

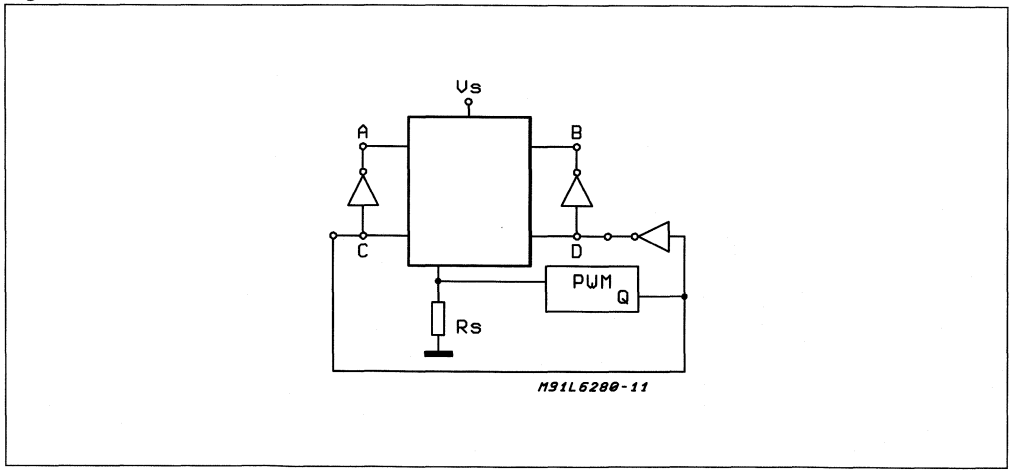


D0	D1	D2	D3	
X	1	0	0	Three state left and right (see X000 configuration)

D0	D1	D2	D3	
X	1	0	1	Diagonal chopper (Two phase chopping)

During On time (Q=LOW) the current flows through HSD1, motor winding and LSD2A and 2B. During OFF time (Q = HIGH) the current can recirculate through LSD1A and 1B motor winding and HSD2 (Fig. 18).

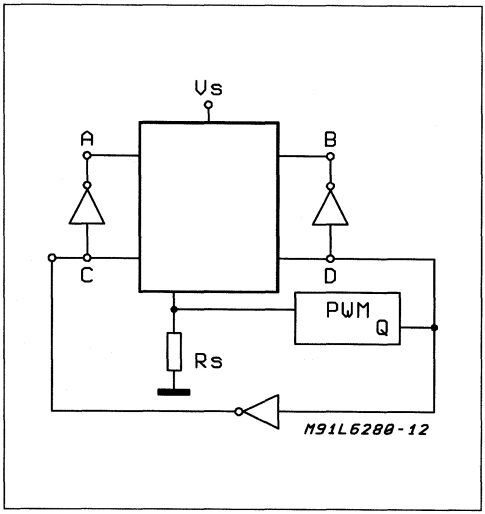
Figure 18



D0 D1 D2 D3 INVERTED DIAGONAL CHOPPER (Two phase chopping)

During ON time (Q = LOW) the current flows through HSD2, motor winding and LSD1A and 1B. During OFF time (Q = HIGH) the current can recirculate through LSD2A and 2B motor windind and HSD1 (Fig.19).

Figure 19

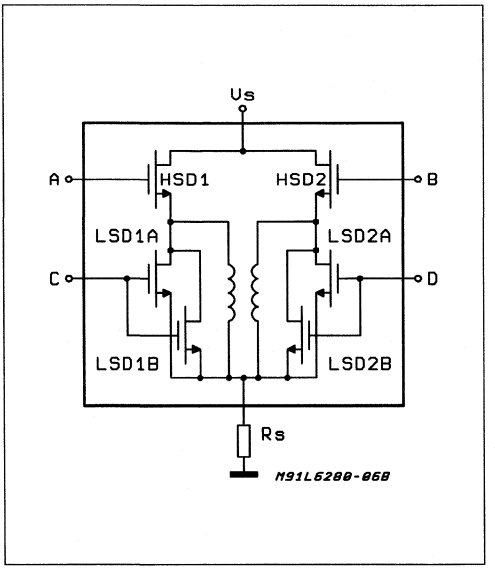


D0	D1	D2	D3	
X	1	1	1	Tristate left and right (see X000 configuration)

DUAL HALF BRIDGE CONFIGURATION (CH1 and CH2)

In dual half bridge configuration the connection between the output of the high side drivers and the corresponding low side drivers has to be made with external jumpers. The output stage block diagram shown in figure 20 must be substituted in side the blank boxes in the following block diagrams. In dual half bridge configuration, the time sharing strategy is always used.

Figure 20

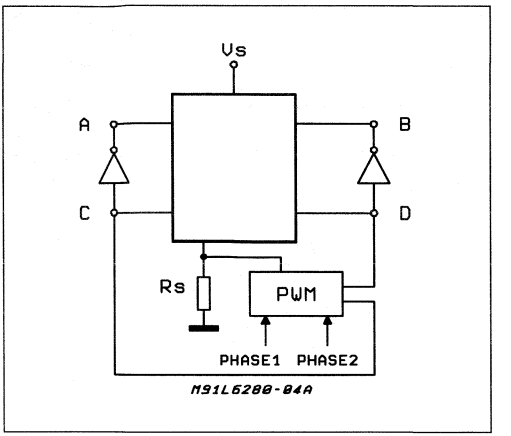


D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Chopper left, fixed righ
X	0	1	0	Chopper right, fixed left
X	0	1	1	Fixed left and right. For these configurations, see the corresponding shown in Full Bridge Configuration paragraph (Page 14/24).

D0	D1	D2	D3	
X	1	0	0	Chopper left chopper right

As foreseen when in unipolar motor configuration(see Figure 5), the time sharing strategy is used (see Figure 10), so when the current in left winding is controlled, the current in right winding recirculate trough the low side drivers and not through the sense resistor (Fig. 21).

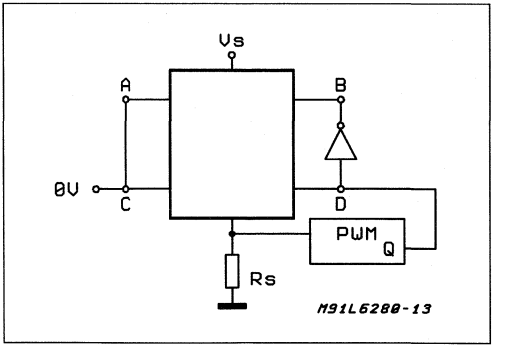
Figure 21



D0	D1	D2	D3	
X	1	0	1	Tristate left, chopper right

During ON time (Q = LOW) the current flows through high side driver HSD2, right winding and sense resistor. During OFF time the current recirculate through winding and side drivers LSD2A and LSD2B (Fig. 22).

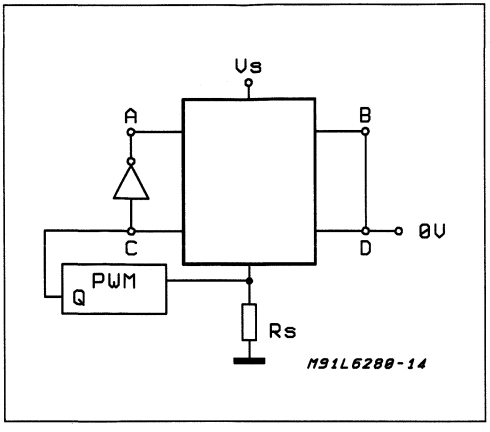
Figure 22



D0	D1	D2	D3	
X	1	1	0	Tristate right, chopper left

During ON time (Q = LOW) the current flows through high side driver HSD1, left winding and sense resistor. During OFF time the current recirculate through the winding and low side drivers LSD1A and LSD2A (Fig 23).

Figure 23



D0	D1	D2	D3	
X	1	1	1	Tristate left and right (see X000 configuration of full bridge).

APPLICATION INFORMATION

An application circuit useful to test the performance of the L6280 can be formed as shown on Figure 24: CH1 drives one unipolar stepper motor, CH2 drives a DC motor, CH3 drives one solenoid and the SMPS can supply continuously 0.5A.

If the Watch Dog and the Chip Select functions are not of interest, pins 22 and 23 must be grounded. Each sensing resistor would be obtained by the parallel of two or more metal film resistor of the same value to minimize their series equivalent inductance.

Generally, optimum stability of the SMPS voltage control loop, is achieved by a series network made by 1nF and 39 KΩ (see pin 15) and by using an output capacitor of 100µF having an equivalent series resistance of 100 mΩ (see pin 14): the most of the unexpensive aluminium electrolithic capacitors can be right.

The snubber network at the secondary winding of the step-down inductor can be saved by accepting a not regulated voltage at the Charge Pump input pin 13. This condition is not recommended when the supply voltage and/or the SMPS output current changes too much (for instance respectively 20V ± 30% and/or 100 to 800 mA).

The inductance value of the primary winding of T1 defines the peak-to peak current ripple that flows throught itself, that is the minimum output current that allows the correct behaviour in continuous mode of the SMPS; nevertheless, the device is not demaged if it is obliged to work in discontinuous mode at a low current level.

Figure 25 shows the characteristics of the transformer T1 suitable to be used on the Application of Figure 24:

The maximum output current is of 500 mA continuous but current peaks of 800 mA can be sinked out without the risk of the core saturation. To avoid the discontinuous mode, the minimum SMPS output current must be of 70mA. The rectified voltage trend for the high side gate drive at pin 13 is as shown on Figure 26.

Not equally cheap, the choice of a toroidal core for T1 can optimize the application.

Instead of this, another solution can be as in Figure 27a it is shown. This is a full wave rectifier of the voltage at pin 3; Z1 and R1 clamp the positive peak while the forward characteristic of the Zener rectifies the negative peak and charges C1. The recommended Zener voltage is of 12V.

Could happen that the V_{SS} output voltage is not requested because already available: in this case and only if at least one unipolar stepper motor is continuously driven, the solution shown in Figure 27b can be implemented. The step down output components can be left out.

The connection of the network is as follows:

A: to pin 4 (or pin 5) when the unipolar motor is driven via CH1;
to pin 41 (or pin 42) when the unipolar motor is driven via CH2;
B: to pin 1
C: to pin 13

The SMPS switching frequency is the same of the oscillator frequency that can be typically defined by:

$$f_{osc} = \frac{9}{RC}$$

Referring to Fig. 24 it is calculated f_{osc} = 82KHz.

CH3 is chopped at the same frequency. The output diodes must be chosen according to the solenoid working current (50ns of reverse recovery time or better): for a current less than 1 A, the PLQ08 is a good choice.

Driving one unipolar stepper motor, output protection diodes (Transil) are recommended: CH1 in Fig 24 uses four BZW04 - 48 diodes; when a low current motor is driven or a Vs less than 20V is supplied, four fast diodes and only one Zener diode can be used as a protection of the outpus (see Figure 28). The driving of DC motor needs the connection as shown for CH2 (full bridge configuration).

The drive of one bipolar stepper motor by using CH1 and CH2 both in full bridge configuration allows the use of a higher supply voltage level

hat however cannot exceed the Absolute Maxi-
num Ratings of 35V:a max value of 33V is rec-
ommended.

n this case, at each couple of outputs for the bi-
polar windings, a snubber network must be con-
nected. This network is done by the series of a re-
sistor and of one capacitor:

$$R_{snub} = V_S \text{ max/Imotor peak;}$$

$$C_{snub} = \text{Imotor peak/ (dv/dt)}$$

One dv/dt of 200V/µsec is generally a correct choice.

Of course, care must be taken in the Printed Circuit Board design regarding the ground paths and the high current loops.

An example of P.C.B. layout is shown in Figure 29ab; Figure 30 shows the Schematic Diagram of the circuit of the L6280 S.P.D. S.AB.

The driving signals useful for this board can be easily generated by using an additional board (EMU KIT 512) not described here.

On Figure 29a it can be observed the copper area near the I.C. is used to sink out the heat from the device. Useful thermal characteristics of the L6280 are shown in Figure 31 and 32.

Figure 24: Application Test Circuit of the L6280

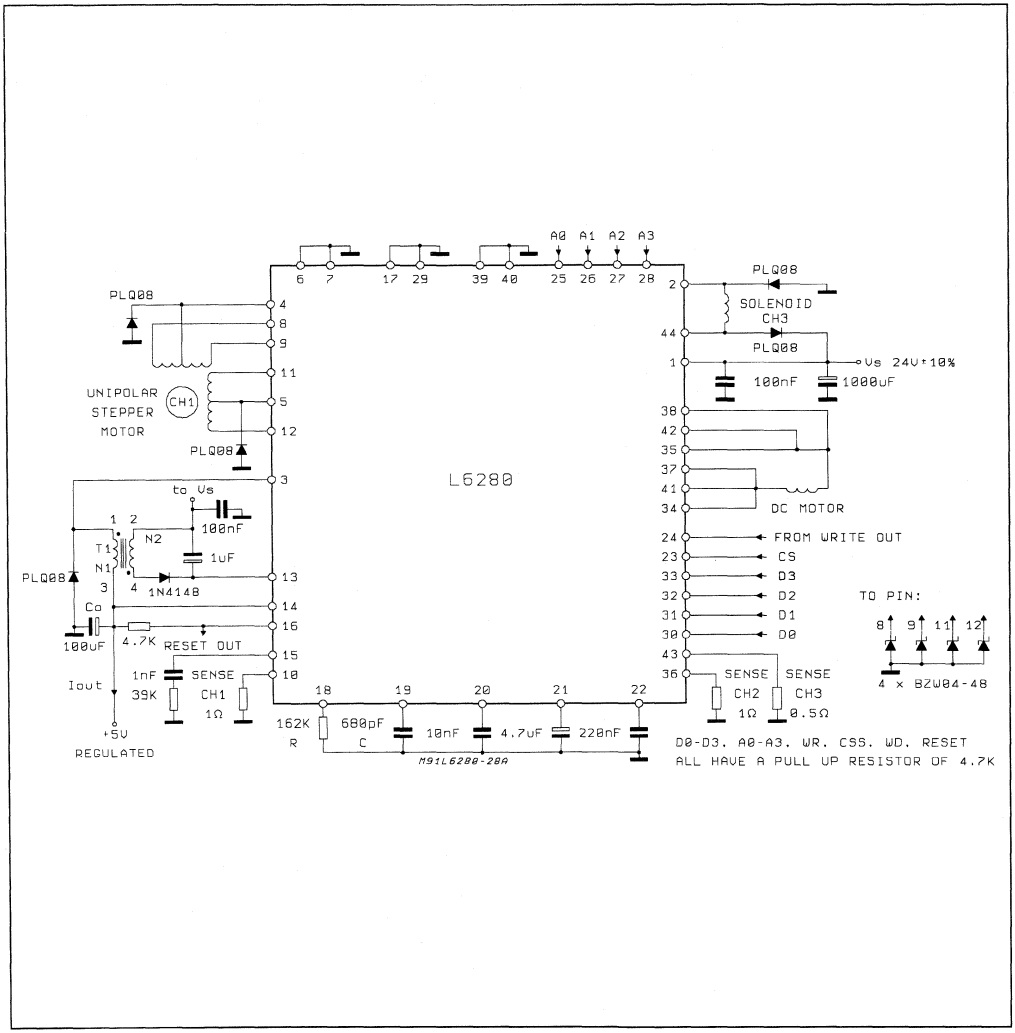
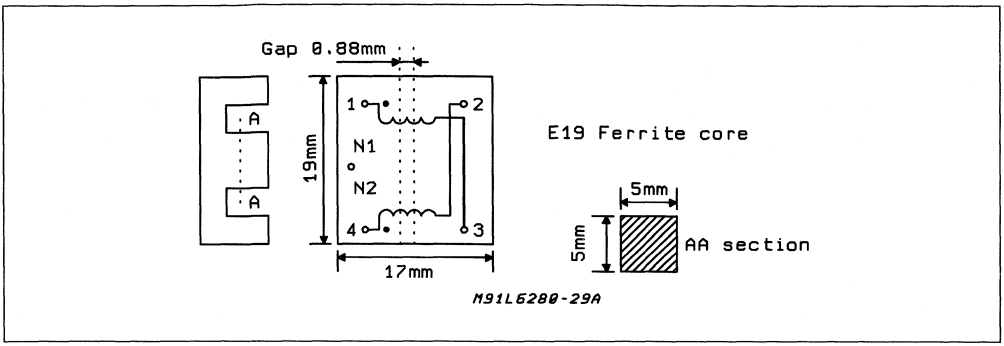


Figure 25: Characteristics of the Transformer T1.



N1: 118 tourns, copper wire ∅ 0.35mm
N2: 88 tourns, copper wire ∅ 0.2mm

TYPICAL PARAMETERS

N1	L_1 = 560µH R_1 = 680mΩ	@ 1KHz
N2	L_2 = 300µH R_2 = 1.5Ω	@ 1KHz

Figure 26: Charge Pump Voltage vs. Supply Voltage by using the transformer shown on Figure 25

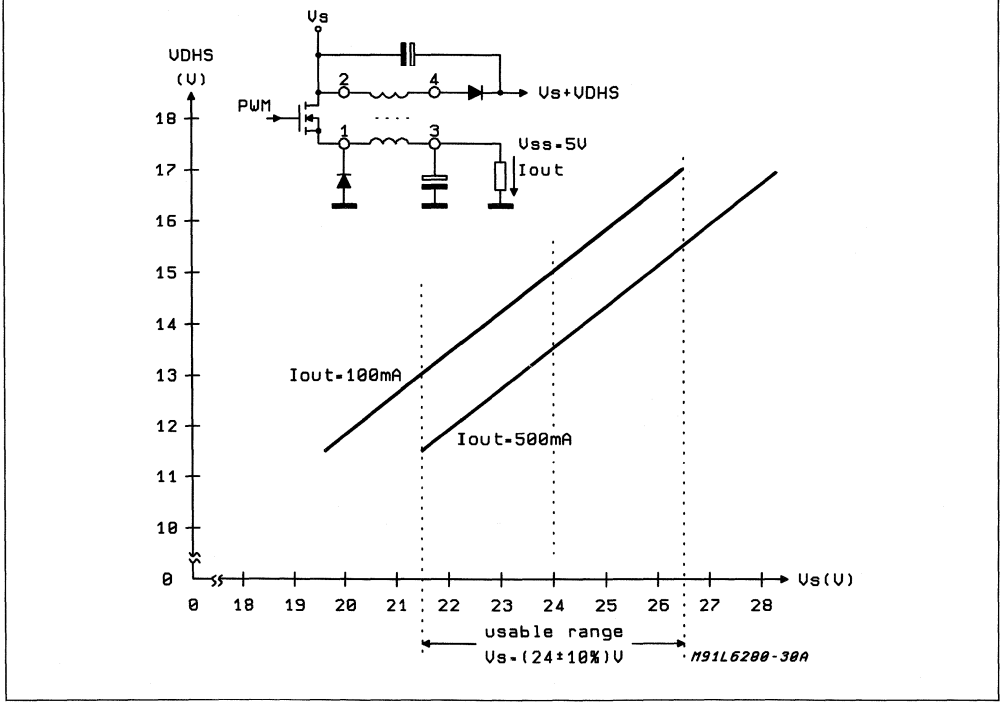


Figure 27a : Other Charge Pump Solution

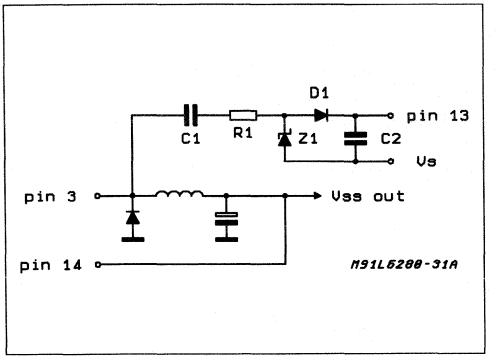


Figure 27b : Other Charge Pump Solution

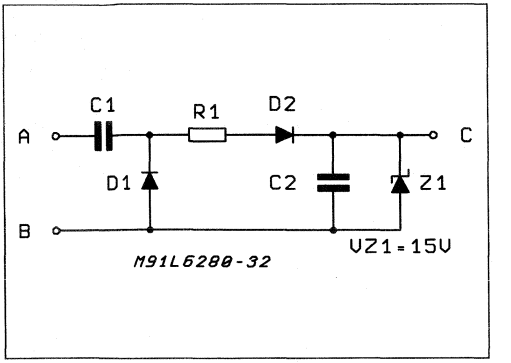


Figure 28 : Unexpensive Output Protection Network for the Unipolar Motor Driving

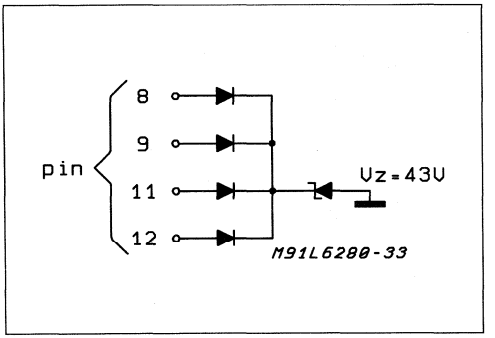


Figure 29a: L6280 PCB Components Side (1st metallization)

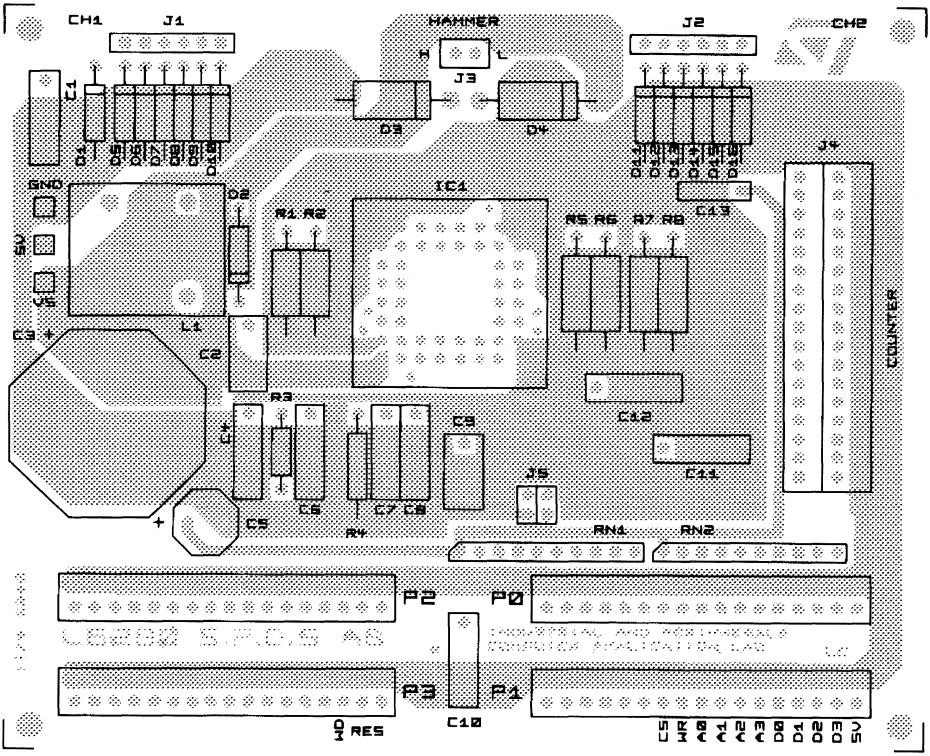


Figure 29b: P.C.B. Back Side (2nd metallization)

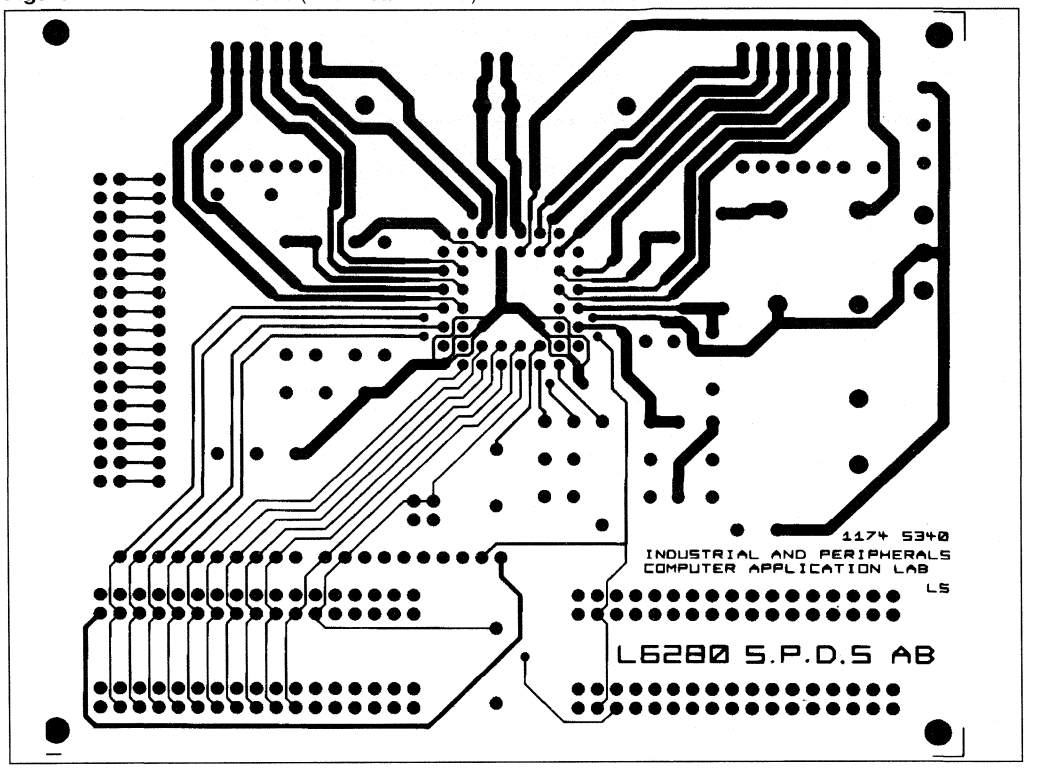


Figure 30: Schematic Diagram of the Circuit Assembled on the L6280-AB (Figure 29)

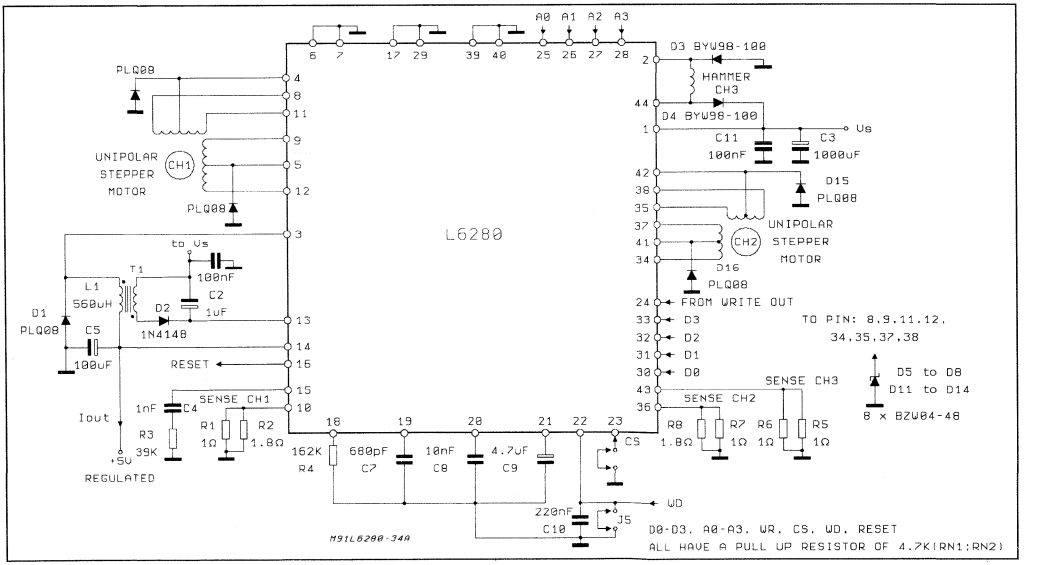


Figure 31; Typical Transient Thermal Resistance vs. Single Pulse Width.

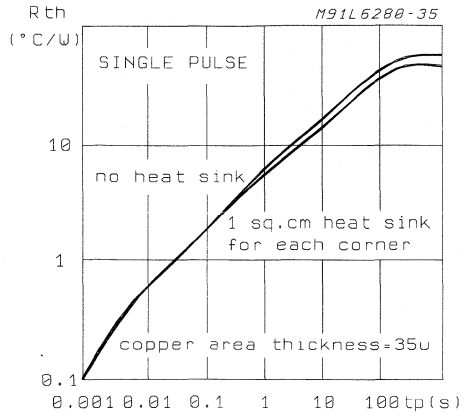
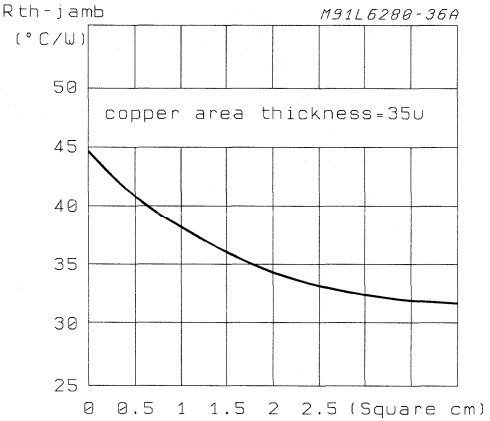


Figure 32; Typical Thermal Resistance vs. Heat-sinking Copper Area.

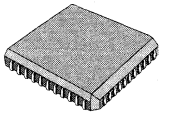


3 CHANNELS MULTIPOWER SYSTEM

ADVANCE DATA

- CHANNEL-A AND CHANNEL-B FOR UNIPOLAR STEPPER MOTORS
  - LOW SIDE: R_{DSON} = 1.2Ω
  - HIGH SIDE ; R_{DSON} = 1.2Ω
- CHANNEL-C FOR DC MOTORS
  - LOW SIDE: R_{DSON} = 1.7Ω
  - HIGH SIDE: R_{DSON} = 1.2Ω
- CHOPPING MODE DRIVING FOR C.L. CURRENT CONTROL ON CHA AND CHB AND O.L. VOLTAGE CONTROL ON CHC.
- INTERNAL FOUR DRIVING LATCHES
- 16 BIT INTERNAL SHIFT REGISTER
- DIRECT INTERFACE TO μP
- SERIAL DRIVING SEQUENCE LOADING
- CMOS COMPATIBLE INPUTS
- PRE-ALARM OUTPUT SIGNAL
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



PLCC44

ORDERING NUMBER: L6285

DESCRIPTION

This Combo Motor Driver uses large scale integration to incorporate several functions into the same chip.

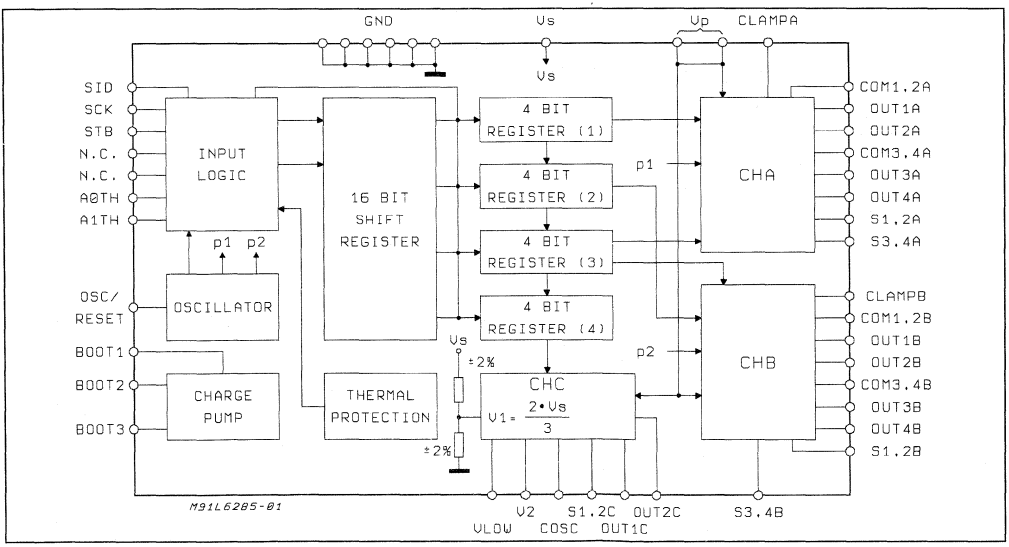
1) Two unipolar stepper motor driver
2) A full bridge DC motor driver
3) Serial microprocesor interface

The power output stages are DMOS and the input can be interfaced to a CMOS Microprocessor logic.

The phase current in the unipolar stepper motor windings is controlled by two external sensing resistors in fixed frequency chopping mode. The oscillator block provides clocks each other 180° out of phase to the two stepper motor driver in order to avoid symultaneous current peaks.

For the DC motor driver is used a bridge; the RMS voltage to supply this motor is fixed by a

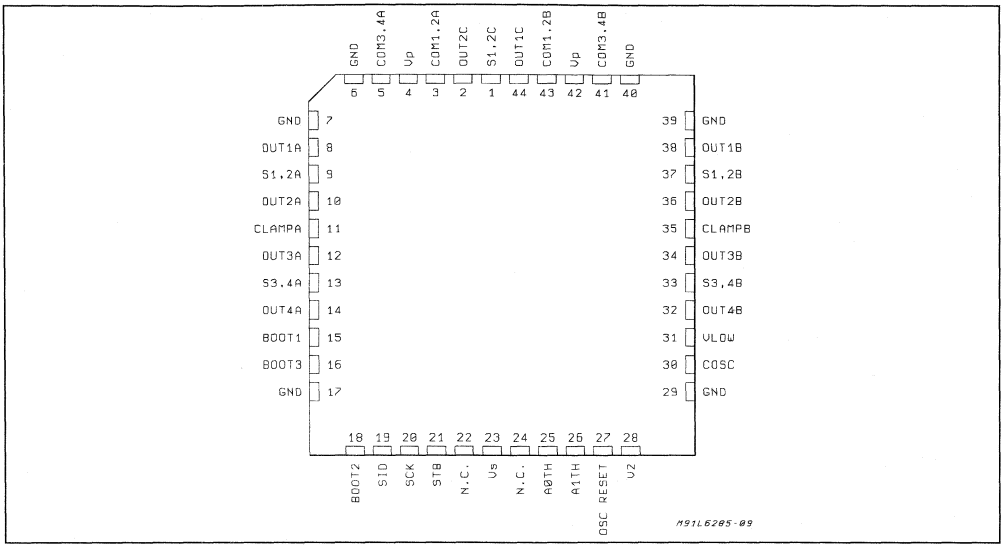
BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

simple PWM open loop. The 3 motors are controlled by the micro through 4 latches of 4 bit each. The loading of these registers is in serial mode. The I.C. operates at 5V supply for the logic and at 24V supply for the power stages. The package is the PLCC44 with 6 pins devoted to ground and to sink out the heat produced by power dissipation.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_P	Power Supply Voltage	30	V
V_S	Logic Supply Voltage	7	V
V_{in}	Logic Input Voltage	-0.3 to V_S + 0.3	V
I_{LOW}	Low Side DMOS max DC Current	1	A
I_{HIGH}	High Side DMOS max DC Current	1	A
I_{pLOW}	Low Side DMOS max Peak Current (1µs On; 50µs OFF)	2	A
I_{pHIGH}	High Side DMOS max Peak Current (1µs On; 50µs OFF)	2	A
V_{bout}	Max Output Voltage of Stepper Motor Driver (transient rcirculation)	60	V
V_{sense} 1;2	Max Voltage ON Vsense (CHA/CHB)	-1 to 2	V
V_{sense} 3	Max Voltage ON V_{sense} (CHC)	-1 to 2	V
I_{fdDC}	Max DC Current of Forward Diode (DMOS Source Drain Diode)	1	A
I_{fdpk}	Max Peak Current of Forward Diode (DMOS Source Drain Diode) (1µs On; 50µs OFF)	2	A
P_{tot}	Total Power Dissipation (Tpins = 90°C) With minimized dissipating copper area (T_{amb} = 70°C)	5 1.6	W W
T_{op}	Operating Temperature Range	0 to 150	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	50	°C/W

PIN DESCRIPTION

Pins	Name	Functions
1	S1,2C	Full bridge common source output to separate between power GND and logic GND.
2,44	OUT 1C, OUT 2C	Output of the channel C bridge.
3	COM 1,2A	High side DMOS channel A for current chopping in the windings connected pins to OUT 1A, OUT 2A.
4,42	V_p	Power Supply Voltage.
5	COM 3,4A	High side DMOS channel A for current chopping in the windings connected to pins OUT 3A, OUT 4A.
6,7,39,40	GND	PowerGround and heatsink pins.
8,10 12,14	OUT 1A, OUT 2A OUT 3A, OUT 4A	Low side DMOS outputs of channel A stepper motor driver.
9	S1,2A	Channel A sources of the DMOS OUT 1A, OUT 2A. A sensing resistor has to be connected from this pin and ground, for current control of phase 1,2 A.
11,35	CLAMP A, CLAMP B	These pins have to be connected to an external zener diode to clamp the output voltage spikes of channel A/B.
13	S3,4A	Channel A sources of the DMOS OUT 3A, OUT 4A. A sensing resistor has to be connected from this pin and ground, for current control of phase 3,4 A.
15	BOOT 1	A capacitor between this pin and V_p stores the overvoltage for each high side DMOS driver gate.
16	BOOT 3	A capacitor between this pin and internal diodes allows the change pump to transfer energy to the capacitor at the pin BOOT 1.
17,29	GND	Logic Ground and Heatsink pins.
18	BOOT 2	Charge pump oscillator output.
19	SID	Serial data input.
20	SCK	Serial clock for serial data input.
21	STB	Strobe to transfer the 16 bit shift register contents to the latch registers.
22,24	NC	Not connected.
23	V_s	Logic Supply Voltage.
25,26	A0TH / A1TH	Open collector outputs for thermal informations to the µP.
27	OSC/ RESET	An RC network connected to this pin defines the oscillator frequency for stepper drivers. When OSC/RES is <1V, a reset signal is internally generated.
28	V2	A voltage to this pin defines the output duty cycle of Channel C.
30	C_{osc}	A capacitor connected to this pin defines the chopping frequency of channel C.
31	V_{low}	This pin is low when the chopping low voltage (V2 low level) is selected; it is in high impedance when the chopping high voltage (V2 high level) is selected. Only for CHC operation.
32,34 36,38	OUT4B, OUT3B OUT2B ,OUT1B	Low side DMOS outputs of channel B stepper motor driver.
33	S 3, 4B	Same as S 3, 4A, but for channel B.
37	S 1, 2B	Same as S 1, 2A, but for channel B.
41	COM 3, 4B	Same as COM 3, 4A, but for channel B.
43	COM 1, 2B	Same as COM 1, 2A, but for channel B.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_S = 5V, V_P = 24V unless othewise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_P	Power Supply Voltage		9		26.5	V
I_P	Quiescent Power Supply Current	(note 1)			7	mA
V_S	Logic Supply Voltage		4.5		5.5	V
I_S	Quiescent Logic Supply Current	(note 1)			20	mA

LOGIC LEVEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{inL}	Input Low Voltage		-0.3		1.35	V
V_{inH}	Input High Voltage		3.15		V_S+0.3	V
I_{inL}	Input Low Current	$V_{in} = V_{inL}$	-10			µA
I_{inH}	Input High Current	$V_{in} = V_{inH}$			10	µA

CHANNEL A AND CHANNEL B (UNIPOLAR MOTORS)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSONL}	Low Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
R_{DSONH}	High Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
I_{DSSL}	Low Side DMOS Leakage Current	V_{DS} = 60V; output OFF			2	mA
I_{DSSH}	High Side DMOS Leakage Current	V_P = 30V; V_O= 0V	-1.5			mA
V_{REF}	Voltage reference to the Comparator	LEVEL 1 LEVEL 2 LEVEL 3 LEVEL 4	100 220 340 465	125 250 375 500	150 280 410 535	mV mV mV mV
T_d	Turn OFF Delay on HIGH Side DMOS after the Sensing Current Reach the Threshold Value	(note 2)			1	µs
f_{max}	Max Chopping Frequency				40	KHz

CHANNEL C (DC MOTORS) (see Fig. 5)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{osc}	Oscillator Frequency	Cosc = 3.3nF; V1 = 2/3V_S	17	22	28	KHz
DC	Duty Cycle	V2 = 1/2V_S	72	75	81	%
I_{b2}	Comparator Input Bias	V2 = 200mV	-1			µA
V_{low}	Open Drain Output	I = 5mA		0.2	0.4	V
R_{DSONH}	High Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
R_{DSONL}	Low Side DMOS ON Res.	I_{DS} = 0.7A			1.7	Ω
I_{LH}	HSD MOS Leakage Current	V_P = 30V; V_O = 0V	-1			mA
I_{LL}	LSD MOS Leakage Current	V_O = 30V; V_{sense} = 0V	-1.5			mA
V_{fddc}	Forward Diode DC Voltage (DMOS Diode)	I_{fdcc} = 0.7A		1.4	2	V
f_{max}	Max Chopping Frequency				40	KHz
V_{boot}	Voltage on pin Boot1		V_p +7			V
$I_{L\ boot}$	Leakage Current on pin Boot1	$V_{bott} = V_p$ +12V; V_p = 26.5V			200	µA

ELECTRICAL CHARACTERISTICS (continued)

OSCILLATOR (see Fig. 6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{osc}	Oscillator Frequency Pin OSC/RESET	C_{OSC} = 3.3nF; R_{OSC} = 10KΩ	27	41	46	KHz
T_{dsc}	Capacitor Discharge Time (protect dead time)	C_{OSC} = 3.3nF; R_{OSC} = 10KΩ (see Fig. 1)	0.8	1.4	2	µs
V_{reset}	Reset Threshold Voltage		1			V

INTERFACE TIMING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t1	SCK Data Clock Cycle	(see Fig. 2)	200			ns
t2	SCK Data Set-upTime		30			ns
t3	SCK Data Hold Time		20			ns
t4	SCK-STB Interval Time		30			ns
t5	STB Pulse Width		100			ns

Note 1: No output loaded; all register to low condition; no reset applied; V_P = 26.5V; V_S = 5.5V
Note 2: The effect of the internal filter (RC Network) is not considered.

Figure 1: Discharge time t_{dsc} or Protection Time

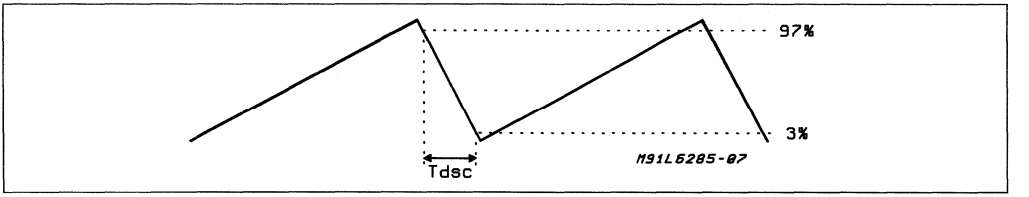
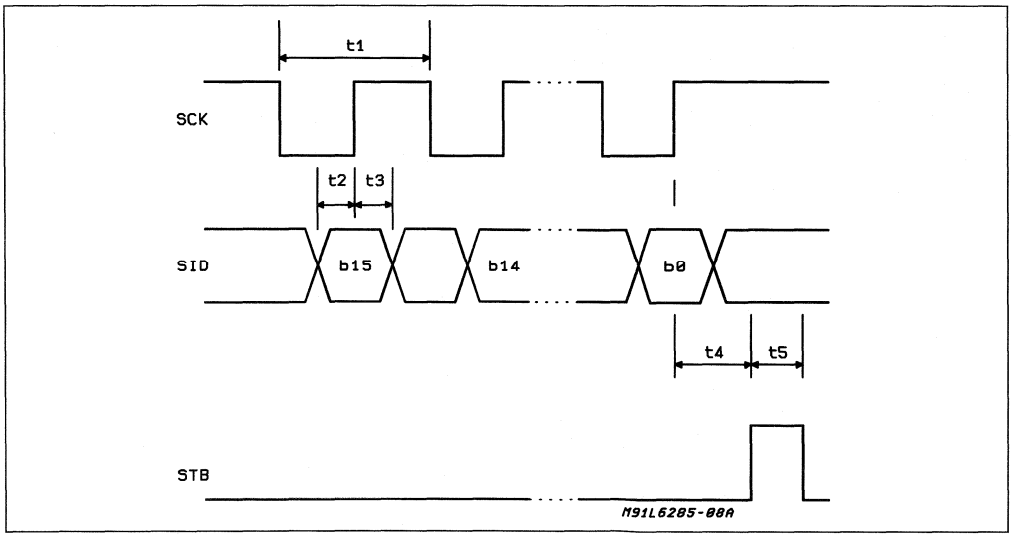


Figure 2: Interface Timing (Serial loading Mode)



BLOCK DIAGRAM DESCRIPTION

(see Block Diagram)

Inside the I.C. there are two unipolar stepper motor drivers, one bridge driver for DC motor, 4x4 bit latch registers, one shift register. the input logic, the charge pump, and the thermal protection.

The following conditions are valid for all the 3 driver sections:

1) When the osc/res pin is tied to GND, an internal reset signal is generated which switches off all the outputs and resets the internal registers.
2) The conditions 1 is valid also during power on and power off transitions.
3) During power on and power off, the I.C. is safe for any conditions of V_S and V_P
3) If V_P is present and V_S desappears, the outputs are switched off.

Input Logic

The input CMOS logic interfaces the microprocessor logic to the 4 registers. An integrated Schmitt-trigger circuit is used to improve noise immunity at each logic input.

The data is introduced in the 16bit shift register by the SID pin. The first bit b 15 after 16 clock applied to SCK pin will be the D15 of the shift register.

On the falling edge of STB the 16 bits of the shift register are transferred to the outputs of the 4 latch registers. Fig 2 shows the timing.

Registers

The Combo Motor Driver controls the 3 channels using 4 latch registers of 4 bit each:

REGISTER 1	D0	=	PHASE 1A	CHANNEL A
	D1	=	NPHASE 2A	CHANNEL A
	D2	=	PHASE 3A	CHANNEL A
	D3	=	NPHASE 4A	CHANNEL A
REGISTER 2	D0	=	PHASE 1B	CHANNEL B
	D1	=	NPHASE2B	CHANNEL B
	D2	=	PHASE 3B	CHANNEL B
	D3	=	NPHASE4B	CHANNEL B
REGISTER 3	D0	=	D/A CHANNEL A	LEAST
	D1	=	D/A CHANNEL A	MOST
	D2	=	D/A CHANNEL B	LEAST
	D3	=	D/A CHANNEL B	MOST
REGISTER 4	D0	=	INPUT 1	CHANNEL C
	D1	=	INPUT 2	CHANNEL C
	D2	=	V2 VOLTAGE	CHANNEL C
	D3	=	V2 VOLTAGE	CHANNEL C

Register 1/2 Output Status (CHA and CHB) . See note 1

D0	D1	D2	D3	OUT1 A/B	OUT2 A/B	OUT3 A/B	OUT4 A/B
0	0	0	0	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF
1	0	1	0	ON	OFF	ON	OFF
0	0	1	0	OFF	OFF	ON	OFF
0	1	1	0	OFF	ON	ON	OFF
0	1	0	0	OFF	ON	OFF	OFF
0	1	0	1	OFF	ON	OFF	ON
0	0	0	1	OFF	OFF	OFF	ON
1	0	0	1	ON	OFF	OFF	ON
ALL THE OTHERS				OFF	OFF	OFF	OFF

Register 3 Current Reference (D/A OUTPUT)

DO	D1	REFER. VOLTAGE CHANNEL A
0	0	0.125 V
0	1	0.250 V
1	0	0.375 V
1	1	0.500 V

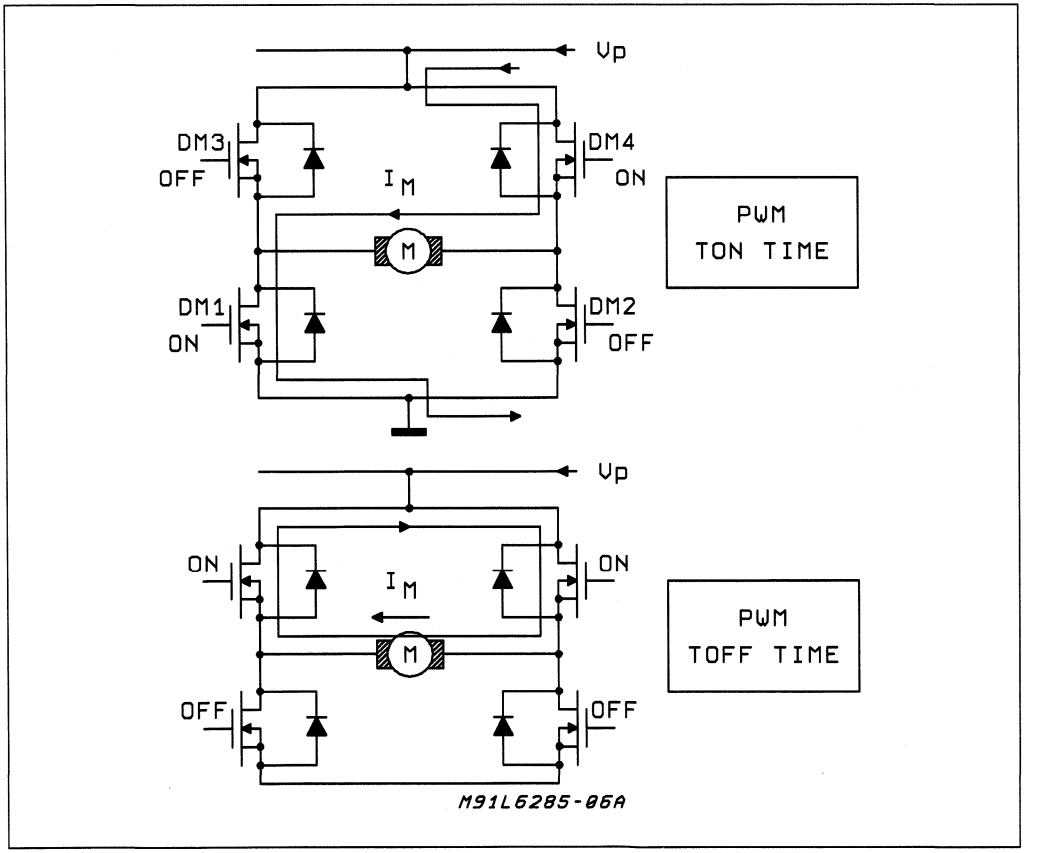
D2	D3	REFER. VOLTAGE CHANNEL B
0	0	0.125 V
0	1	0.250 V
1	0	0.375 V
1	1	0.500 V

REGISTER 4 (CHC). See note 2

D0	D1	D2	D3	OUT1 C	OUT2 C
X	X	0	0	OFF	OFF
0	0	1	1	OFF	OFF
1	0	1	1	V_P	GND
0	1	1	1	GND	V_P
1	1	1	1	GND	GND
1	0	1	0	V_P	CHOPPING; V2 LOW LEVEL
0	1	1	0	CHOPPING; V2 LOW LEVEL	V_P
1	0	0	1	V_P	CHOPPING; V2 HIGH LEVEL
0	1	0	1	CHOPPING; V2 HIGH LEVEL	V_P
0	0	1	0	OFF	OFF
1	1	1	0	V_P	V_P
0	0	0	1	OFF	OFF
1	1	0	1	V_P	V_P

Note 1: Low side DMOS status (DM1/2 in Fig. 4)
Note 2: Bridge status (see Fig. 3): OFF = tristate; V_P =, DM3/4ON; GND = DM1/2 ON

Figure 3: CHC Chopping Characteristics

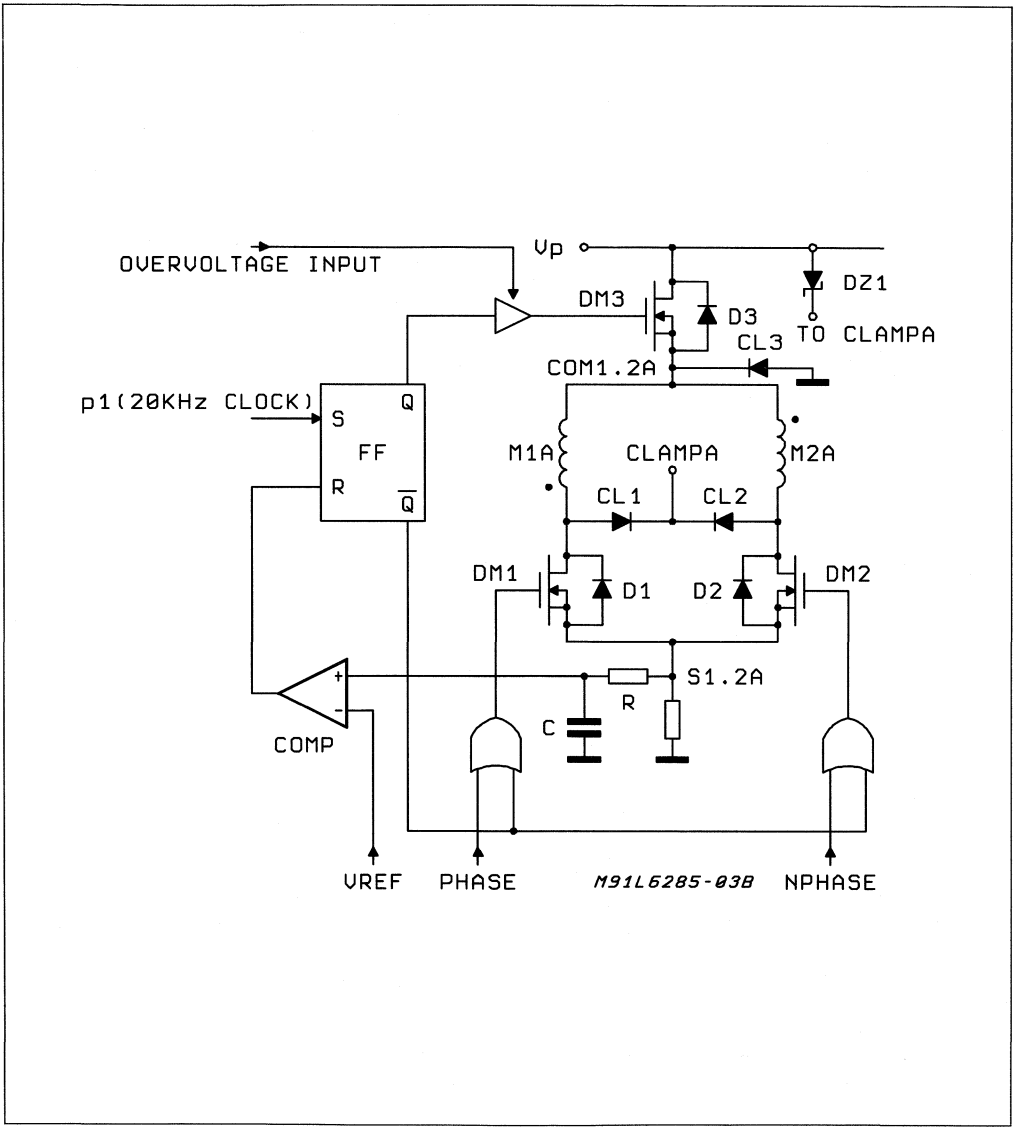


CHA and CHB Stepper Motor Drivers

These two channels drive two unipolar stepper motors in chopping mode. The basic channel configuration is shown in Fig 4. by considering well known the PWM Current Control Loop behaviour here below only particular trick are underlined. During DM3 off period the low side DMOS DM1 and DM2 are switched on to reduce the power dissipation.

The drain overvoltages generated because of the stray inductance of the motor windings are limited by connecting the DZ1 external zener diode to the clamp pin.. The diodes CL1 and CL2 are integrated as far as the CL3 diode which limits the negative voltage at pin COM1.2. An internal RC network (1µs) is realized to filter the sensing resistor signal.

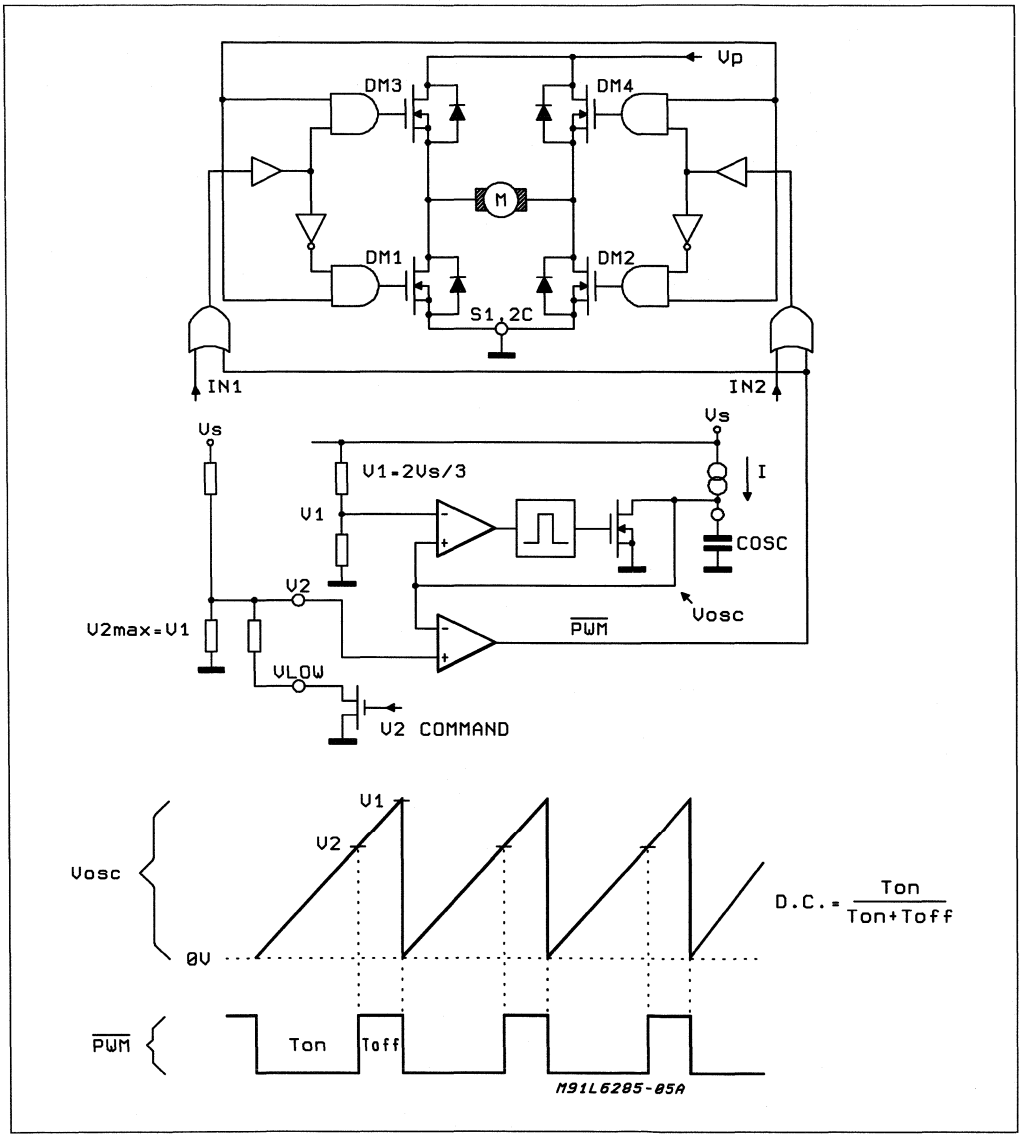
Figure.4: Unipolar motor driver CHA (or CHB)



CHC DC Motor Driver

The DC motor driver is a DMOS full bridge with a PWM Open Loop Voltage Control. Fig.5 shows the theory of operation. The C_{osc} Capacitor is charged by a constant current source. The oscillating voltage value is from 0V to the V1 level internally fixed at V1 = 2/3 V_S. The output duty cycle is controlled by the V2 voltage. The operational range of V2 is from 200mV to V1. Fig.3 shows the DMOS status during PWM: t_{ON} and t_{OFF} bridge configurations. While the PWM Duty Cycle defines the motor speed (not controlled since the loop is open),the logic level of IN1 and IN2 can choose the direction of the motor.

Figure.5: DC Motor Driver CHC



Oscillator For Clock and Reset Generation

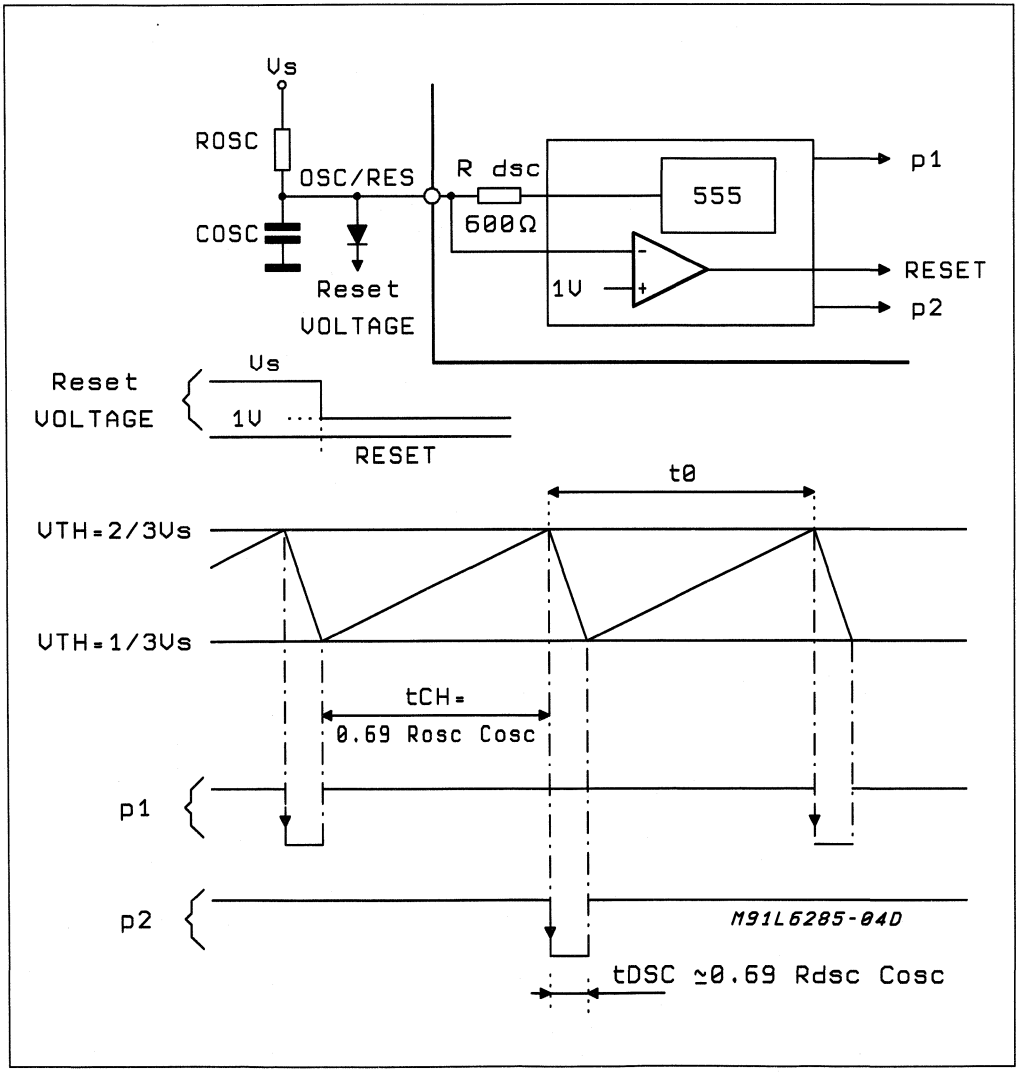
The oscillator block provides for two functions:

1) Generate an internal reset signal when the voltage at pin osc/res is below 1V. The reset signal switches off all the outputs and resets the logic registers.
2) Generate, when the pin osc/res is left free two syncro signals p1 and p2 for the clock of the PWM Current Control of the two stepper driver blocks

The oscillator operates like the 555 concept in which the capacitor voltage oscillates between $1/3V_S$ $2/3V_S$ (Fig. 6). The oscillator frequency is 2 times the chopping frequency in order to generate the two syncro signals at operative 20KHz PWM. The t_{CH} = charge time of Cosc is defined by R_{osc}, V_{TH1} and V_{TH2} (threshold voltages)and C_{osc}.

The discharge time T_{dsc} is practically only defined by Cosc and the internal discarge resistor Rdsc. The t_{dsc} is also the time lockout during which the RS FF cannot read the Comparator output (see Fig. 4)

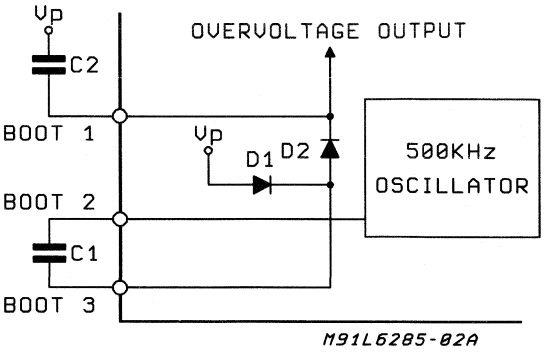
Figure 6: Oscillator Concept



Charge Pump

The charge pump circuitry generates the overvoltage needed to drive the gate of the high side output DMOS power transistors.It is realized by using two external capacitors (C1 and C2) and two integrated diodes that operate as a full wave rectifier (see Fig. 7). The oscillator peak to peak output voltage is stored by C2 and summed to the Power Supply Voltage V_p..
The voltage present at the pin BOOT1, is then the overvoltage needed to supply the gate of the high side DMOS drivers.

Figure 7: Charge Pump Circuit



THERMAL PROTECTION

The thermal protection shuts down the chip before it can reach a dangerous temperature.
Additional informations to the microprocessor are available at the A0TH, A1TH pins.

A0TH	A1TH	THERMAL PROTECTION	CIRCUIT STATUS
0	0	OK	OPERATING
1	0	PREALARM	OPERATING
1	1	ALARM	THERMAL SHUTDOWN
0	1	NOT POSSIBLE	

APPLICATION INFORMATION

A typical application circuit is shown in Fig.8. By this application it is possible to drive two unipolar stepper motors (M1,M2) and one DC motor (M3). As it can be seen, only two external Zener diodes (D1,D2) are needed to clamp the voltage transients generated by the stray inductance of the motor windings. This is recommended when the peak current is not more than three to four hundred mAmps. For a power supply voltage of V_P=24V ±10%, D1=D2 must be 30V ±5%-1W (1N4751A or equivalent). Both the V_P and the V_S pins need bypass capacitors (C1,C2,C3); to supply the high-side DMOS (Source Transistors) at pin.15 ,only two external capacitors (C4,C5) complete the charge pump circuitry. The oscillator frequency, that is twice the chopping frequency for M1 and M2, is mainly defined by the network R6C6:

$f_{osc} = [0.69 (R_{ch} + Rd_{sc}) C_{osc}]^{-1}$, where

R_{ch} = R6 ; R_{dsc} = 600 ohm typ.

At the same time, the lockout duration (or protection window) needed for a correct chopping behavior, is given by :

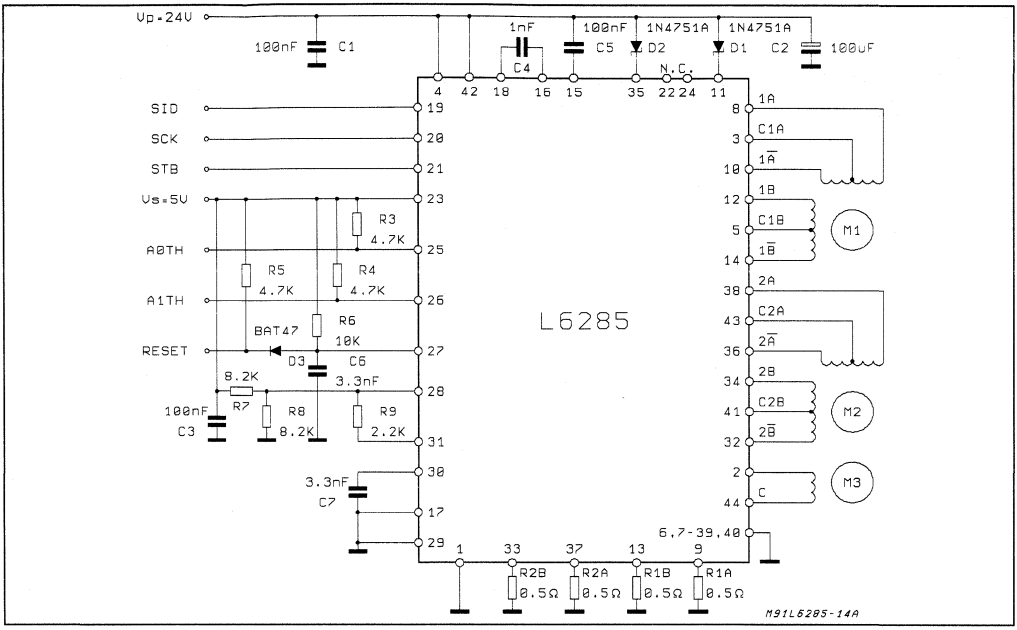
$T_{lockout} = 0.69 R_{dsc} C_{osc}$

The shown values (fig.8) give a nominal frequency a little bit more than 41KHz and a protection window of 1.4 µs roughly. The Schottky diode D3 and the pull-up resistor R5 driven via an open-collector transistor can generate the Reset function. The chopping current is sensed across R1 A/B; R2 A/B that must be of a not inductive type. The DC motor PWM Open Loop Voltage Control operates at a frequency defined by C7, charged with a typical constant current source (I = 240 µA), up to V1 = 0.67 V_S. Since the discharge time is very short, it can be written :

$f_{osc} = I / C_{osc} V1$, where C_{osc} = C7.

Tha values indicated in figure give a typical frequency of about 22 KHz.

Figure 8: Typical Application Circuit



The duty cycle DC can be chosen between two possibilities (High and Low) than can be defined externally by the resistors R7, R8 and R9: Fig.5 let well understand how to calculate the dividers that fix V2 H (wider t_{on}) and V2 L (wider t_{off}). It may be needed to drive stepper motors that require a higher peak current than told above. In this case each motor phase requires a particular application arrangement (see Fig.9b). In Fig.9a all the protection components are integrated with the exception of Z1. In Fig.9b the clamp of the voltage spikes generated by the stray inductance Ls is achieved using Transil protection T1 and T2 that works also as additional diodes during current recirculation at the phase change. The diode D1, externally connected, is recommended at the highest working current levels and/or when the supplied voltage (plus Back EMF) at the end of the motor winding is too much unbalanced.

Figure 9a: Output Configuration as it is obtained by the Application Circuit

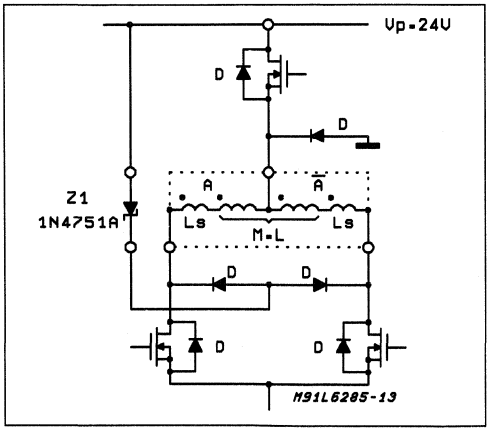
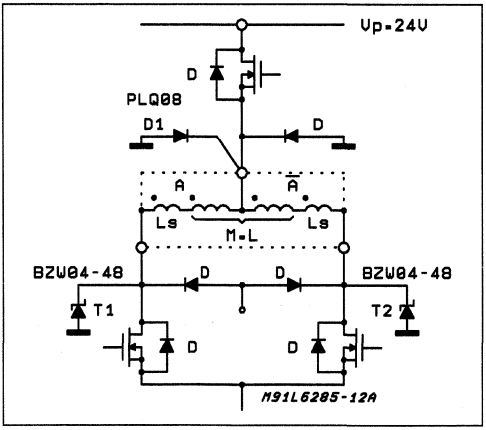


Figure 9b: Output Configuration at Higher Operating Currents



THERMAL CHARACTERISTICS

The cooling of the device is obtained by soldering its ground pins on a proper p.c.b copper side , acting as a true heatsink. By considering four squared side as in Fig.10, the junction to ambient thermal resistance has been measured (see Fig.11). The typical transient thermal resistance versus values of single pulse width of power is shown in Fig.12. In general these thermal characteristics are very important to the designer to optimize the L6285 applications.

Figure 10: Four "on board" Square Heatsink

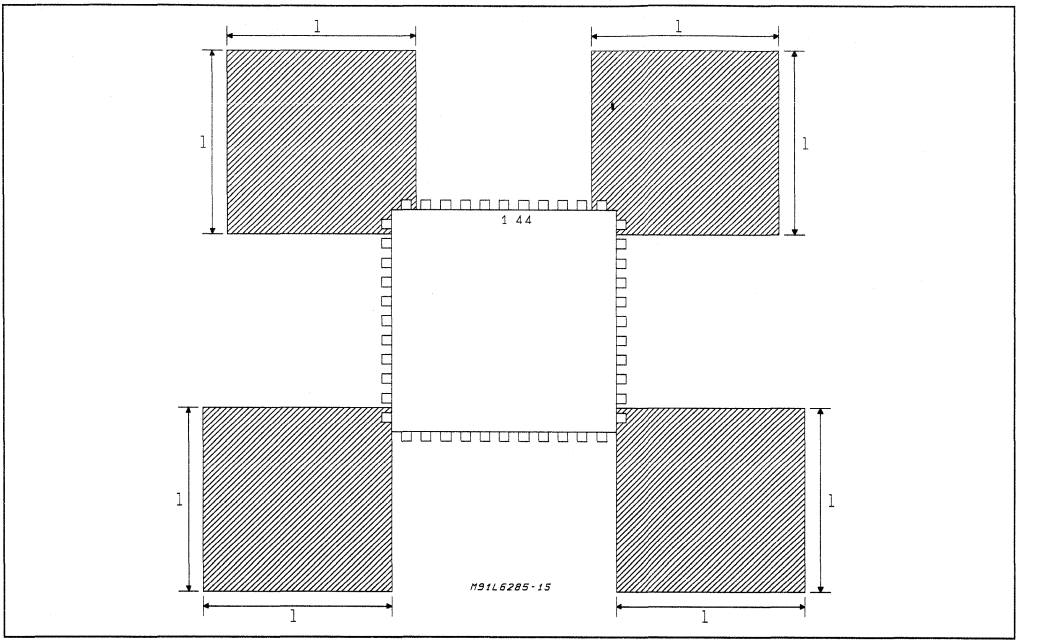


Figure 11: Typical $R_{th\ j\text{-}amb}$ vs. lenght "l" (Fig. 10)

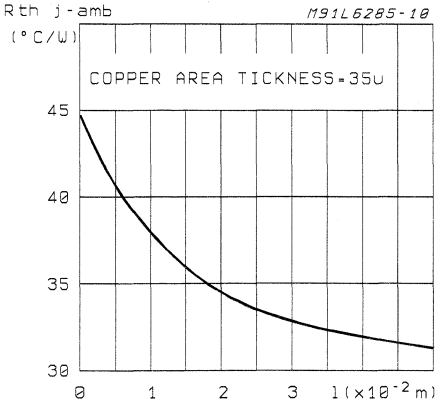
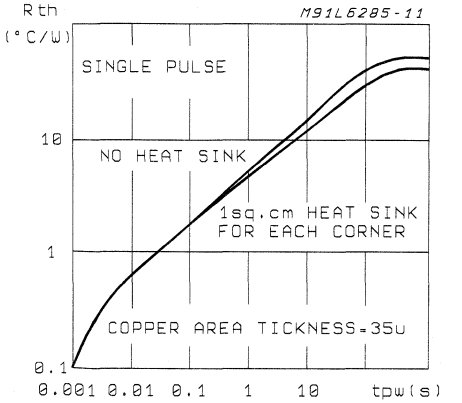


Figure 12: Typical Transient Thermal Resistance vs. Time or Pulse Width



SGS-THOMSON MICROELECTRONICS

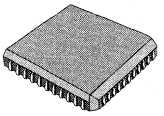
L6286

3 CHANNELS MULTIPOWER SYSTEM

ADVANCE DATA

- CHANNEL-A AND CHANNEL-B FOR UNIPOLAR STEPPER MOTORS
  - LOW SIDE: R_{DSON} = 1.2Ω
  - HIGH SIDE ; R_{DSON} = 1.2Ω
- CHANNEL-C FOR DC MOTORS
  - LOW SIDE: R_{DSON} = 1.7Ω
  - HIGH SIDE: R_{DSON} = 1.2Ω
- CHOPPING MODE DRIVING FOR C.L. CURRENT CONTROL ON CHA AND CHB AND O.L. VOLTAGE CONTROL ON CHC.
- INTERNAL FOUR DRIVING LATCHES
- 16 BIT INTERNAL SHIFT REGISTER
- DIRECT INTERFACE TO µP
- PARALLEL DRIVING SEQUENCE LOADING
- CMOS COMPATIBLE INPUTS
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



PLCC44

ORDERING NUMBER: L6286

DESCRIPTION

This Combo Motor Driver uses large scale integration to incorporate several functions into the same chip.

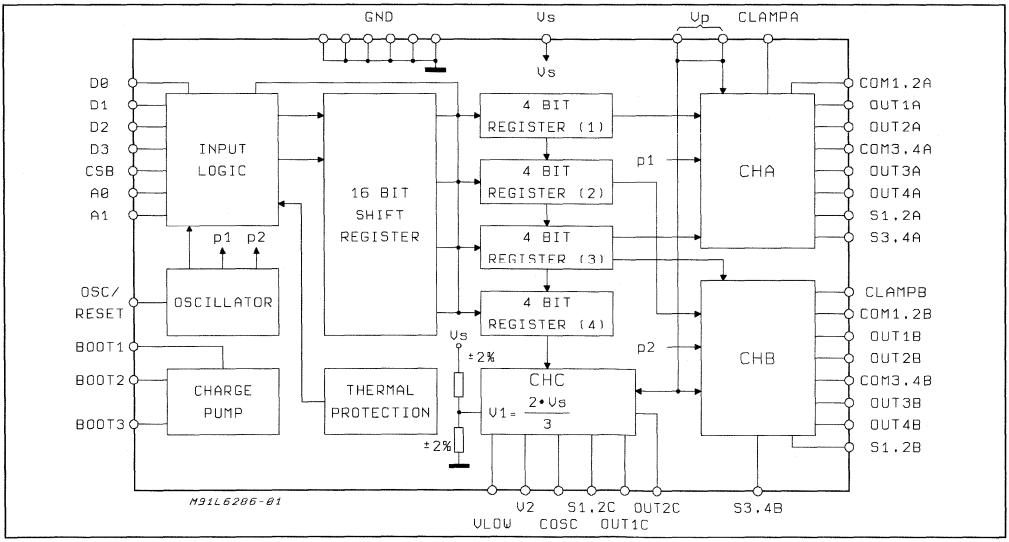
1) Two unipolar stepper motor driver
2) A full bridge DC motor driver
3) Parallel microprocesor interface

The power output stages are DMOS and the input can be interfaced to a CMOS Microprocessor logic.

The phase current in the unipolar stepper motor windings is controlled by two external sensing resistors in fixed frequency chopping mode. The oscillator block provides clocks each other 180° out of phase to the two stepper motor driver in order to avoid symultaneous current peaks.

For the DC motor driver is used a bridge; the RMS voltage to supply this motor is fixed by a simple PWM open loop. The 3 motors are control-

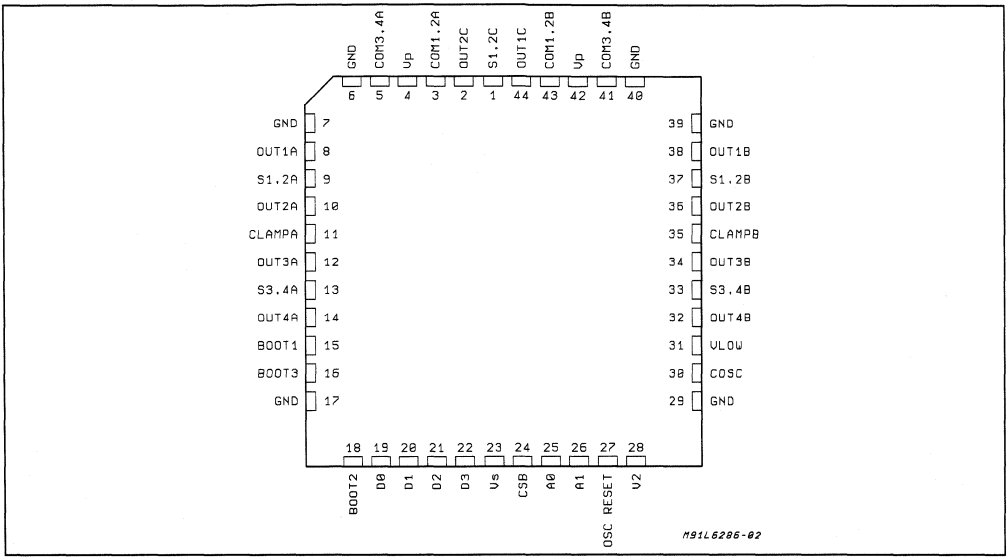
BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

led by the micro through 4 latches of 4 bit each. The loading of these registers is in serial mode. The I.C. operates at 5V supply for the logic and at 24V supply for the power stages. The package is the PLCC44 with 6 pins devoted to ground and to sink out the heat produced by power dissipation.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_P	Power Supply Voltage	30	V
V_S	Logic Supply Voltage	7	V
V_{in}	Logic Input Voltage	-0.3 to V_S + 0.3	V
I_{LOW}	Low Side DMOS max DC Current	1	A
I_{HIGH}	High Side DMOS max DC Current	1	A
I_{pLOW}	Low Side DMOS max Peak Current (1µs On; 50µs OFF)	2	A
I_{pHIGH}	High Side DMOS max Peak Current (1µs On; 50µs OFF)	2	A
V_{bout}	Max Output Voltage of Stepper Motor Driver (transient rcirculation)	60	V
V_{sense} 1;2	Max Voltage ON Vsense (CHA/CHB)	-1 to 2	V
V_{sense} 3	Max Voltage ON V_{sense} (CHC)	-1 to 2	V
I_{fdDC}	Max DC Current of Forward Diode (DMOS Source Drain Diode)	1	A
I_{fdpk}	Max Peak Current of Forward Diode (DMOS Source Drain Diode) (1µs On; 50µs OFF)	2	A
P_{tot}	Total Power Dissipation (Tpins = 90°C) With minimized dissipating copper area (T_{amb} = 70°C)	5 1.6	W W
T_{op}	Operating Temperature Range	0 to 150	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	50	°C/W

PIN DESCRIPTION

Pins	Name	Functions
1	S1,2C	Full bridge common source output to separate between power GND and logic GND.
2,44	OUT 1C, OUT 2C	Output of the channel C bridge.
3	COM 1,2A	High side DMOS channel A for current chopping in the windings connected pins to OUT 1A, OUT 2A.
4,42	V_p	Power Supply Voltage.
5	COM 3,4A	High side DMOS channel A for current chopping in the windings connected to pins OUT 3A, OUT 4A.
6,7,39,40	GND	PowerGround and heatsink pins.
8,10 12,14	OUT 1A, OUT 2A OUT 3A, OUT 4A	Low side DMOS outputs of channel A stepper motor driver.
9	S1,2A	Channel A sources of the DMOS OUT 1A, OUT 2A. A sensing resistor has to be connected from this pin and ground, for current control of phase 1,2 A.
11,35	CLAMP A, CLAMP B	These pins have to be connected to an external zener diode to clamp the output voltage spikes of channel A/B.
13	S3,4A	Channel A sources of the DMOS OUT 3A, OUT 4A. A sensing resistor has to be connected from this pin and ground, for current control of phase 3,4 A.
15	BOOT 1	A capacitor between this pin and V_p stores the overvoltage for each high side DMOS driver gate.
16	BOOT 3	A capacitor between this pin and internal diodes allows the change pump to transfer energy to the capacitor at the pin BOOT 1.
17,29	GND	Logic Ground and Heatsink pins.
18	BOOT 2	Charge pump oscillator output.
19	D0	Parallel D0 data input.
20	D1	Parallel D1 data input.
21	D2	Parallel D2 data input.
22	D3	Parallel D3 data input.
23	V_s	Logic Supply Voltage.
24	CSB	A logical low level to this pin loads the four parallel inputs D0 to D3 into the register selected by A0, A1.
25	A0	Together A1 it selects an internal register.
26	A1	Together A0 it selects an internal register.
27	OSC/ RESET	An RC network connected to this pin defines the oscillator frequency for stepper drivers. When OSC/RES is <1V, a reset signal is internally generated.
28	V2	A voltage to this pin defines the output duty cycle of Channel C.
30	C_{osc}	A capacitor connected to this pin defines the chopping frequency of channel C.
31	V_{low}	This pin is low when the chopping low voltage (V2 low level) is selected; it is in high impedance when the chopping high voltage (V2 high level) is selected. Only for CHC operation.
32,34 36,38	OUT4B, OUT3B OUT2B ,OUT1B	Low side DMOS outputs of channel B stepper motor driver.
33	S 3, 4B	Same as S 3, 4A, but for channel B.
37	S 1, 2B	Same as S 1, 2A, but for channel B.
41	COM 3, 4B	Same as COM 3, 4A, but for channel B.
43	COM 1, 2B	Same as COM 1, 2A, but for channel B.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_s = 5V, V_p = 24V unless othewise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_p	Power Supply Voltage		9		26.5	V
I_p	Quiescent Power Supply Current	(note 1)			7	mA
V_s	Logic Supply Voltage		4.5		5.5	V
I_s	Quiescent Logic Supply Current	(note 1)			20	mA

LOGIC LEVEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{inL}	Input Low Voltage		-0.3		1.35	V
V_{inH}	Input High Voltage		3.15		VS+0.3	V
I_{inL}	Input Low Current	$V_{in} = V_{inL}$	-10			µA
I_{inH}	Input High Current	$V_{in} = V_{inH}$			10	µA

CHANNEL A AND CHANNEL B (UNIPOLAR MOTORS)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSONL}	Low Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
R_{DSONH}	High Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
I_{DSSL}	Low Side DMOS Leakage Current	V_{DS} = 60V; output OFF			2	mA
I_{DSSH}	High Side DMOS Leakage Current	V_p= 30V; V_O= 0V	-1.5			mA
V_{REF}	Voltage reference to the Comparator	LEVEL 1 LEVEL 2 LEVEL 3 LEVEL 4	100 220 340 465	125 250 375 500	150 280 410 535	mV mV mV mV
T_d	Turn OFF Delay on HIGH Side DMOS after the Sensing Current Reach the Threshold Value	(note 2)			1	µs
f_{max}	Max Chopping Frequency				40	KHz

CHANNEL C (DC MOTORS) (see Fig. 5)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{osc}	Oscillator Frequency	Cosc = 3.3nF; V1 = 2/3Vs	17	22	28	KHz
DC	Duty Cycle	V2 = 1/2V_S	72	75	81	%
I_{b2}	Comparator Input Bias	V2 = 200mV	-1			µA
V_{low}	Open Drain Output	I = 5mA		0.2	0.4	V
R_{DSONH}	High Side DMOS ON Res.	I_{DS} = 0.7A			1.2	Ω
R_{DSONL}	Low Side DMOS ON Res.	I_{DS} = 0.7A			1.7	Ω
I_{LH}	HSD MOS Leakage Current	V_P = 30V; V_O = 0V	-1			mA
I_{LL}	LSD MOS Leakage Current	V_O = 30V; V_{sense} = 0V	-1.5			mA
V_{fddc}	Forward Diode DC Voltage (DMOS Diode)	I_{fdcc} = 0.7A		1.4	2	V
f_{max}	Max Chopping Frequency				40	KHz
V_{boot}	Voltage on pin Boot1		V_p +7			V
$I_{L\ boot}$	Leakage Current on pin Boot1	$V_{bott} = V_p$ +12V; V_p = 26.5V			200	µA

ELECTRICAL CHARACTERISTICS (continued)

OSCILLATOR (see Fig. 6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{osc}	Oscillator Frequency Pin OSC/RESET	COSC = 3.3nF; R_{OSC} = 10KΩ	27	41	46	KHz
T_{dsc}	Capacitor Discharge Time (protect dead time)	C_{OSC} = 3.3nF; R_{OSC} = 10KΩ (see Fig. 1)	0.8	1.4	2	µs
V_{reset}	Reset Threshold Voltage		1			V

Note 1: No output loaded; all register to low condition; no reset applied; V_P = 26.5V; V_S = 5.5V
Note 2: The effect of the internal filter (RC network) is not considered.

Figure 1: Discharge time t_{dsc} or Protection Time

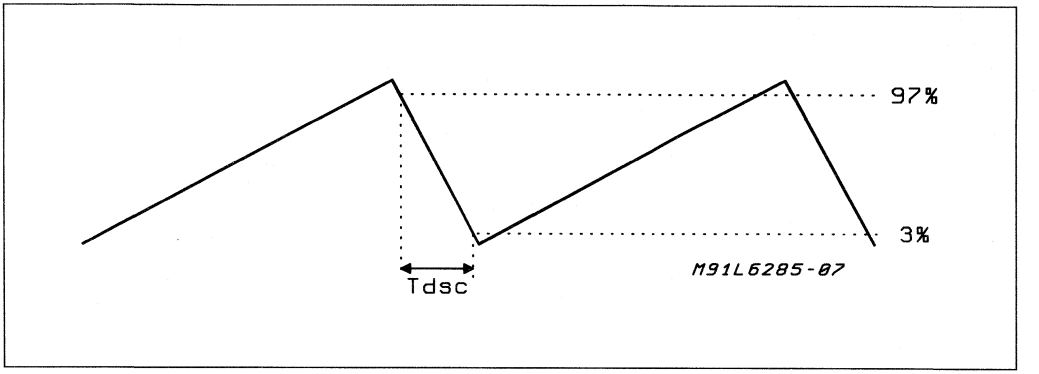
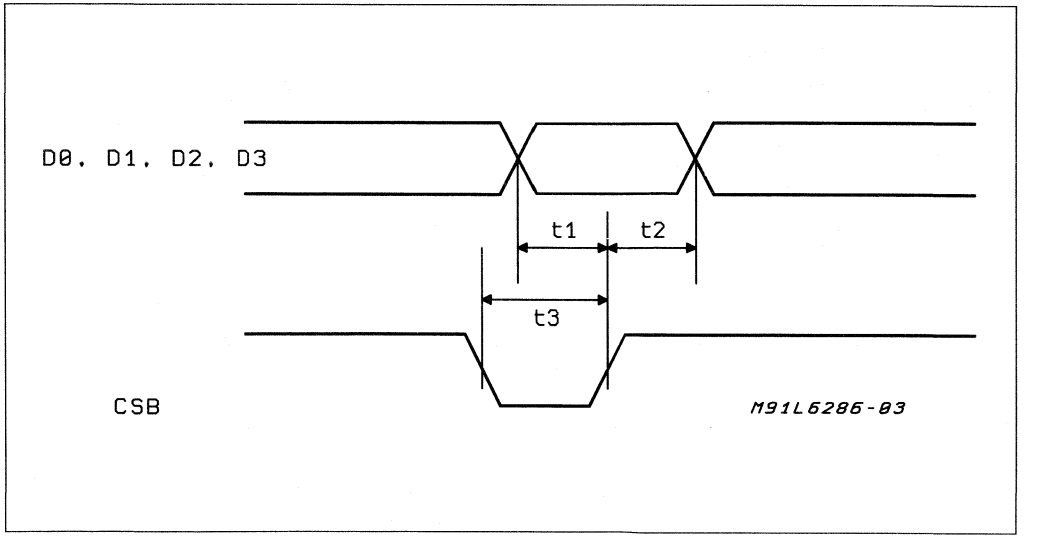


Figure 2: Interface Timing (Parallel Loading Mode)



BLOCK DIAGRAM DESCRIPTION

(see Block Diagram)

Inside the I.C. there are two unipolar stepper motor drivers, one bridge driver for DC motor, 4x4 bit latch registers, one shift register. the input logic, the charge pump, and the thermal protection.

The following conditions are valid for all the 3 driver sections:

1) When the osc/res pin is tied to GND, an internal reset signal is generated which switches off all the outputs and resets the internal registers.
2) The conditions 1 is valid also during power on and power off transitions.
3) During power on and power off, the I.C. is safe for any conditions of V_S and V_p
3) If V_p is present and V_S desappears, the outputs are switched off.

Input Logic

The input CMOS logic interfaces the microprocessor logic to the 4 registers. An integrated Schmitt-trigger circuit is used to improve noise immunity at each logic input.

The address inputs A0; A1 select the 4 latch registers for loading according to Table 1. The rising edge of the CSB signal transfers the bits D0 to D3 to the outputs of the selected latch-register. Fig. 2 shows the timing.

Table 1

A0	A1	Register
0	0	1
1	0	2
0	1	3
1	1	4

Registers

The Combo Motor Driver controls the 3 channels using 4 latch registers of 4 bit each:

REGISTER 1	D0	=	PHASE 1A	CHANNEL A
	D1	=	NPHASE 2A	CHANNEL A
	D2	=	PHASE 3A	CHANNEL A
	D3	=	NPHASE 4A	CHANNEL A
REGISTER 2	D0	=	PHASE 1B	CHANNEL B
	D1	=	NPHASE2B	CHANNEL B
	D2	=	PHASE 3B	CHANNEL B
	D3	=	NPHASE4B	CHANNEL B
REGISTER 3	D0	=	D/A CHANNEL A	LEAST
	D1	=	D/A CHANNEL A	MOST
	D2	=	D/A CHANNEL B	LEAST
	D3	=	D/A CHANNEL B	MOST
REGISTER 4	D0	=	INPUT 1	CHANNEL C
	D1	=	INPUT 2	CHANNEL C
	D2	=	V2 VOLTAGE	CHANNEL C
	D3	=	V2 VOLTAGE	CHANNEL C

Register 1/2 Output Status (CHA and CHB) . See note 1

D0	D1	D2	D3	OUT1 A/B	OUT2 A/B	OUT3 A/B	OUT4 A/B
0	0	0	0	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF
1	0	1	0	ON	OFF	ON	OFF
0	0	1	0	OFF	OFF	ON	OFF
0	1	1	0	OFF	ON	ON	OFF
0	1	0	0	OFF	ON	OFF	OFF
0	1	0	1	OFF	ON	OFF	ON
0	0	0	1	OFF	OFF	OFF	ON
1	0	0	1	ON	OFF	OFF	ON
ALL THE OTHERS				OFF	OFF	OFF	OFF

Register 3 Current Reference (D/A OUTPUT)

DO	D1	REFER. VOLTAGE CHANNEL A
0	0	0.125 V
0	1	0.250 V
1	0	0.375 V
1	1	0.500 V

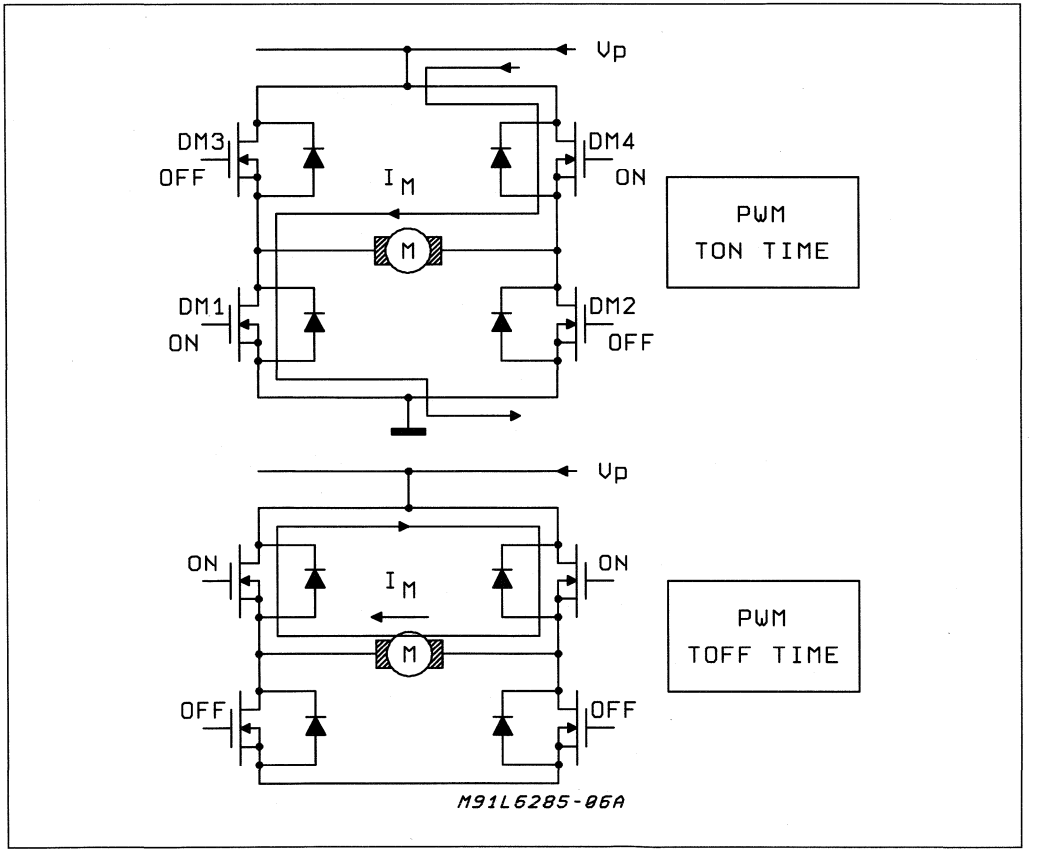
D2	D3	REFER. VOLTAGE CHANNEL B
0	0	0.125 V
0	1	0.250 V
1	0	0.375 V
1	1	0.500 V

REGISTER 4 (CHC). See note 2

D0	D1	D2	D3	OUT1 C	OUT2 C
X	X	0	0	OFF	OFF
0	0	1	1	OFF	OFF
1	0	1	1	V_P	GND
0	1	1	1	GND	V_P
1	1	1	1	GND	GND
1	0	1	0	V_P	CHOPPING; V2 LOW LEVEL
0	1	1	0	CHOPPING; V2 LOW LEVEL	V_P
1	0	0	1	V_P	CHOPPING; V2 HIGH LEVEL
0	1	0	1	CHOPPING; V2 HIGH LEVEL	V_P
0	0	1	0	OFF	OFF
1	1	1	0	V_P	V_P
0	0	0	1	OFF	OFF
1	1	0	1	V_P	V_P

Note 1: Low side DMOS status (DM1/2 in Fig. 4)
Note 2: Bridge status (see Fig. 3): OFF = tristate; V_P =, DM3/4ON; GND = DM1/2 ON

Figure 3: CHC Chopping Characteristics

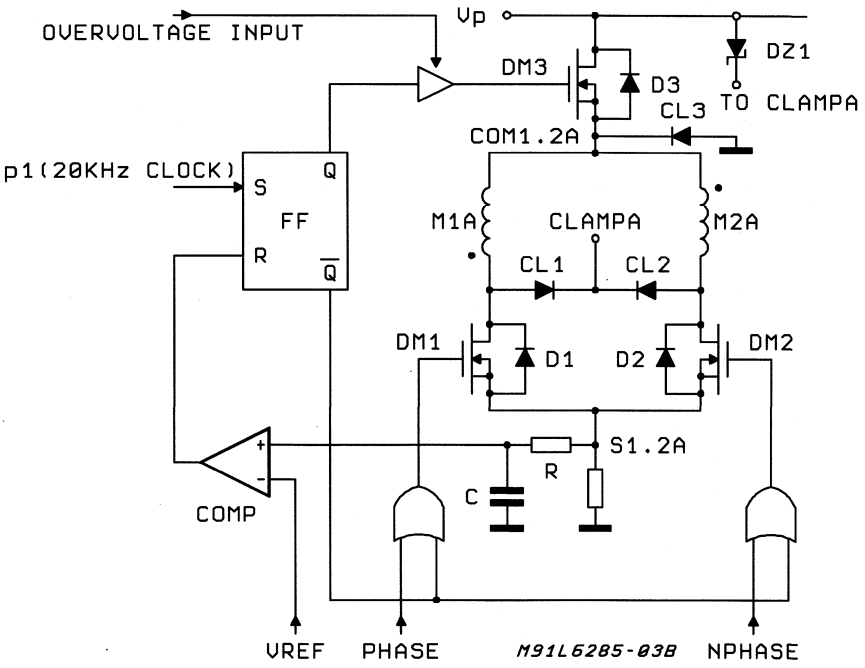


CHA and CHB Stepper Motor Drivers

These two channels drive two unipolar stepper motors in chopping mode. The basic channel configuration is shown in Fig 4. by considering well known the PWM Current Control Loop behaviour here below only particular trick are underlined. During DM3 off period the low side DMOS DM1 and DM2 are switched on to reduce the power dissipation.

The drain overvoltages generated because of the stray inductance of the motor windings are limited by connecting the DZ1 external zener diode to the clamp pin.. The diodes CL1 and CL2 are integrated as far as the CL3 diode which limits the negative voltage at pin COM1.2. An internal RC network (1µs) is realized to filter the sensing resistor signal.

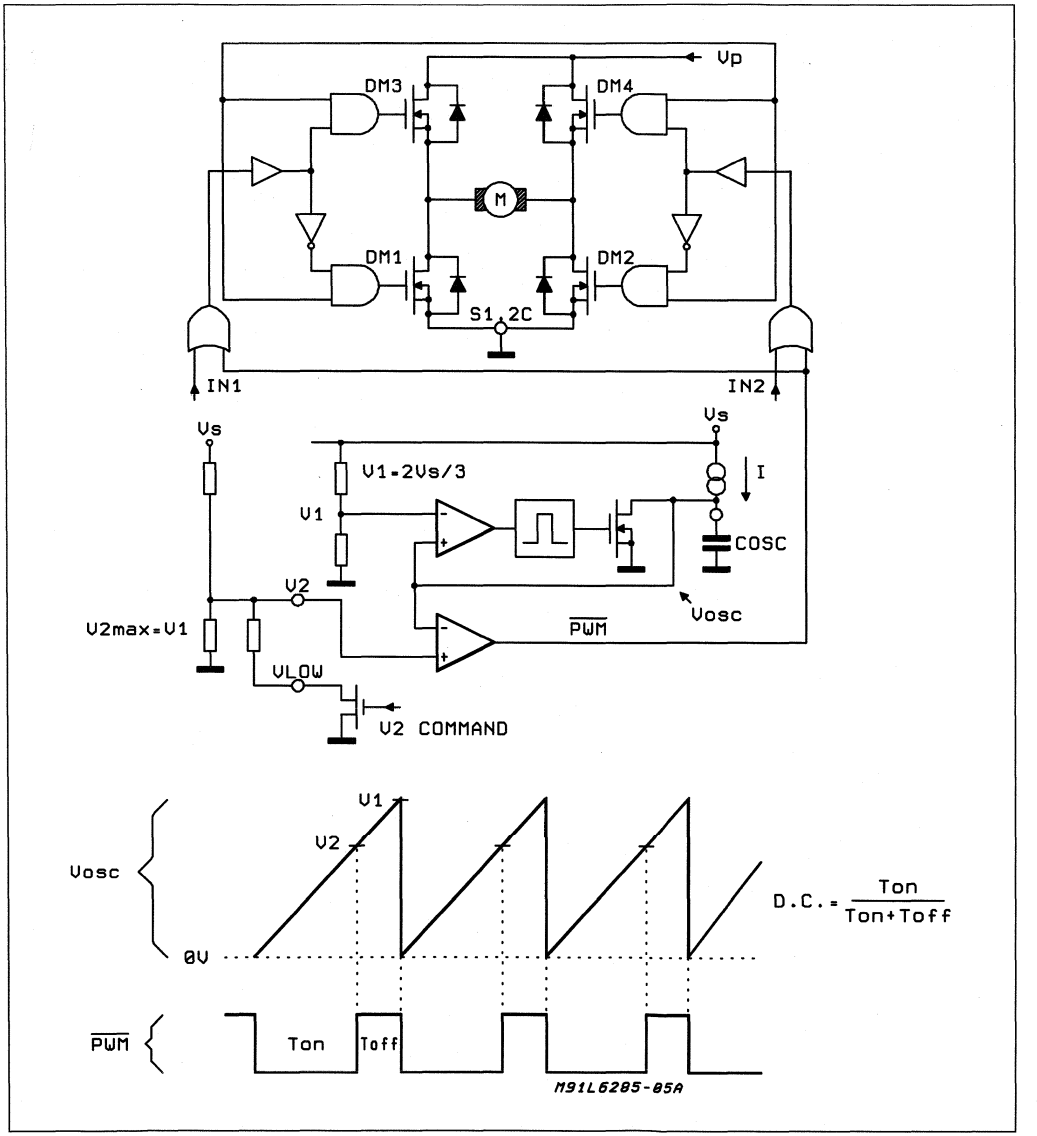
Figure.4: Unipolar motor driver CHA (or CHB)



CHC DC Motor Driver

The DC motor driver is a DMOS full bridge with a PWM Open Loop Voltage Control. Fig.5 shows the theory of operation. The C_{osc} Capacitor is charged by a constant current source. The oscillating voltage value is from 0V to the V1 level internally fixed at V1 = 2/3 Vs. The output duty cycle is controlled by the V2 voltage. The operational range of V2 is from 200mV to V1. Fig.3 shows the DMOS status during PWM: t_{ON} and t_{OFF} bridge configurations. While the PWM Duty Cycle defines the motor speed (not controlled since the loop is open),the logic level of IN1 and IN2 can choose the direction of the motor.

Figure.5: DC Motor Driver CHC



Oscillator For Clock and Reset Generation

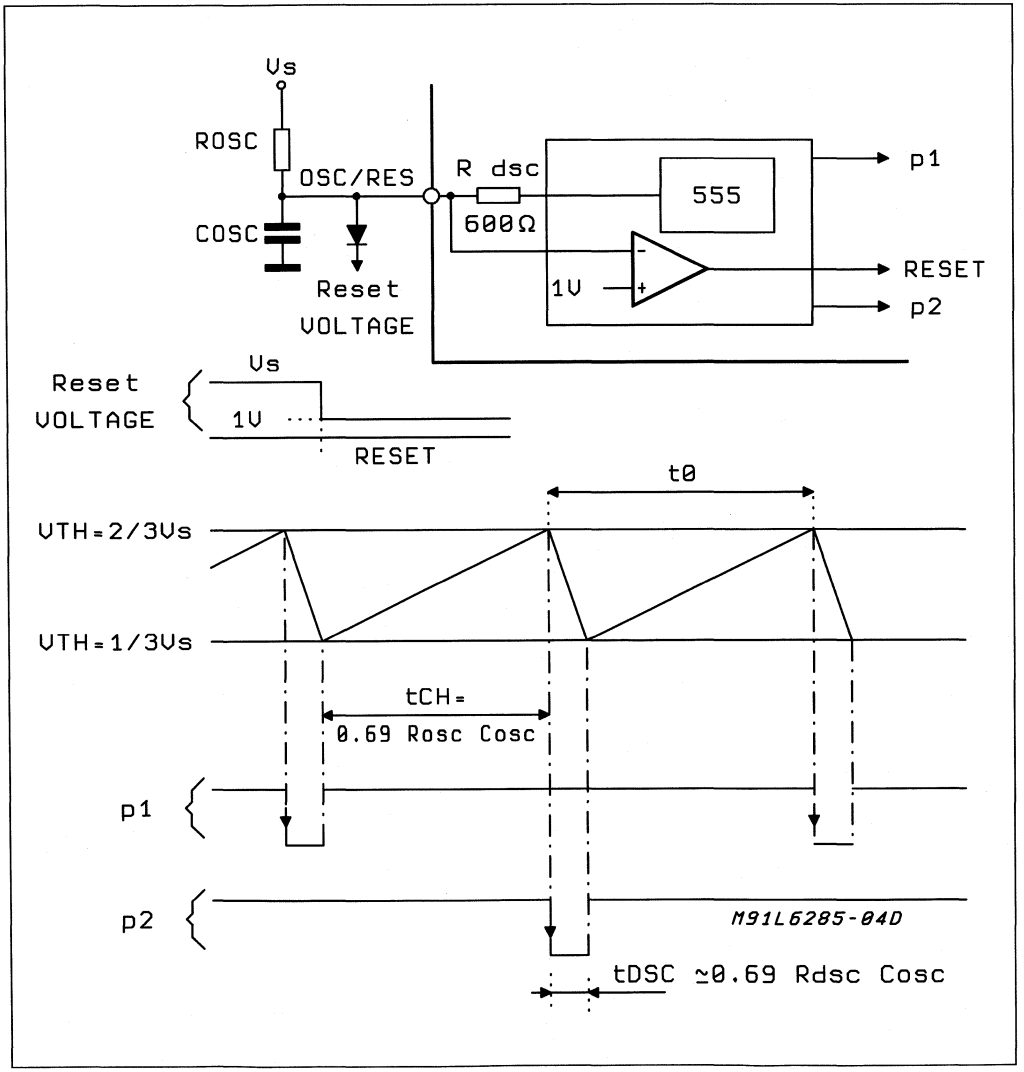
The oscillator block provides for two functions:

1) Generate an internal reset signal when the voltage at pin osc/res is below 1V. The reset signal switches off all the outputs and resets the logic registers.
2) Generate, when the pin osc/res is left free two syncro signals p1 and p2 for the clock of the PWM Current Control of the two stepper driver blocks

The oscillator operates like the 555 concept in which the capacitor voltage oscillates between 1/3 Vs 2/3 Vs (Fig. 6). The oscillator frequency is 2 times the chopping frequency in order to generate the two syncro signals at operative 20KHz PWM. The t_{CH} = charge time of Cosc is defined by R_{osc}, V_{TH1} and V_{TH2} (threshold voltages)and C_{osc}.

The discharge time T_{dsc} is practically only defined by Cosc and the internal discarge resistor Rdsc. The t_{dsc} is also the time lockout during which the RS FF cannot read the Comparator output (see Fig. 4)

Figure 6: Oscillator Concept



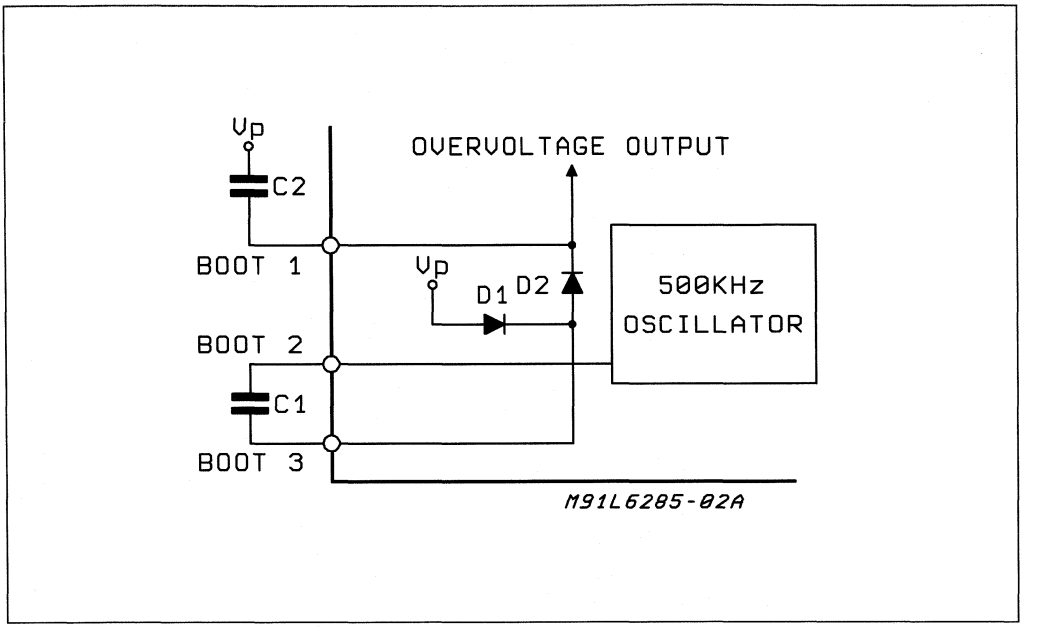
Charge Pump

The charge pump circuitry generates the overvoltage needed to drive the gate of the high side output DMOS power transistors.It is realized by using two external capacitors (C1 and C2) and two integrated diodes that operate as a full wave rectifier (see Fig. 7). The oscillator peak to peak output voltage is stored by C2 and summed to the Power Supply Voltage V_P..
The voltage present at the pin BOOT1, is then the overvoltage needed to supply the gate of the high side DMOS drivers.

THERMAL PROTECTION

The thermal protection shuts down the chip before it can reach a dangerous temperature.

Figure 7: Charge Pump Circuit



APPLICATION INFORMATION

A typical application circuit is shown in Fig.8. By this application it is possible to drive two unipolar stepper motors (M1,M2) and one DC motor (M3). As it can be seen, only two external Zener diodes (D1,D2) are needed to clamp the voltage transients generated by the stray inductance of the motor windings. This is recommended when the peak current is not more than three to four hundred mAmps. For a power supply voltage of V_P=24V ±10%, D1=D2 must be 30V ±5%-1W (1N4751A or equivalent). Both the Vp and the Vs pins need bypass capacitors (C1,C2,C3); to supply the high-side DMOS (Source Transistors) at pin.15 ,only two external capacitors (C4,C5) complete the charge pump circuitry. The oscillator frequency, that is twice the chopping frequency for M1 and M2, is mainly defined by the network R4C6:

$f_{osc} = [\ 0.69\ (R_{ch} + Rd_{sc})\ C_{osc}\ ]^{-1}$, where

R_{ch} = R4 ; R_{dsc} = 600 ohm typ.

At the same time, the lockout duration (or protection window) needed for a correct chopping behavior, is given by :

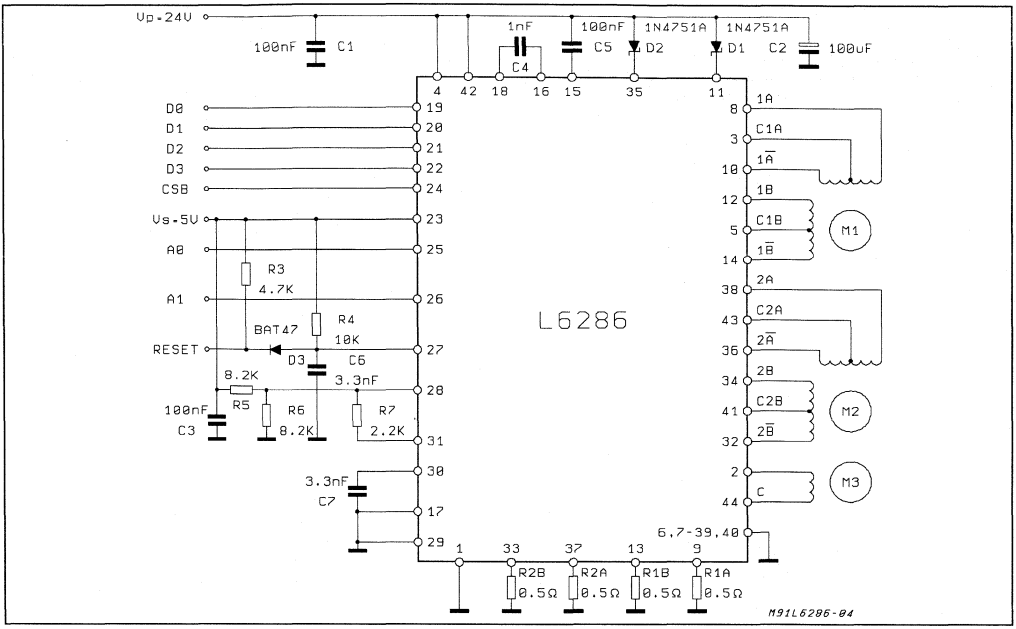
$T_{lockout} = 0.69\ R_{dsc}\ C_{osc}$

The shown values (Fig.8) give a nominal frequency a little bit more than 41 KHz and a protection window of 1.4 µs roughly. The Schottky diode D3 and the pull-up resistor R3 driven via an open-collector transistor can generate the Reset function. The chopping current is sensed across R1 A/B ; R2 A/B that must be of a not inductive type . The DC motor PWM Open Loop Voltage Control operates at a frequency defined by C7, charged with a typical constant current source (I = 240 µA), up to V1 = 0.67 Vs. Since the discharge time is very short, it can be written :

$f_{osc} = I / C_{osc}\ V1$, where C_{osc} = C7.

Tha values indicated in figure give a typical frequency of about 22 KHz.

Figure 8: Typical Application Circuit



The duty cycle DC can be chosen between two possibilities (High and Low) than can be defined externally by the resistors R5, R6 and R7 : Fig.5 let well understand how to calculate the dividers that fix V2 H (wider t_{on}) and V2 L (wider t_{off}). It may be needed to drive stepper motors that require a higher peak current than told above. In this case each motor phase requires a particular application arrangement (see Fig.9b). In Fig. 9a, all the protection components are integrated with the exception of Z1. In Flg. 9b the clamp of the voltage spikes generated by the stray inductance Ls is achieved using Transil protection T1 and T2 that works also as additional diodes during current recirculation at the phase change. The diode D1, externally connected, is recommended at the highest working current levels and/or when the supplied voltage (plus Back EMF) at the end of the motor winding is too much unbalanced.

Figure 9a: Output Configuration as it is obtained by the Application Circuit

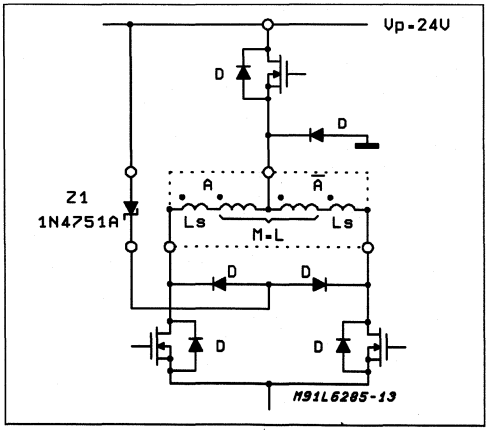
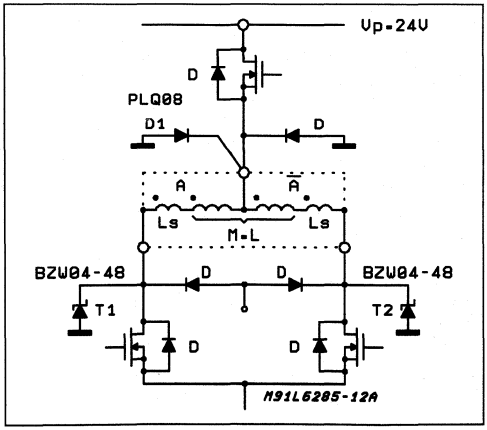


Figure 9b: Output Configuration at Higher Operating Currents



THERMAL CHARACTERISTICS

The cooling of the device is obtained by soldering its ground pins on a proper p.c.b copper side, acting as a true heatsink. By considering four squared side as in Fig.10, the junction to ambient thermal resistance has been measured (see Fig.11). The typical transient thermal resistance versus values of single pulse width of power is shown in Fig.12. In general these thermal characteristics are very important to the designer to optimize the L6285 applications.

Figure 10: Four "on board" Square Heatsink

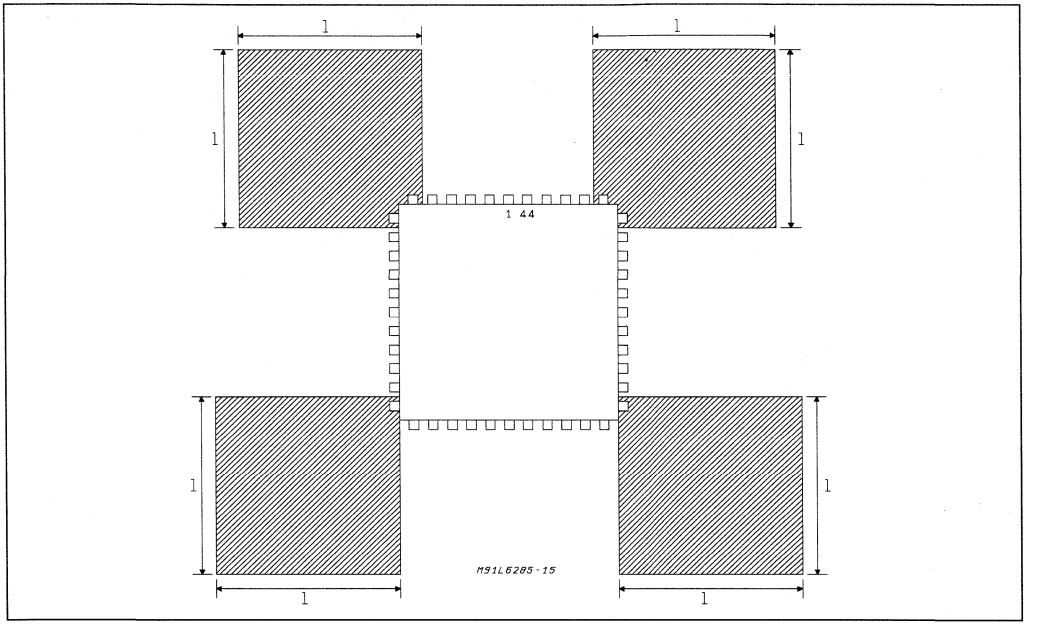


Figure 11: Typical $R_{th\ j\text{-}amb}$ vs. lenght "l" (Fig. 10)

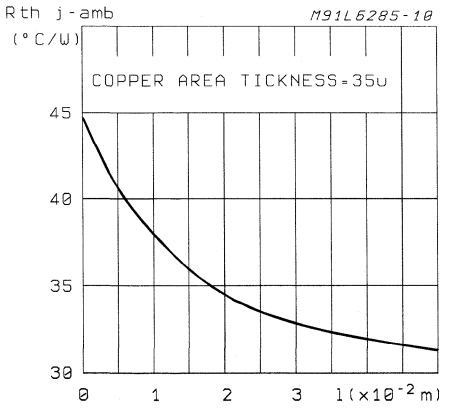
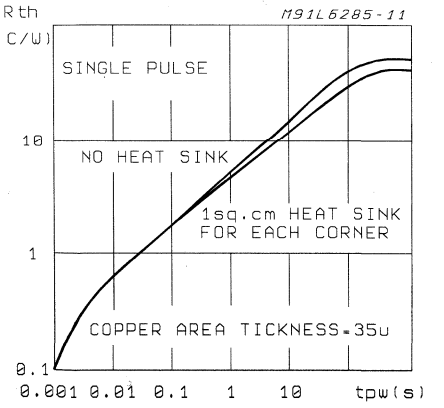


Figure 12: Typical Transient Thermal Resistance vs. Time or Pulse Width



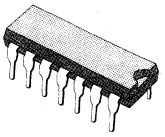
SOLENOID CONTROLLER

PRELIMINARY DATA

- SWITCH MODE CURRENT REGULATION
- TTL COMPATIBLE LOGIC INPUTS
- DRIVES ONE OR TWO EXTERNAL POWER TRANSISTORS
- VERY PRECISE ON-CHIP REFERENCE
- ANALOG CURRENT CONTROL INPUT
- ADJUSTABLE CURRENT RISE AND FALL TIME CONTROL INDEPENDENT OF SOLENOID SUPPLY VOLTAGE
- UNDERVOLTAGE LOCKOUT

DESCRIPTION

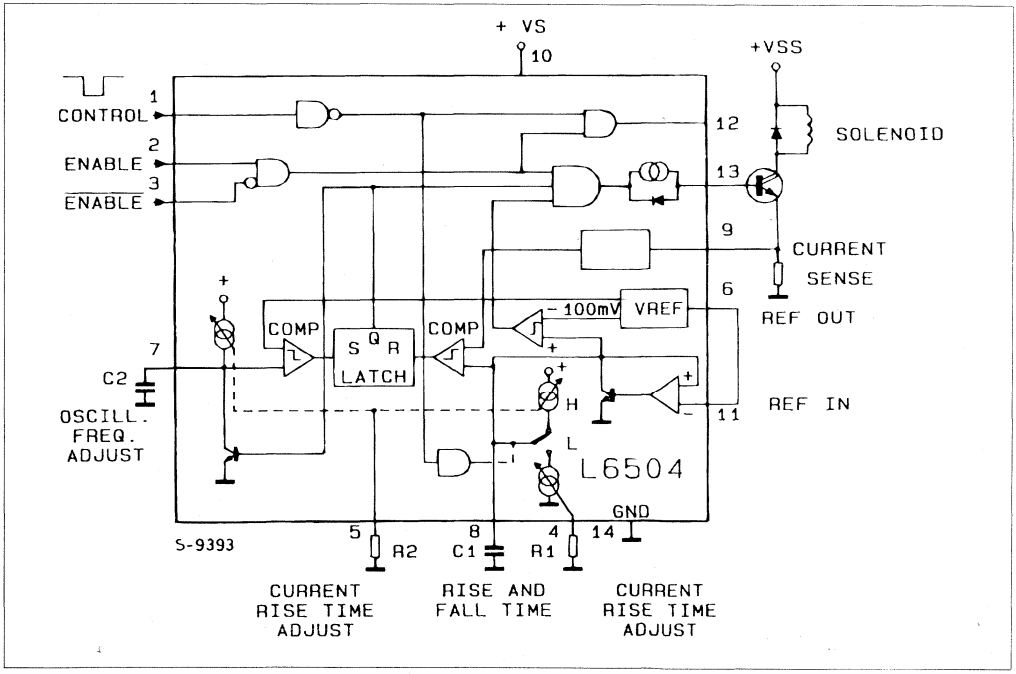
Designed for use with one external power transistor, the L6504 drives the hammer solenoid in daisy-wheel printers and typewrites. The device is controlled by three logic inputs and features switchmode regulation of the load current. A key feature of the device is that the rise and fall time of the load current can be set by external components. Additionally an analog input allows the load current to be set by an external DC voltage. An undervoltage lockout circuit guarantees the output off state for switch on phase.



DIP-14 Plastic
(0.25)

ORDER CODE : L6504

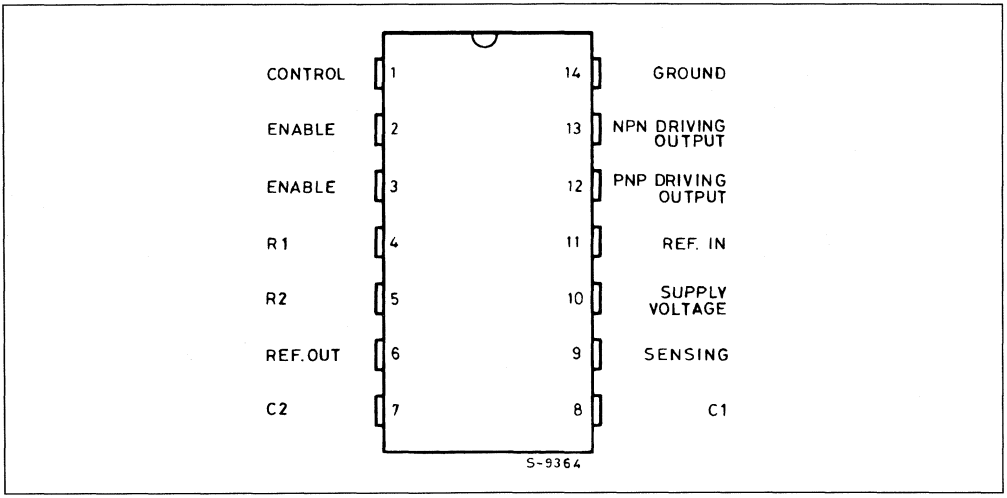
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	10	V
$V_{2,3}$	Enable Input Voltage Range	– 0.3 to 7	V
V_1	Control Input Voltage Range	– 0.3 to 7	V
V_9	Sense Voltage	– 0.3 to 2	V
I_6	Reference Output Current	2	mA
V_{11}	External Reference Voltage	2	V
T_{stg}	Storage Temperature	– 55 to 150	°C
T_j	Junction Temperature	– 55 to 150	°C
T_{op}	Operating Temperature	0 to 85	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN FUNCTION

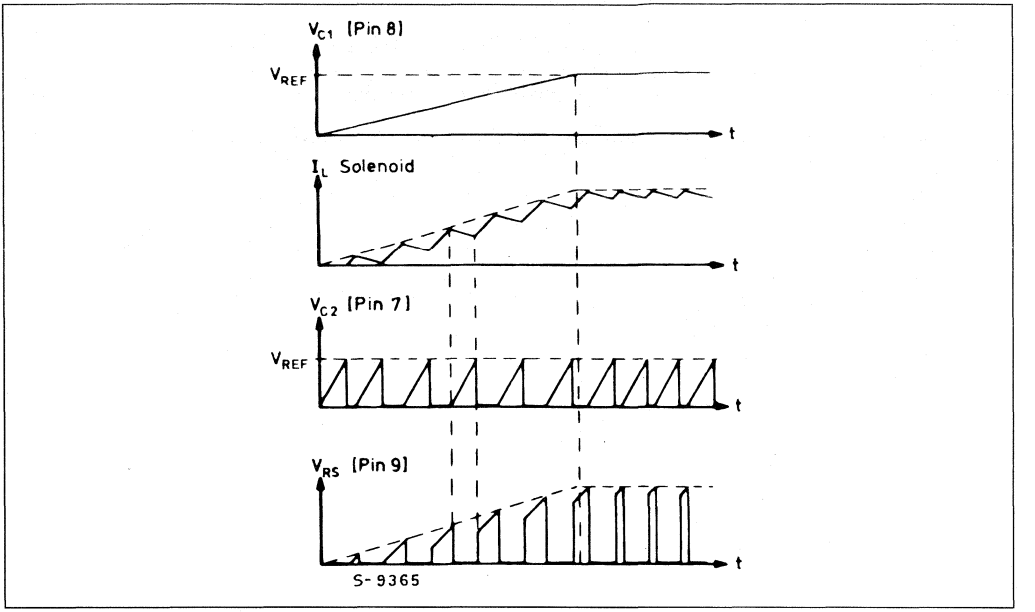
N°	Name	Function
1	CONTROL	TTL Compatible Control Input. A low level activates the output, driving the load. Internal Pull-up Resistor.
2	ENABLE	TTL Compatible Enable Input. A low level disables the output stage.
3	$\overline{\text{ENABLE}}$	TTL Compatible Enable Input. A high level disables the output stage.
4	R1	The value of this resistor (*) sets slope of trailing edge of load current.
5	R2	The value of this resistor (*) sets slope of leading edge of load current.
6	REFERENCE OUT	Output for Internal Reference Voltage.
7	C2	The value of this capacitor sets the duration of power transistor switch off time.
8	C1	The value of this capacitor sets slope of leading and trailing edge of load current.
9	SENSING	Connection for Load Current Sense Resistor. Value sets the maximum load current : $I = V_{ref}/R_s$.
10	SUPPLY VOLTAGE	Supply Voltage Input.
11	REFERENCE IN	Input for External Reference Voltage to Control Load Current by DC-level.
12	PNP DRIVING OUTPUT	Output to Control External PNP-transistor for Fast Current Discharge.
13	NPN DRIVING OUTPUT	Output for Basecharge and Discharge of External Power Transistor.
14	GROUND	Ground

(*) Value between 10 kΩ and 200 kΩ (or open).

ELECTRICAL CHARACTERISTICS

N°	Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
1 .	V_s	Operating Supply Voltage	10		4.5		10	V
2 .	V_{sth}	Supply Voltage Threshold For Output Switch-off	10	V_{CH} = LOW V_E = HIGH	2.96	3.7	4.45	V
3 .	I_s	Quiescent Current	10	Pin1 Highstate		7	12	mA
4 .	V_{CL}	Control Voltage	1	Low State			1.5	V
5 .	V_{CH}	Control Voltage	1	High State	2.3			V
6 .	I_{CL}	Control Input Current	1	V_1 Low State	– 1		0	mA
7 .	I_{CH}	Control Input Current	1	V_1 High State	– 0.6		5	uA
8 .	V_{EL}	Enable Voltage	2/3	Low State			1.5	V
9 .	V_{EH}	Enable Voltage	2/3	High State	2.3			V
10 .	I_{IN}	Input Current	2/3	$V_{2,3}$ Low State	– 10		1	µA
11 .	I_{IN}	Input Current	2/3	$V_{2,3}$ High State	– 1		5	µA
12 .	V_{DL}	Driving Voltage Low	13	R13, 14 = 5 K Low State			0.5	V
13 .	I_D	Driving Current	13	V_{13} = 2 V	6.5	10	16	mA
14 .	V_{SE}	Sense Voltage	9		0		2	V
15 .	V_{ref}	Reference Voltage	6	I_6 = 0. . . 2 mA	1.28	1.33	1.38	V
16 .	I_{ref}	Reference Current	6				2	mA
17 .	V_{RIN}	Reference Input	11		0.3		2	V
18 .	I_{C8}	Charge Current	8	R2 (Pin 5) = 20 K Pin1L	58	65	72	µA
19.	I_{D8}	Discharge Current	8	R1 (Pin 4) = 20 K Pin1H	28	32.5	37	µA
20 .	I_{SD}	Source Current	12	V_{12} = 2 V	0.5	1	1.6	mA
21 .	V_{sats}	Source Saturation Voltage	12	Isource = 0.5 mA			1.2	V
22 .	V_{sats}	Sink Saturation Voltage	12	Isink = 2 mA			0.4	V
23 .	V_{V-I}	VI-Converter Voltage	4 / 5	10 K < R1, 2 < 200 K R1 = R2	1.26	1.32	1.4	V
24 .	t_r	Recirculation Time of Load Current	7	C2 = 1.5 ns R2 = 20 Kohm	27	30	33	µs
25 .	t_D	Current Sense Delay Time	9		0.3	1	2.5	µs

Figure 1 : Timing Diagram Start Phase.



APPLICATION INFORMATION

Figure 2 : Free Running Load Current Leading and Trailing Edge.

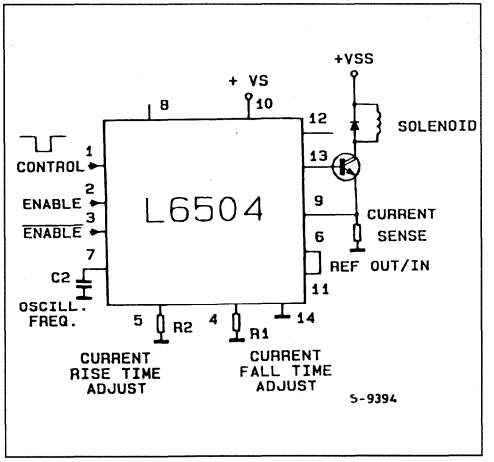


Figure 3.

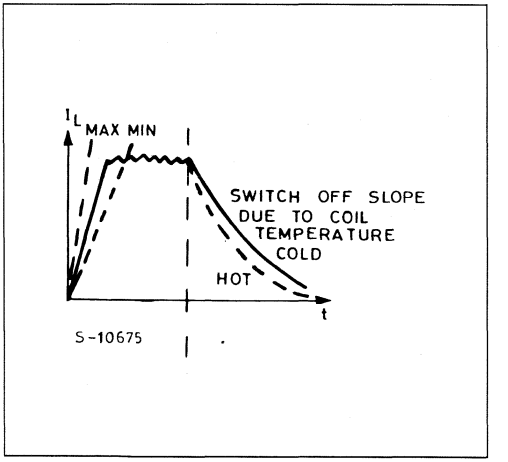


Figure 4 : Slew Rate of Leading and Trailing Edge Controlled.

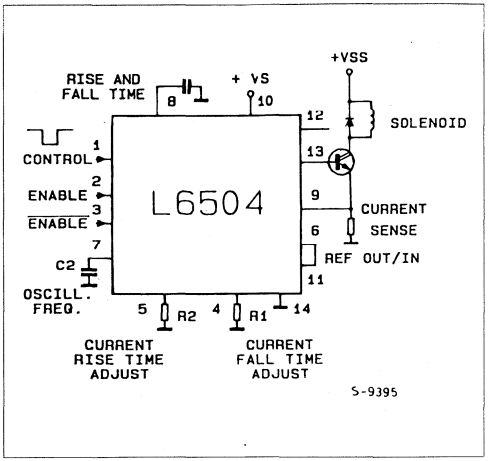


Figure 7.

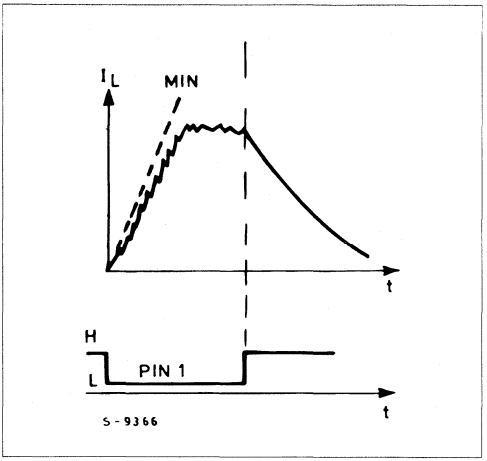


Figure 6 : Slew Rate of Leading Edge Controlled

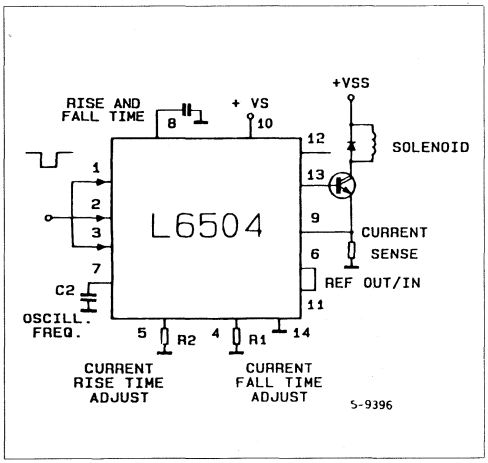


Figure 5.

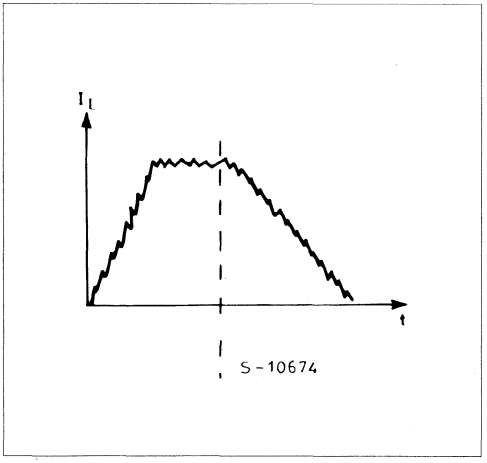


Figure 8 : Free Running Leading Edge Fast Current Slope at Trailing Edge.

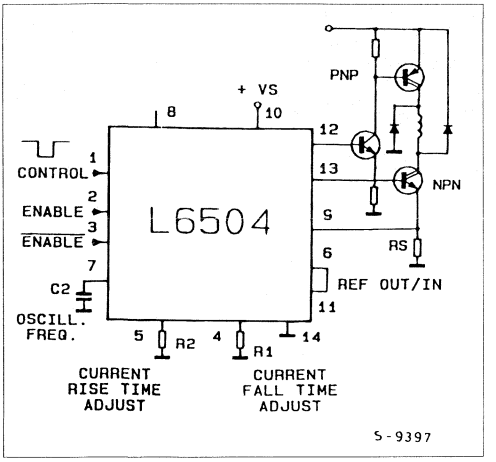
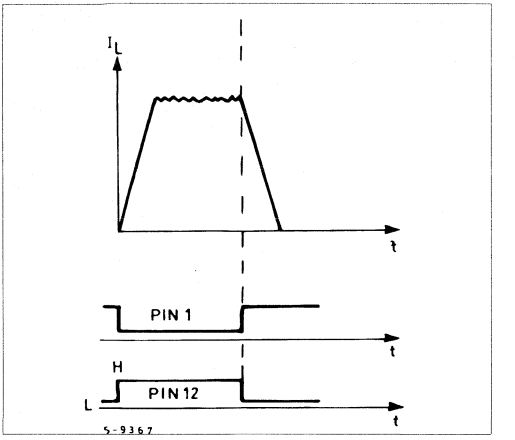


Figure 9.



SGS-THOMSON
MICROELECTRONICS

L6506
L6506D

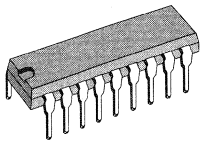
CURRENT CONTROLLER FOR STEPPING MOTORS

ADVANCE DATA

DESCRIPTION

The L6506/D is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, L6114/L6115, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

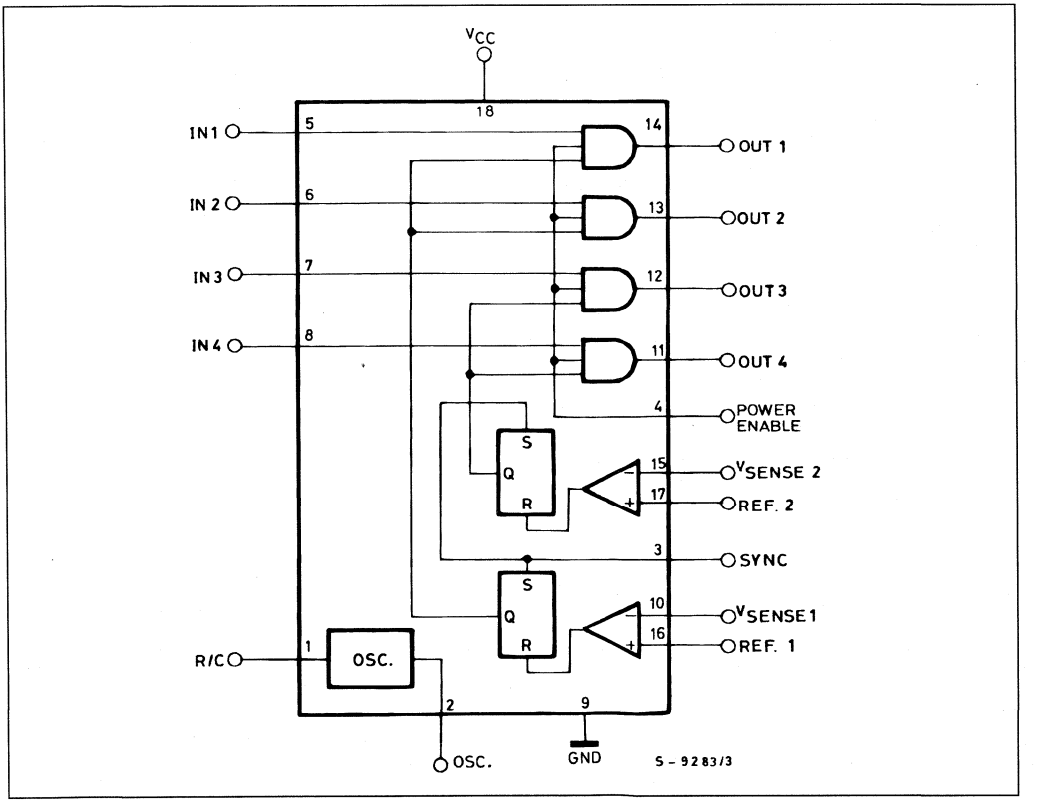
Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.



DIP-18 **SO-20**

ORDERING NUMBERS:
L6506 L6506D1

BLOCK DIAGRAM (pin's number referred to DIP-18)



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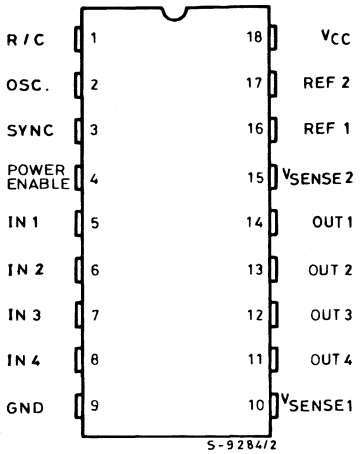
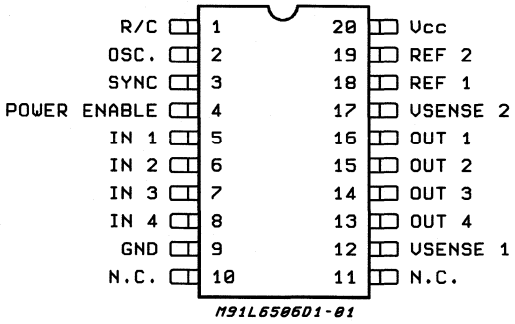
PIN CONNECTIONS (top view)



DIP18



SO20

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	10	V
V_i	Input Signals	7	V
P_{tot}	Total Power Dissipation (T_{amb} = 70°C) for DIP18 for SO20	1 0.8	W W
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter		DIP18	SO20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_{amb} = 25 °C ; unless otherwise noted)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5		7	V
I_{CC}	Quiescent Supply Current	V_{CC} = 7 V			25	mA

COMPARATOR SECTION

V_{IN}	Input Voltage Range	V_{sense} Inputs	– 0.3		3	V
V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 5.0	mV
I_{IO}	Input Offset Current				± 200	nA
I_{IB}	Input Bias Current				1	µA
	Response Time	V_{REF} = 1.4 V V_{SENS} = 0 to 5 V		0.8	1.5	µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

COMPARATOR SECTION PERFORMANCE (over operating temperature range)

V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 20	mV
I_{IO}	Input Offset Current				± 500	nA

LOGIC SECTION(over operating temperature range) - (TTL compatible inputs & outputs)

V_{IH}	Input High Voltage		2.0		V_s	V
V_{IL}	Input Low Voltage				0.8	V
V_{OH}	Output High Voltage	V_{CC} = 4.75 V I_{OH} = 400 µA	2	3.5		V
V_{OL}	Ouptut Low Voltage	V_{CC} = 4.75 V I_{OH} = 4.0 mA		0.25	0.4	V
I_{OH}	Ouput Source Current Outputs 1 - 4	V_{CC} = 4.75 V	2.75			mA

OSCILLATOR

f_{osc}	Frequency Range		5		70	KHz
V_{thL}	Lower Threshold Voltage			0.33 V_{CC}		V
V_{thH}	Higher Threshold Voltage			0.66 V_{CC}		V
R_i	Internal Discharge Resistor		0.7	1	1.3	KΩ

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7150, quad DMOS array such as L6114-L6115, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation :

$$f = \frac{1}{0.69\ RC} \quad \text{for } R > 10\ K$$

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref}. Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is 1/3 V_{CC}. Upper threshold is 2/3 V_{CC} and internal discharge resistor is 1 KΩ ± 30 %.

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can be found by looking at the figure 1 and are :

$$T2 = 0.69\ C1\ \frac{R1\ R_{IN}}{R1 + R_{IN}} \quad (1)$$

$$T1 = 0.69\ R1\ C1 \quad (2)$$

$$DC = \frac{T2}{T1 + T2} \quad (3)$$

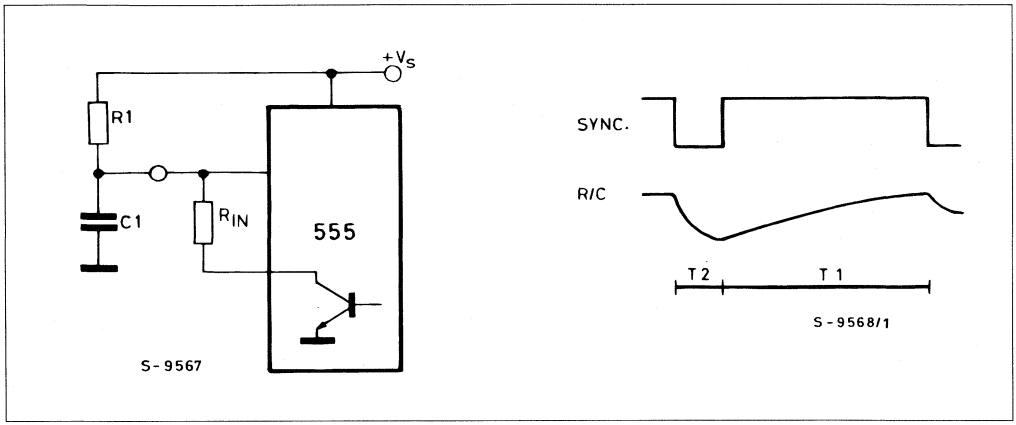
By substituting equations 1 and 2 into equation 3 and solving for the value of R1 the following equations for the external components can be derived :

$$R1 = \left(\frac{1}{DC} - 2\right) R_{IN} \quad (4)$$

$$C1 = \frac{T1}{0.69\ R1} \quad (5)$$

Looking at equation 1 it can easily be seen that the minimum pulse width of T2 will occur when the value of R1 is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R1 of 700Ω (1 KΩ – 30 %) should be used to guarantee the required pulse width.

Figure 1 : Oscillator Circuit and Waveforms.



APPLICATIONS INFORMATION

The circuits shown in figure 2 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. The peak current can be calculated using the equation :

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

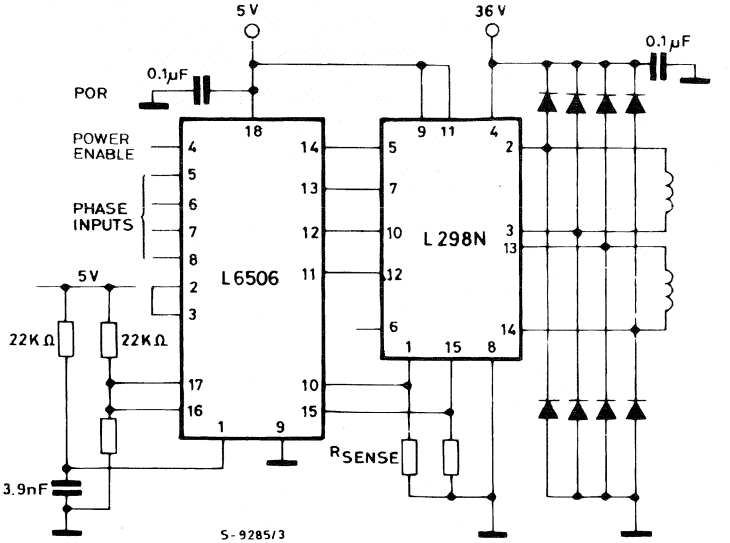
The circuit of Fig.2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

Figure 2 : Application Circuit Bipolar Stepper Motor Driver. (pin's number referred to DIP18)



SGS-THOMSON MICROELECTRONICS

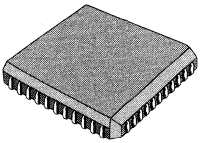
L6515

DUAL DC-MOTOR POSITIONING SYSTEM

ADVANCE DATA

- PRECISE OPERATION ALSO WITH LOW COST OPTICAL ENCODER
- PWM - OUTPUT FOR DIGITAL SWITCHED POWER BRIDGES
- DIRECTION INDICATOR FOR EASY POSITION COUNTING WITH µP
- EXTERNAL LOOP GAIN AND TRANSFER FUNCTIONAL ADJUSTMENT
- PARALLEL ADDRESSED INPUTS WITH LATCH
- 44 LEAD PLCC PACKAGE

MULTIPOWER BCD TECHNOLOGY



PLCC44

ORDERING NUMBER: L6515

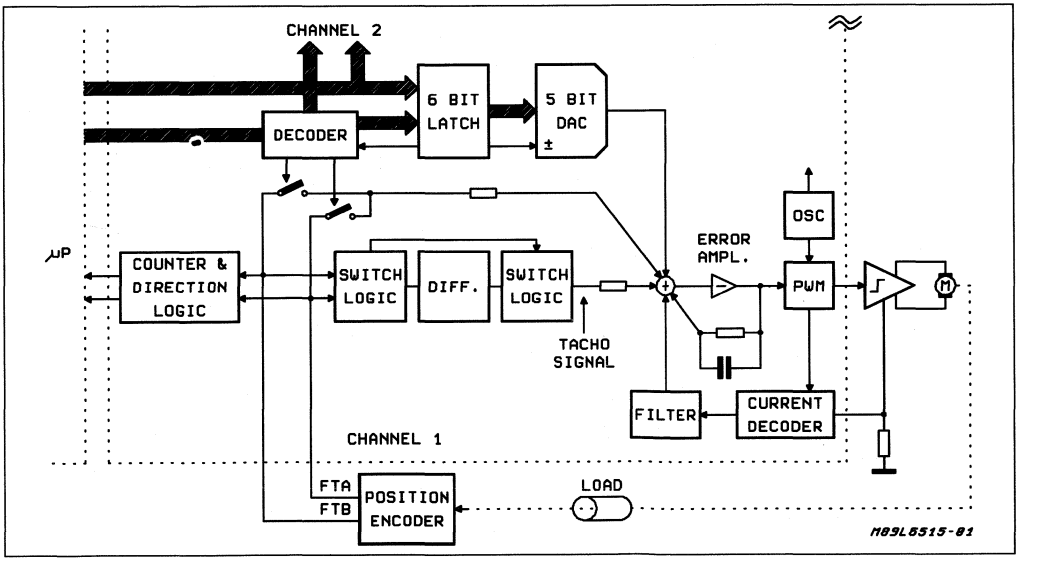
DESCRIPTION

The L6515 is a monolithic integrated circuit in BCD-Technology assembled in a PLCC-44 plastic chip carrier.

The device contains all functions for a complete dual DC-Motor positioning system. For the motor driver stage only digital switched bridges are needed.

Useful are L293E, L298, L6203 and L6202. The device is intended to drive DC-Motors in typewriters, printers, plotters and general purpose industrial applications.

SYSTEM BLOCK DIAGRAM (ONE CHANNEL)



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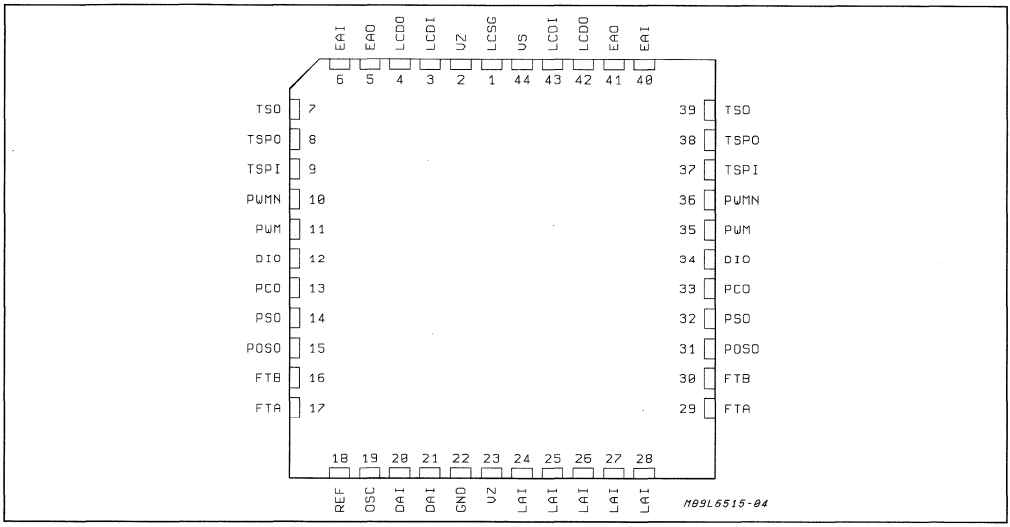
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	12	V
V_{IA}	Analog Inputs Voltage	-0.3 to 7	V
V_{IL}	Logic Inputs Voltage	-0.3 to 7	V
V_O	Open Collector Output Current	12	V
I_O	Open Collector Current	10	mA
I_Z	Zener Current	20	mA
T_{stg}, Tj	Storage Temperature	-40 to 150	°C
T_{amb}	Operative Ambient Temperature	0 to 70	°C

PIN CONNECTION (top view)



SYSTEM DESCRIPTION

The L6515 is intended to be used as a microprocessor controlled positioning system.

For the motor driver stage only digital operating bridges are needed like L293E, L298, L6203, L6202.

The system operates in two modes to achieve high-speed, high-accurancy positioning.

Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the controller chip, which in turn gets its information from the encoder. From this basic input, the microprocessor computes a 6-bit control word that sets the system speed and direction dependent on the distance to travel.

When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processors signal thus reducing accelerating torque. The motor continues to run at top speed but under closed-loop control.

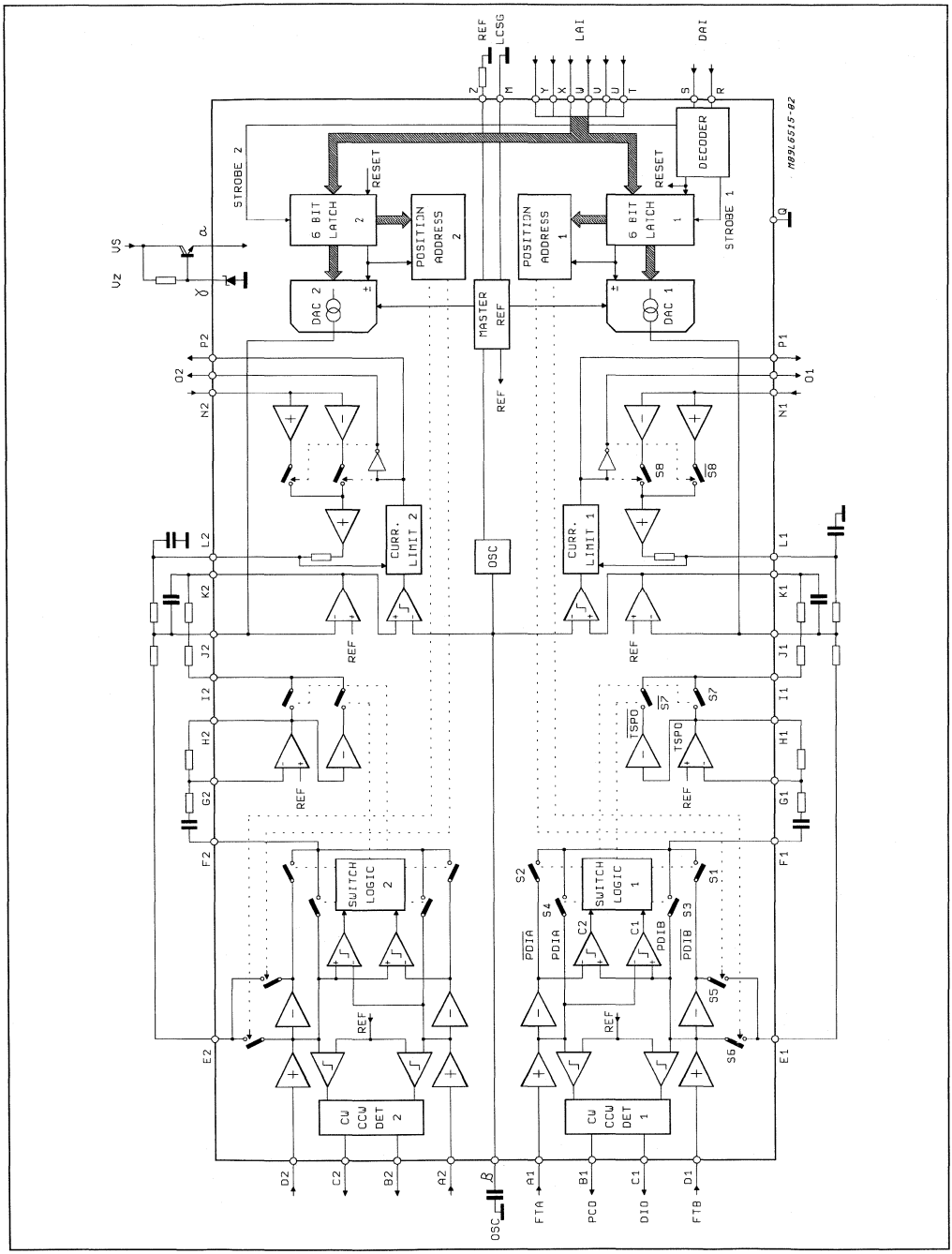
As a target position is approached, the microprocessor lowers the value of the speed-demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.

At that time, the microprocessor orders a switch to the position mode, and within 3 to 4ms the power stage drives the motor to a null position, where it is held by electronic "detening".

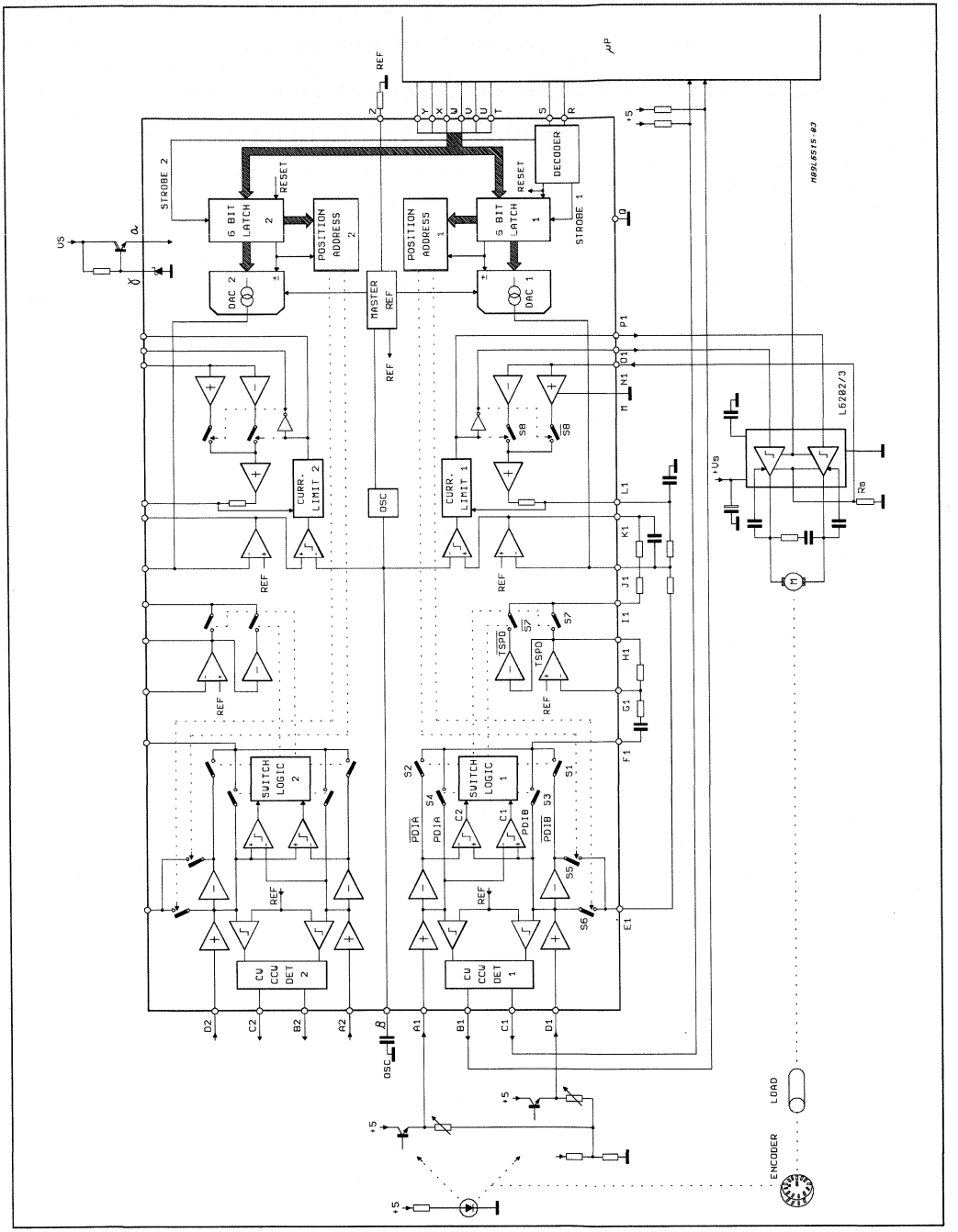
PIN FUNCTIONS

Pin	Name	Description
1	LCSG	Load Current Decoder Sens Reference Ground
2,23	V_Z	Zener Clamp
3,43	LCDI	Load Current Decoder Input
4,42	LCDO	Load Current Decoder Output
5,41	EAO	Error Amplifier Output for Current Mode PWM Modulator
6,40	EAI	Error Amplifier Input for Current Mode PWM Modulator
7,39	TSO	Tacho Signal Output
8,38	TSPO	Tacho Signal Processor Output
9,37	TSPI	Tacho Signal Processor Input
10,36	PWMN	Current Mode PWM Output Inverted
11,35	PWM	Current Mode PWM Output non Inverted
12,34	DIO	Direction Indicator Digital Open Collector Output. A Low Level is cw, A High Level is ccw Operation of the Motor
13,33	PCO	Position Counter Digital Open Collector Output
14,32	PSO	Phase Selector Output for Signal Differentation
15,31	POSO	Positioning Output. The Output Becomes Activated via Position Adress Decoder.
16,30	FTB	Analog Input from Position Encoder Phase B. Proposed Operation Range is 2.8V ± 1V.
17,29	FTA	Analog Input from Position Encoder Phase A. Proposed Operation Range is 2.8V ± 1V
18	REF	Master Current Reference
19	OSC	Oscillator
20,21	DAI	Decoder Logic Input for Latch Select + Reset
22	GND	Major and Logic Ground
24 to 28	LAI	Latch Adress Input
44	V_S	Supply Voltage

SCHEMATIC DIAGRAM



APPLICATION CIRCUIT


µP
REF
Z
Y
X
W
U
V
T
S
R
+5
DECODER
STROBE 2
RESET
6 BIT LATCH 2
POSITION ADDRESS 2
POSITION ADDRESS 1
6 BIT LATCH 1
RESET
STROBE 1
Q
Vs
DAC 2
MASTER REF
DAC 1
P1
O1
N1
M
L1
K1
J1
I1
H1
G1
F1
E1
CURR. LIMIT 2
OSC
CURR. LIMIT 1
S8
S6
REF
TSPD
S7
SWITCH LOGIC 2
SWITCH LOGIC 1
S2
S4
S1
S3
PD1A
C2
C1
PD1B
S5
S6
CW CCW DET 2
CW CCW DET 1
D2
C2
B2
A2
8
OSC
A1
B1
C1
D1
L6202/3
+Vs
Rs
M
ENCODER
LOAD
MOTOR
MOTOR
MOTOR

ELECTRICAL CHARACTERISTICS (refer to test circuit, V_S=10V, I_{REF}=300µA, T_{amb}=25 °C unless otherwise specified)

Symbol	Parameter	Pin	Test Condition	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range			7		11	V
I_S	Quiescent supply current					50	mA
V_Z	Zener Voltage		I_z=1mA	8,5	9.9	11,4	V
I_Z	Operating Zener Current			1			mA

POSITION ENCODER SECTION

V_I	Operating Input Voltage Range	A/D/1/2	referred to V_{REF}	-1,65		+1,65	V
I_I	Input Bias Current					1	µA
V_{OS}	INput-output Offset Voltage Between A/D/1/2 and F/1/2		S3 or S4 closed I_o=0			±15	mV
			S1 or S2 closed I_o=0 $V_{IN}=V_{REF}$			±20	mV
V_{SAT}	Output Saturation Voltage	B/C/1/2	I_o=1.4mA			0.4	V
I_{OH}	Output Leakage Current					10	µA
V_{TH}	Threshold Hysteresis voltage Between A/1/2 and B/1/2 D/1/2 and C/1/2			80		150	mV
R_{ON}	Output Resistance ON State	E/F/1/2	One of S1 to S6 closed		150	300	Ω
V_{OL}	Output Operating Low Voltage	E/F/1/2	referred to V_{REF} I_O=1mA			-1.2	V
V_{OH}	OutpUt Operating High Voltage			+1.2			V

TACHO SIGNAL PROCESSING SECTION

Symbol	Parameter	Pin	Test Condition		Min.	Typ.	Max.	Unit
V_I	Input Voltage	G/1/2	gain=1 referred to V_{REF}		-1.65		+1.65	V
I_I	Input Bias Current						1	µA
V_{OL}	Output Operating Low Voltage	H/1/2	referred to V_{REF}				-1.62	V
		I/1/2	I_O=1mA	$\overline{S7}$ closed			-1.3	
V_{OH}	Output Operating low Voltage	I/1/2			+1.3			
		H/1/2			+1.62			
R_{ON}	Output Resistance On State	I1/2	S7 or $\overline{S7}$ closed			150	260	Ω
V_{OS}	Input Offset Voltage	H1/2	V_{IN}=V_{REF} S7 closed I_o = 0				±20	mV
V_{OS}	Input Offset Voltage	G1/2	referred to V_{REF} g1/2 shorted to H1/2				±20	mV
R_{MO}	Output Matching Resistance	I1/2	S7 or $\overline{S7}$ closed		0.8		1.2	Ω

ERROR AMPLIFIER SECTION

V_I	Input Voltage	J1/2	gain=1	1		4.6	V
I_I	Input Bias Current					1	µA
V_{OL}	Lower Clamping Voltage	K1/2	I_o=1ma	-1.45		-1.22	V
V_{OH}	Higher Clamping Voltage		refered to V_{REF}	+1.06		+1.56	V
V_{OS}	Input Offset Voltage	J1/2	referred to V_{REF} K1/2 J1/2 shorted			±20	mV

CURRENT DECODER SECTION

V_{OS}	Output Offset Voltage	L1/2	N1/2=0 referred to V_{REF}			±140	mV
R_{OUT}	Output Resistance			0.5		1.7	KΩ
V_{CLH}	Current Limit Threshold	O1/2 P1/2	referred to V_{REF}		±0.5		V
V_{CDO}	Differential Output Offset Voltage	L1/2	$V_{off(+)}$ - $V_{off(-)}$			±20	mV

OSCILLATOR -PWM SECTIONS

Symbol	Parameter	Pin	Test Condition	Min.	Typ.	Max.	Unit
V_H	Upper Triangle Threshold		Referred to V_{REF}	+1.2		+1.8	V
V_L	Lower Triangle Threshold			-1.6		-1.3	V
I_{CD}	Charge/Discharge Current		I_{REF}=500µA	±160		±180	µA
V_O	PWM Output Voltage	O1/2	I_o=1.4mA			0.4	V
		P1/2		2.7			

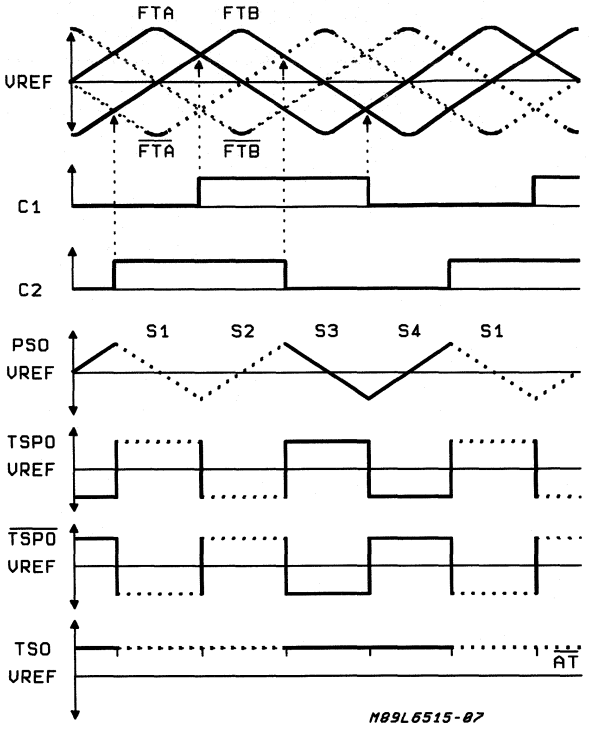
DAC SECTION

I_{REF}	Current Reference Input Range	Z		0.3		0.7	mA
I_O	Sink and Source Output Current	J1/2	I_{REF}=0.5 mA	918	968	1018	µA
V_{REF}	Reference Voltage	Z	I_{REF}=20 µa	2.7	2.8	2.9	V
I_O	Linearity Error	J1/2	I_{REF}=0.5 mA			1.61	/FS

INPUT LOGIC SECTION

V_{INL}	Input IOw Voltage	R S		-0.3		0.8	V
V_{INH}	Input High Voltage	T U		2		7	V
I_L	Input	V W				-10	µA
I_H	Input High Current High Voltage	X Y				30	µA

APPLICATION CIRCUIT



TRUTH TABLE TACHO-ENCODER LOGIC

INPUT SIGNAL

PDIB > PDIA	C 1 = HIGH
PDIB < PDIA	C 1 = LOW
PDIB > $\overline{PDIA}$	C2 = HIGH
PDIB < $\overline{PDIA}$	C2 = LOW

SWITCH SIGNAL

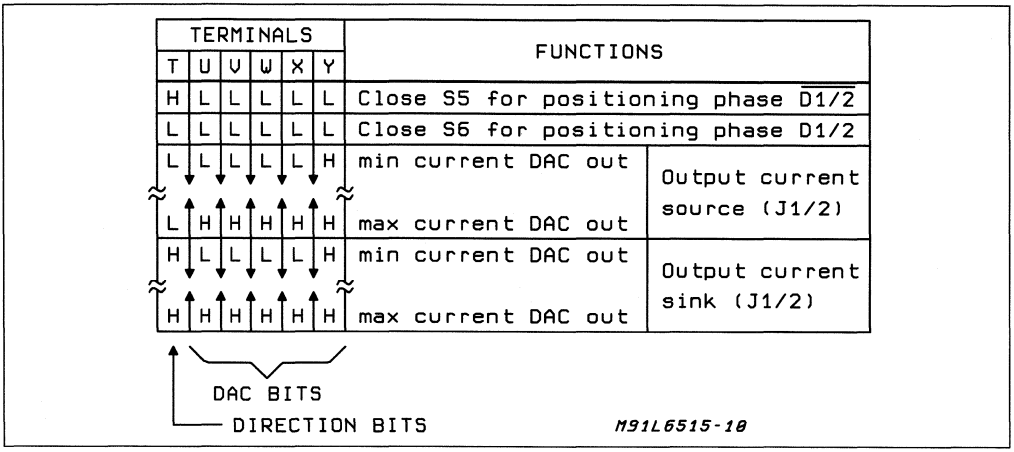
C1	C2	CLOSED	S2 POSITION
L	H	S1	TSPO
H	H	S2	$\overline{TSPO}$
H	L	S3	TSPO
L	L	S4	$\overline{TSPO}$

TRUTH TABLE LOGIC SELECTION CHIP ADDRESS

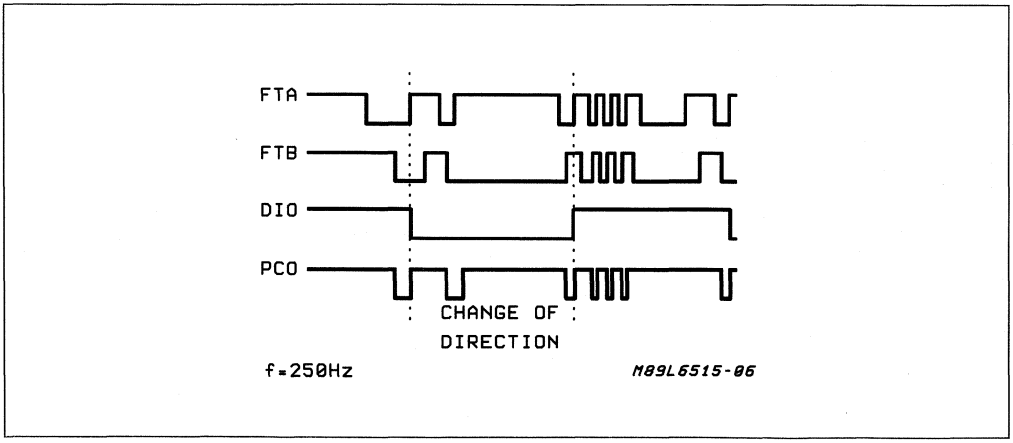
DECODER ADDRESS

Terminals		Functions
R	S	
L	L	NO ACTION
H	L	STROBE LATCH 1
L	H	STROBE LATCH 2
H	H	RESET LATCH 1/2

LATCH ADDRESS



TIMING DIAGRAM OF COUNTER AND DIRECTION INDICATION LOGIC



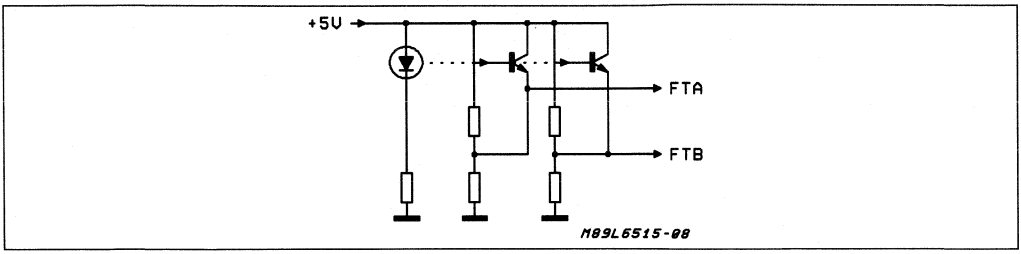
POSITION ENCODER

Main advantage of the operation principle of the positioning system is that a high performance position encoder is not required.

The system accepts several phases and amplitude errors of the encoder output signal without affecting the system performance.
Two position sensors are useful.

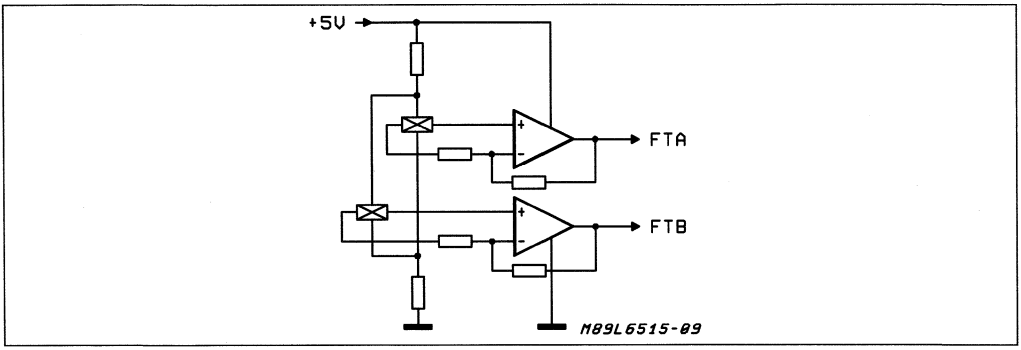
1) Optical-Encoder with IR-LED and Phototransistor

Figure 1.



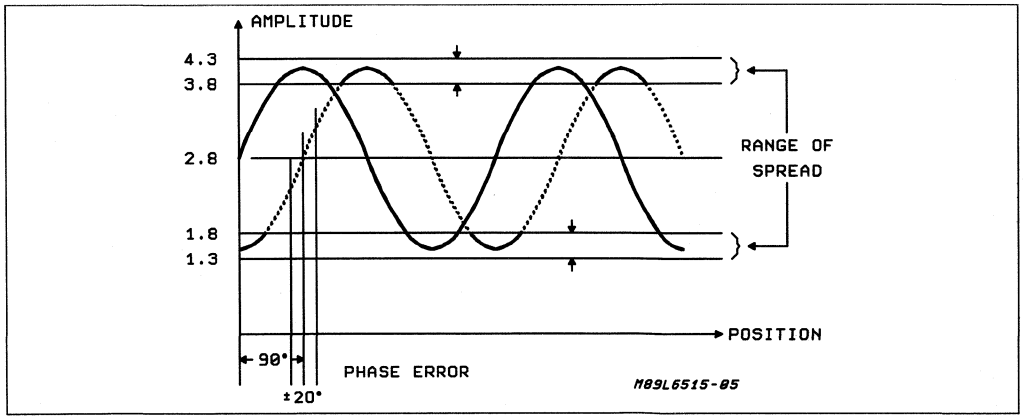
2) Magnetic Encoder with hall-effect sensors

Figure 2.



The allowed spread of the encoder output signal refer to reference level is shown in Fig.3.

Figure 3.



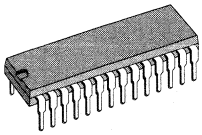
SGS-THOMSON MICROELECTRONICS

L6603A
L6604A

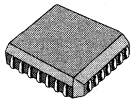
MEMORY CARD INTERFACE

ADVANCE DATA

- Single Power Supply operation
- Internal Clock Generator or External Clock Input
- Adjustable Precision of PVS Output Voltage (2%)
- 100mV/step of the Writing Output Voltage
- I/O, Reset and Clock Outputs Protection Against Short Circuit to GND and to V_{pvs}.



DIP28
ORDERING NUMBER: L6603A

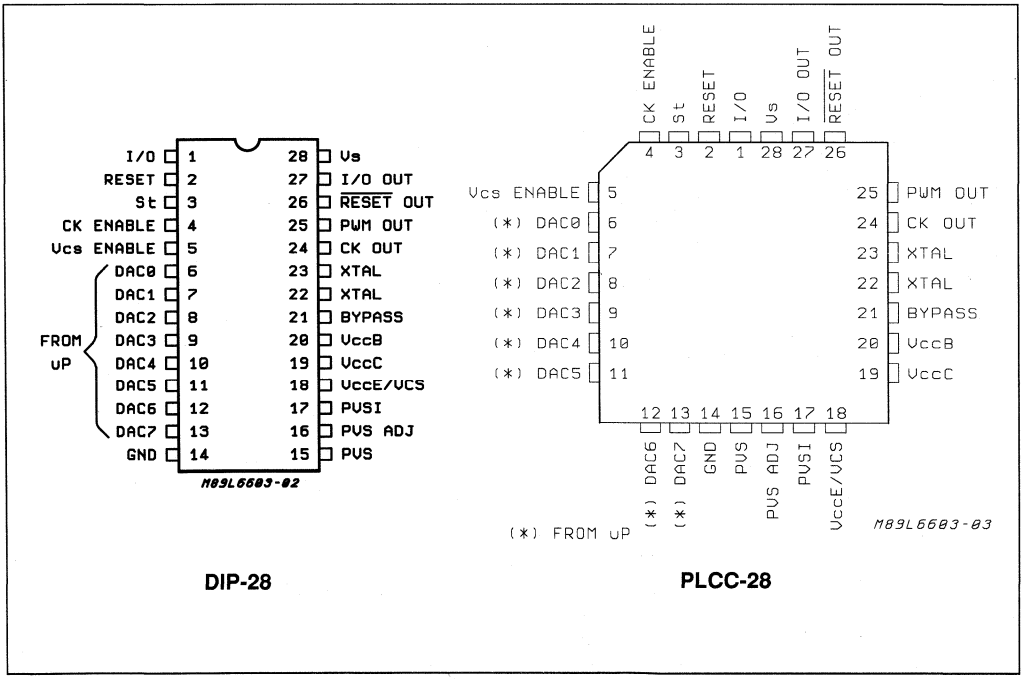


PLCC-28
ORDERING NUMBER: L6604A

DESCRIPTION

The L6603 and L6604 are integrated circuits for applications as interface between different types of memory card and a microprocessor which exchanges data with cards. It operates with a single power supply.

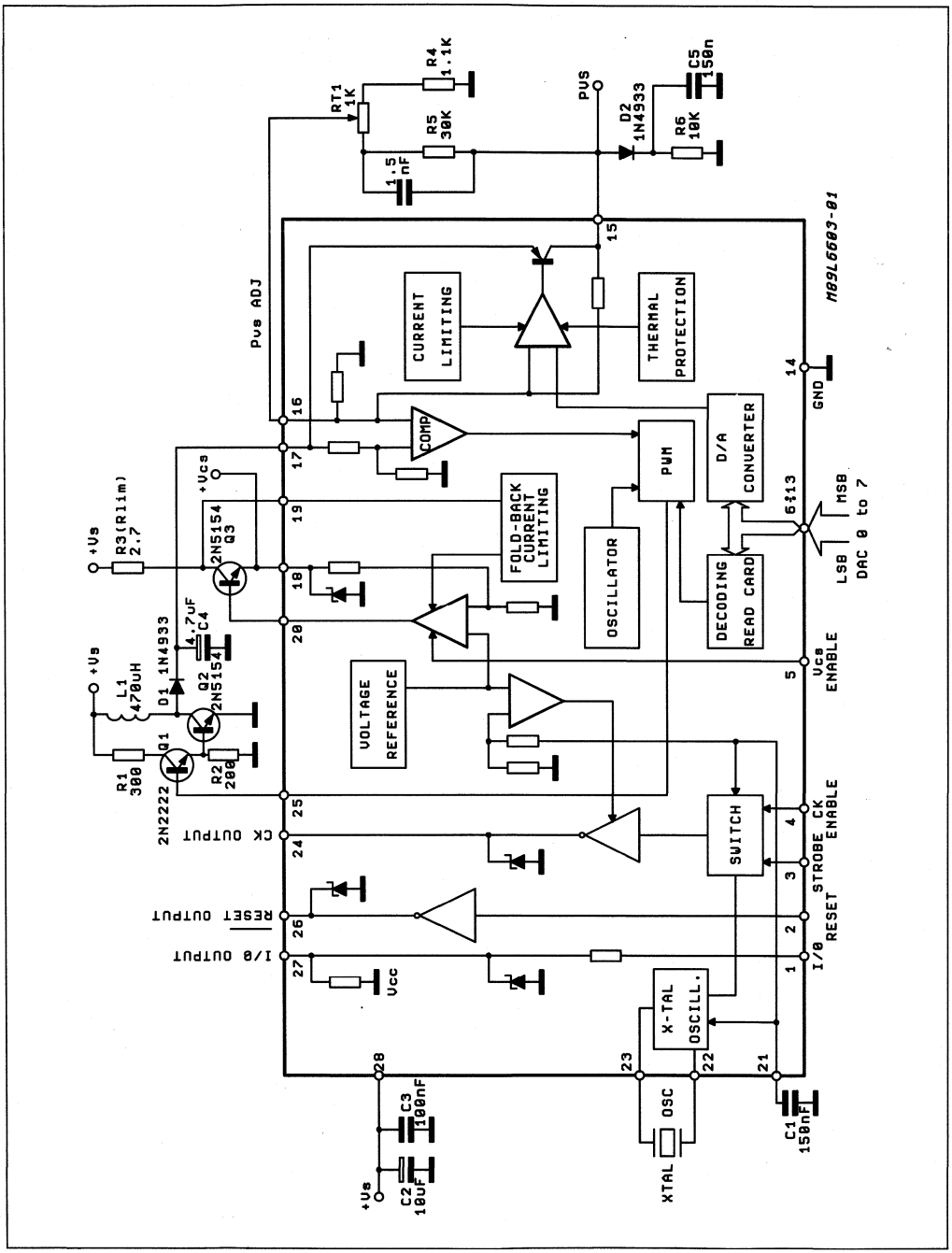
PIN CONNECTIONS



DIP-28 **PLCC-28**

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM AND FUNCTIONAL TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_s	Supply Voltage	11	V
T_{op}	Operating Temperature Range	-20 to 70	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

THERMAL DATA (*)

			DIP 28	PLCC 28	
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	100	°C/W

(*) With all the pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

Pin	Name	Function
1	I/O	Input of the Bidirectional Data Line
2	Reset	Control Input for Reset for Cards with µP and Memory
3	St	Strobe for Cards with Memory (TTL compatible)
4	CK ENABLE	Commutation for µP Cards CK ENABLE = 1 (internal clock)
5	VCS ENABLE	Control Input for VCS Supply Voltage for the Card
6 to 13	DAC0 to DAC7	Control Inputs for Programmation of V_{PVS} Supply (see Application Information)
14	GND	Ground
15	V_{PVS}	Programmable Supply for Memory Card (no use with decoupling capacitor) Note 7 (to the card)
16	V_{PVS} Adj	Adjustment Input for 2% Precision V_{PVS} Output
17	PVS I	Input for V_{PVS} Voltage Regulator
18 19 20	V_{CS} V_{CC} E C B	Inputs for Connection of Power Transistor (V_{CS} regulator) (decoupling capacitor on pin 18 <100nF if necessary) Note 8 (pin 18 to the card supply)
21	BYPASS	Reference Output Voltage (decoupling capacitor > 150nF). Note 9
22, 23	XTAL	Inputs for X-tal Connection. Note 10
24	CK OUT	Output for Clock Signal (TTL levels). Note 11 (to the card)
25	$\overline{\text{PWM OUT}}$	Output for DC/DC Step-up Converter
26	$\overline{\text{RESET}}$/OUT	Reset Output. Note 11 (to the credit card)
27	I/O Out	Output I/O. Note 11 (to the card)
28	V_S	Power Supply (Note 12)

ELECTRICAL CHARACTERISTICS (V_s = 8.5V; Tj = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{IH}	Input High Voltage		2			V	1
V_{IL}	Input Low Voltage				0.8	V	1
$\lvert I_{IH} \rvert$	Input High Current				250	µA	2
					500	µA	3
					100	µA	4
					400	µA	5
					200	µA	6

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$\lvert I_{IL} \rvert$	Input Low Current				150	µA	2
					300	µA	3
					10	µA	4
					200	µA	5
					300	µA	6
I_{SW}	Supply Current Writing Mode (pin 28)	$V_{PVS} = V_{PVSW}$ max		40	50	mA	13
I_{SR}	Supply Current Reading Mode (pin 28)	$V_{PVS} = V_{PVSR}$		40	50	mA	13
I_{stby}	Stand by current (pin 28)	All functions inhibited		35	50	mA	13
V_{CS}	Output Voltage Range	V_S = 7 to 10V; I_{CS} = 0 to -150mA; T_{amb} = -20 to 70 °C	4.8	5	5.2	V	8; 13
$\frac{\Delta V_{CS}}{V_{CS}}$	Load Regulation	I_{CS} = 0 to -150mA		0.18		%	13
$\frac{\Delta V_{CS}}{V_{CS}}$	Line Regulation	V_S = 7 to 10V		-50		dB	13
$\frac{\Delta V_{CS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{CS}	T_{amb} = -20 to 70 °C		65		dB	
t_{off1}	Fall Time of V_{CS}	Fig. 1; C_L = 30pF; I_{CS} = -30mA			200	µs	13
t_{off2}	Fall Time of V_{PVS}	Fig. 1 C_L = 30pF Write to Read	$\frac{V_{PVS}\ (V)}{2V/\mu s}$		200	µs	13
$\lvert I_{CS}$ max $\rvert$	Maximum Operating Current	V_{CS} -4% V_{CS}	180			mA	8; 13
$\lvert I_{CSL} \rvert$	Short Circuit Current limit			70	100	mA	8; 13
$V_{PVSW\ max}$	Maximum Programming Voltage (writing mode memory)	V_S = 8 to 10V; I_{PVS} = 0 to -30mA	24.5	25.5	26.5	V	13
V_{PVSW} max	Maximum Programming Voltage (writing mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -40mA	20.15	21	21.85	V	13
V_{PVSW} min	Minimum Programming Voltage (writing mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -50mA	4.9	5.1	5.3	V	13
V_{PVSR}	Output Voltage Range of PVS (reading mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -20mA	4.8	5	5.2	V	13
$\frac{\Delta V_{PVS}}{V_{PVS}}$	Load Regulation	I_{PVS} = 0 to -30mA @ V_{PVS} = 25.5V; I_{PVS} = 0 to -40mA @ V_{PVS} = 21V; I_{PVS} = 0 to -50mA @ V_{PVS} = 5.1V; Writing Conditions		0.8		%	13
$\frac{\Delta V_S}{\Delta V_{PVS}}$	Line Regulation	I_{PVS} = 0mA; V_S = 7 to 10V		50		dB	13
$\frac{\Delta V_{PVS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{PVS}	I_{PVS} = 0 mA; T_{amb} = -20 to 70 °C		74		dB	
$\lvert I_{PVS\ max} \rvert$	Short Circuit Current Limit		50	70	100	mA	13
V_{PVS} ADJ -V_{CS}	Differential Voltage between V_{PVS} (reading mode) & V_{CS}		-5		5	%	13
t_{pLH1}	Turn ON Time of V_{CS}	Fig. 1 C_L = 30pF			1	ms	
t_{pLH2}	Turn ON Time of VPVS	Fig. 1 CL = 30pF		50	200	µs	13

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
t_{on1}	Rise Time of V_{CS}	Fig. 1 C_L = 30pF			200	µs	13
t_{on2}	Rise Time of V_{PVS}	V_{PVS} = 5 to 25.5V; Fig. 1 C_L = 30pF			200	µs	13
V_{OH1}	High Output Voltage (pin 26)	(pin 26) V_{CSmin} I_{OH} = -200µA	4.2	4.8		V	
V_{OL1}	Low Output Voltage (pin 26)	(pin 26) VIH = 2V I_{OL} =+200µA		0.15	0.4	V	
V_{SC1}	Max Output Voltage during Short-circuit between V_{PVS} and pin 26				V_{CS} +0.3	V	
$\mid I_{SC2} \mid$	Short-circuit Current Limit (pin 26)				0.5	mA	
V_{OH2}	High Output Voltage (pin 27)	V_{CSmin} I_{OH} = -500µA V_{IHmax} = 2V	1.9			V	
V_{OL2}	Low Output Voltage (pin 27)	V_{CSmax} I_{OL} = 200µA V_{IHmin} = 0.8V			1	V	
V_{SC2}	Max Output Voltage during Short-circuit between VPVS and Pin 27				V_{CS} +0.3	V	
$\mid I_{SC3} \mid$	Short-circuit Current limit (pin 27)	I/O = 4.2V			30	mA	
V_{OH3}	High Output Voltage (pin 24)	I_{OH} = -200µA	3.5	4.1		V	
V_{OH4}	High Output Voltage (pin 24)	I_{OH} = -10µA	4.1	4.2		V	
V_{OL3}	Low Output Voltage (pin 24)	I_{OL} = 200µA		0.1	0.4	V	
V_{SC3}	Max Output Voltage during Short-circuit between Pin24 & V_{PVS} Output				V_{CS} +0.3	V	
$\mid I_{SC4} \mid$	Short-circuit Current Limit (pin 24)				35	mA	
t_{on}	Rise Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91MHz C_L = 30pF		15		ns	
t_{off}	Fall Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91MHz C_L = 30pF		18		ns	
	Duty Cycle (T1/T)	f_{XTAL} = 4.91MHz C_L = 30pF	40		60	%	14

Note 1: For inputs V_{CS} enable, Reset, I/O, St, CK enable DAC (0-7)
Note 2: For inputs DAC (0-7); I_{IH} is forward; I_{IL} is coming out.
Note 3: For input CK enable; I_{IH} is forward; I_{IL} is coming out.
Note 4: For input Reset; I_{IH} and I_{IL} are both forward.
Note 5: For input V_{CS} enable; I_{IH} is forward; I_{IL} is coming out.
Note 6: For Input I/O; I_{IH} and I_{IL} are both coming out.
Note 7: Internal thermal protection & current limiting system (see Block Diagram)
Note 8: Current limiting with "fold back system" (fig. 4)
Note 9: Internal current limiting system
Note 10: Input for external clock (fig. 3)
Note 11: Output protected against short-circuit to ground and to V_{PVS}
Note 12: The V_{CS} Voltage Regulator and the DC/DC step-up converter must be supplied with the same voltage.
Note 13: See functional Test Circuit
Note 14: When the External Clock is used, the network shown in fig. 3 is recommended.

APPLICATION INFORMATION

Operation of Programming Supply V_{PVS}

The output voltage VPVS can be programmed from 5V to 25.5V by steps of 0.1 V and can be expressed as follows:

$$V_{VPS} = \frac{\text{Decimal value of code DAC0–7}}{10}$$

Two operating modes are possible:
Reading mode (code DAC = 50): V_{PVS} = 5V;
Writing mode (Decimal value of code 51 to 255): V_{PVS} = 5.1 to 25.5V
In the latter case, the voltage drop between output of converter DC/DC (PVSI) and V_{PVS} is constant and typically of 3V.

The Decimal Value of an 8bit word is computed as it follws:

X	X	X	X	X	X	X	X	Word (DAC0-7)
7	6	5	4	3	2	1	0	Bit (n)

0	0	0	0	0	0	0	0	If X = L (*)
128	64	32	16	8	4	2	1	2^n if X = H (*)

(*) Corresponding Decimal Value

When V_{PVS} is requested to be of 21V the Decimal Value of Code DAC 0to7 is 210, that is obtained by:

128+ 64+ 0+ 16+ 0+ 0+ 2+ 0

Then the word is the following:

H	H	L	H	L	L	H	L	From µP

The throuth table of C_{Kout} is the following:

Strobe (pin 3)	$C_{Kenable}$ (pin 4)	C_{Kout} (pin 24)
H	L	L
L	L	H
X	H	Clock

Figure1: V_{CS} (V_{CC}) and V_{PVS} (V_{PP}) Times test sequence

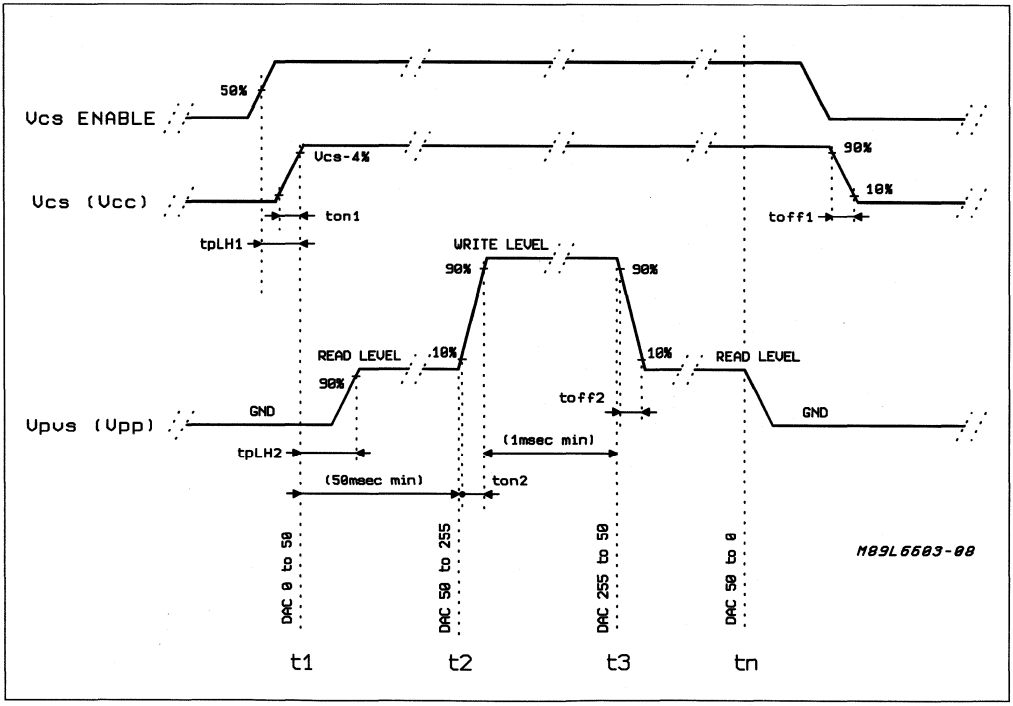


Figure 2: Clock Output Waveform and Times

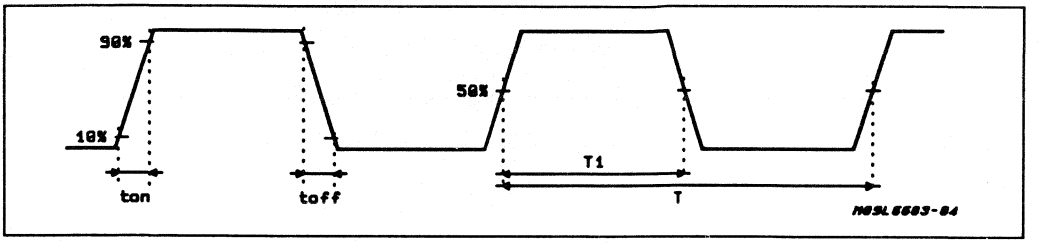


Figure 3: Input for External Clock

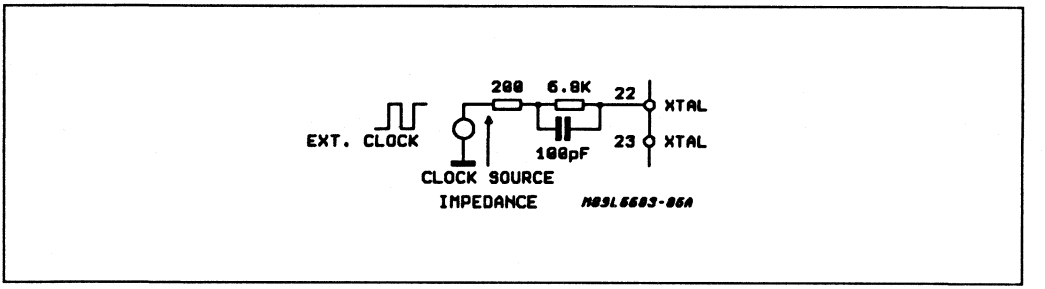
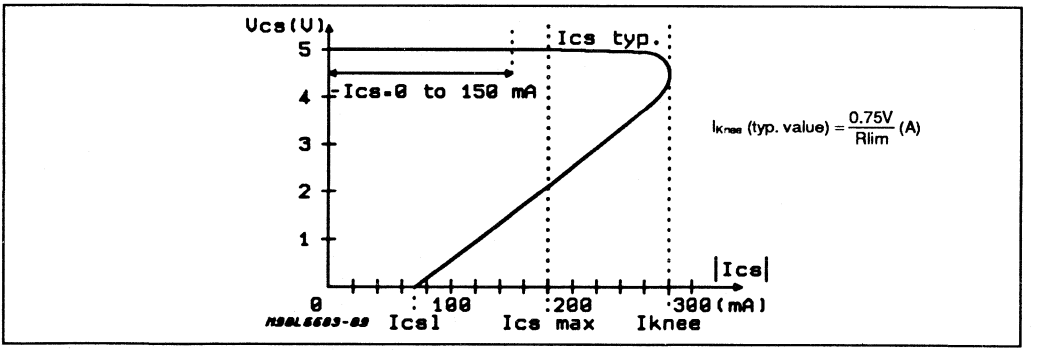


Figure 4

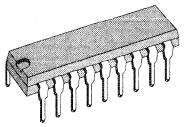


SMART CARD INTERFACE

ADVANCE DATA

- 8 DIFFERENT V_{PP} OUTPUT VOLTAGE LEVELS
- V_{PP}, V_{CS} RISE AND FALL TIME FULL SPEC. WITH ISO/IEC 7816-3
- POWER SUPPLY OUTPUT FOR MEMORY CARD (5V/80mA)
- POWER ON/OFF RESET
- AUTOMATIC SWITCH-OFF OF ALL FUNCTIONS IF THE REGULAR OPERATION IS ABORTED BY EXTRACTING THE SMART CARD
- INTERNAL STATUS FAILURE CODING
  - INSERTION FAILURE CODE
  - OVERTEMPERATURE FAILURE
- ANTI-BOUNCING SYSTEM
- INPUT/OUTPUT LOGIC TTL COMPATIBLE
- THERMAL PROTECTION

MULTIPOWER BCD TECHNOLOGY



Powerdip 12+3+3

DESCRIPTION

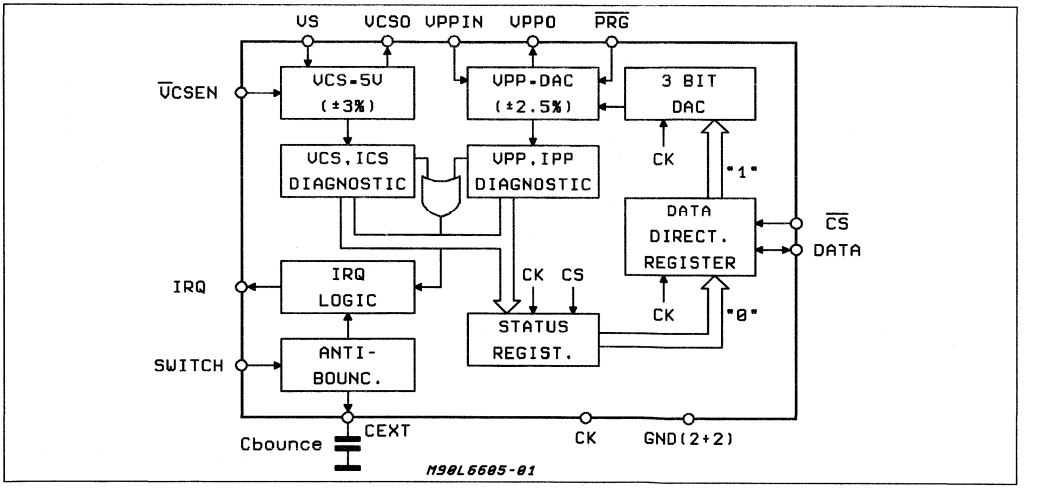
The L6605 is an IC dedicated as intelligent interface between different types of smart cards and microprocessors. The internal architecture can be shared in a power supply section and in a diagnostic parts.

The power supply section can deliver 5V/80mA to supply the card and V_{PP}/50mA to write the memory inside the card; the V_{PP} voltage can be programmed by means of the 3 serial input bit (see TAB, 1).

Table 1: 3 bit DAC CODE

CODE	V_{PP}
0 0 0	5V
0 0 1	10V
0 1 0	12.5V
0 1 1	13.5V
1 0 0	15V
1 0 1	18V
1 1 0	21V
1 1 1	25V

BLOCK DIAGRAM



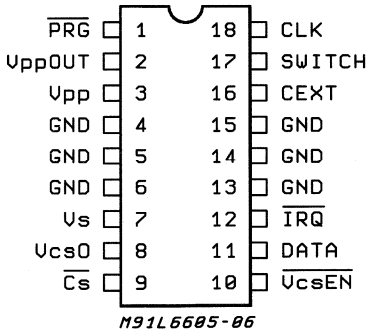
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

DESCRIPTION (continued)
The diagnostic part allows to monitor failures due to overcurrent, overtemperature or wrong card positioning. The failures are internally coded and readable inside the STATUS REGISTER through the bidirectional pin DATA configurated in output. The antibouncing circuitry, active during card insertion only, rejects ripetitive switching-on of the power supply sections.

PIN FUNCTION

Pin	Description
V_S	Input Power Supply voltage for V_{CS} regulated output and for device supply.
V_{CSO}	Output regulated voltage for card supply; I_{CSmax} = 80mA; overload protected (81 to 200mA)
V_{PPIN}	Input power supply for V_{PP} regulated voltage
V_{PPOUT}	Programmable output regulated voltage for memory card writing; 8 voltage levels are allowed by means of 3 bit DAC. I_{PPmax} = 50mA.
$V_{\overline{CSEN}}$	(Active Low) VCS supply input enable; Its value is fixed from the µP allowing or not the normal R/W operations on the card.
SWITCH	Input signal produced by the reader system indicating that a card has been inserted. Internally, an antibounding system is provided to avoid multiple switching.
$\overline{CS}$	Chip select (active low). $\overline{CS}$ low level indicates an I/O operation request from µP.
IRQ	Interrupt Request (Active low). An IRQ low level indicates that a card insertion/extraction or Failure has occured.
$\overline{PRG}$	Program (Active low). $\overline{PRG}$ low level enables L6605 to deliver in output the V_{PPO} level set by 3 bit DAC.
DATA	I/O pin for data exchange between µP and the device. Through this pin flow 3 bit input DAC or 2 bit STATUS REGISTER code.
CK	External clock.
C_{EXT}	Pin to connect an external capacitor for antibouncing delay time.
GND	4 pins to ground.

PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (V_S = 12V; T_j = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10	12	15	V
V_{CS}	Card Supply Voltage (Logic Inputs onset)	I_{CS} = 80mA, V_S = 12V	4.85	5	5.15	V
		I_{CS} = 1mA to 80mA V_S = 10V to 15V $C_{LOAD\ min}$ = 5nF $C_{LOAD\ max}$ = 20µF	4.75	5	5.25	V
I_{CS}	Current Supply Card				80	mA
I_{CSS}	I_{CS} Short Circuit	VS = 12V	81		200	mA
V_{PPI}	V_{PP} Supply Voltage		V_{PPO} + 2.5V		33	V
V_{PPO}	Programming Voltage	I_{PP} = 50mA; V_{PPI} = 30V; $T_{on} \leq$ 5ms	-2.5%	V_{DAC}	+2.5%	V
		I_{PP} = 1mA to 50mA V_{PPI} = max. 33V (see note 1) $C_{LOAD\ min}$ = 5nF $C_{LOAD\ max}$ = 500nF (see note 2)	-5%	V_{DAC}	+5%	V
I_{PP}	Output Program. Current	V_{PPI} = 30V			50	mA
I_{PPS}	I_{PP} Short Circuit		51		150	mA
t_{on}	V_{PP}, Rise Time	$C_{LOAD\ min}$ = 5nF $C_{LOAD\ max}$ = 500nF (see note 2) I_L = 50mA (see note 1)			200	µs
t_{off}	V_{PP}, Fall Time				200	µs
t_{shadow}	Shadow Timing	Cbounce = 0.1µF		1		ms
t_{CKON}	Clock ON Time	C_{LOAD} = 50pF, I_{SINK} = 4mA, V_L = 0.4V	1			µs
t_{CKOFF}	Clock OFF Time		1			µs
t_D	Delay Time		250			ns
$t_{SET-UP1}$	1st bit Set-up Time		500			ns
t_{HOLD1}	1st bit Hold Time		500		t_{CKON}	ns
$t_{SET-UP2}$	Data Set-up Time		500			ns
t_{HOLD2}	Data Hold Time		500			ns
f	Clock Frequency				500	KHz
SR	V_{PP} Slew Rate	From rest state to programming state and viceversa			2	V/µs
V_{STH}	Power ON/OFF Threshold	Logic inputs onset		8.5	9.5	V
V_{SHY}	V_{STH} Hysteresis			0.6		V
T_S	Thermal Shutdown			180		°C
T_H	Thermal Hysteresis			20		°C

Note 1: True for values in Tab. 1 only. ; **Note 2:** Values higher than 500nF are permitted, but the ton, toff timing will be out ISO norm.

CIRCUIT OPERATION

CARD POWER SUPPLY

Regulated voltage to supply the card (5V/80mA). During nominal condition (VS = 12V, ICS = 80mA) the VCS range variation is equal to æ 3%. While during line/load variation (VS = 10V to 15V; ICS = 1mA to 80mA) the VCS range is æ 5%.
An internal circuitry checks the ICS level; the protection block activates an IRQ with the proper failure code when the output current is in 81mA to 200mA range.

PROGRAMMING POWER SUPPLY

L6605 works in step-down mode by means of the programmed output voltage V_{PP}. 8V_{PP} levels can be selected programming the 3 bit DAC as per Table 1. During nominal conditions (I_{PP} = 50mA; V_{PPI} = 30V) the V_{PP} range variation is equal to ±2.5%; while during line/load variation (I_{PP} = 1mA to 50mA; V_{PPI} = max. 33V) the V_{PP} range is ±5%. An internal circuitry checks the I_{PP} level; the protection block activates an IRQ with the proper failure code when the output current is in 51mA to 150mA range. Under the power ON/OFF

threshold value the logic section and the power supply regulators are disabled.

LOGIC SECTION
L6605 includes a logic circuitry in order to protect, both card and itself. If a failure occours an asynchronous IRQ is sent to the µP; consequently the µP forces low CS signal as I/O request. After CS variation the µP sends also one "data direction bit" into DATA DIRECTION REGISTER.

- Direction bit = "0"
  Pin DATA is configurated in output and the µP reads the 2 bit STATUS REGISTER content

Code	1st bit	2nd bit
0	No insertion	No Failure
1	Card Inserted	Failure

Failure could be overtemperature over the 2 regulators (VPP, VCS).

- Direction bit = "1"
  Pin DATA is configurated in input to allow the 3 bit DAC loading and than the programming of V_{PPo} output level voltage. (see Table 1).

During card insertion only resing edge of switch signal is detected , while during card extraction switch level is detected.

In card extraction mode if occours a mechanical switch bouncing, which causes a pulse on SWITCH input pin with duration t ≥ 50µs the L6605 will have the 1st Status Register content equal to "0" and 1 ms t_{shadow} timing like during card insertion mode.
Bouncing on SWITCH pin with duration T<50µs will be transparent in the Status Register .

Figure 1: Card Insertion

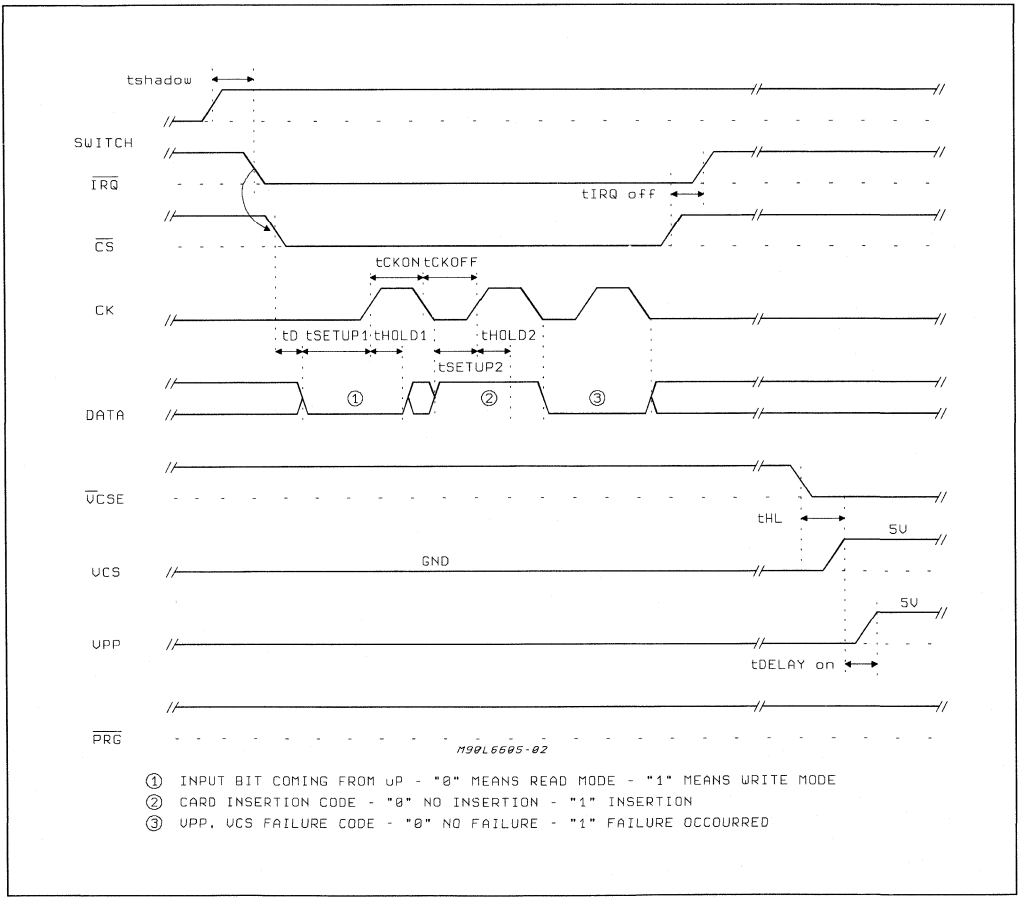
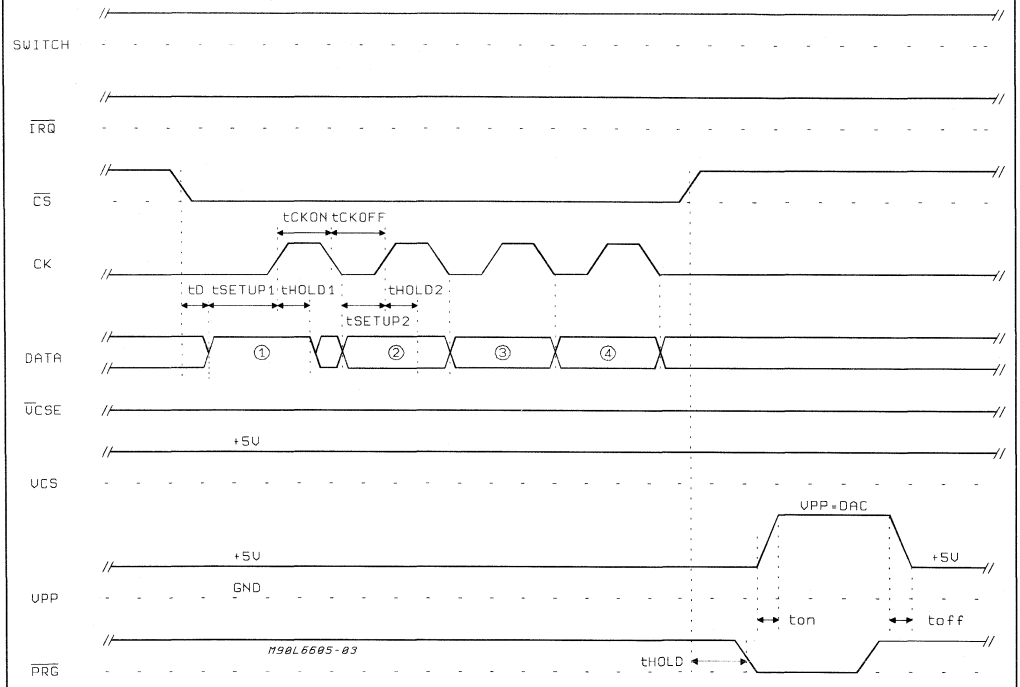
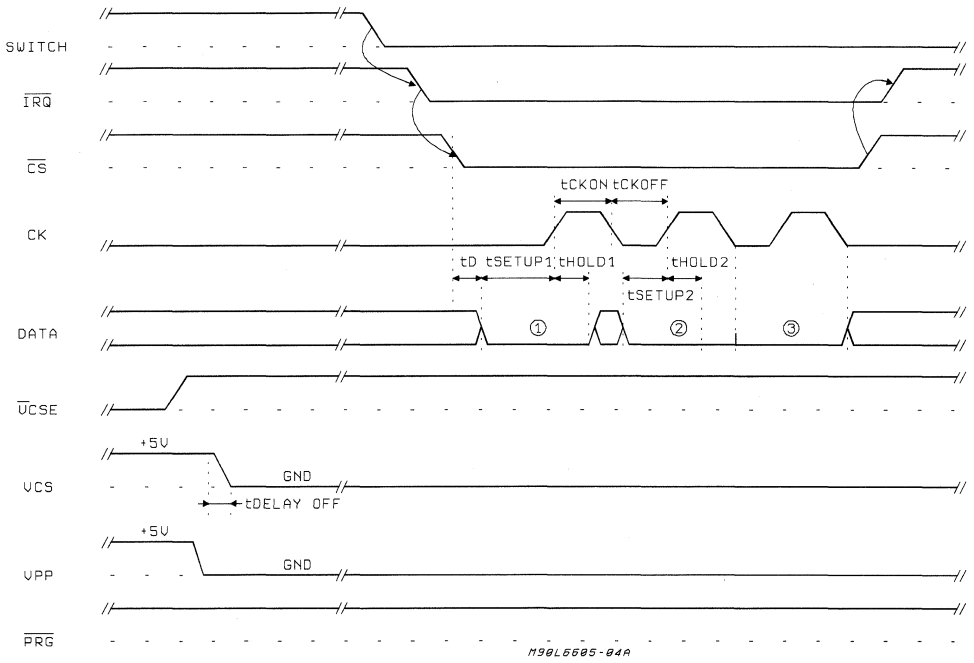


Figure 2: DAC Loading and Programmed Voltage on Set



① INPUT BIT COMING FROM uP - "0" MEANS READ MODE - "1" MEANS WRITE MODE
② 1st BIT DAC
③ 2nd BIT DAC
④ 3th BIT DAC

Figure 3: End Normal Operation



① INPUT BIT COMING FROM uP - "0" MEANS READ MODE - "1" MEANS WRITE MODE
② CARD INSERTION CODE - "0" NO INSERTION - "1" INSERTION
③ VPP, VCS FAILURE CODE - "0" NO FAILURE - "1" FAILURE

Figure 4.

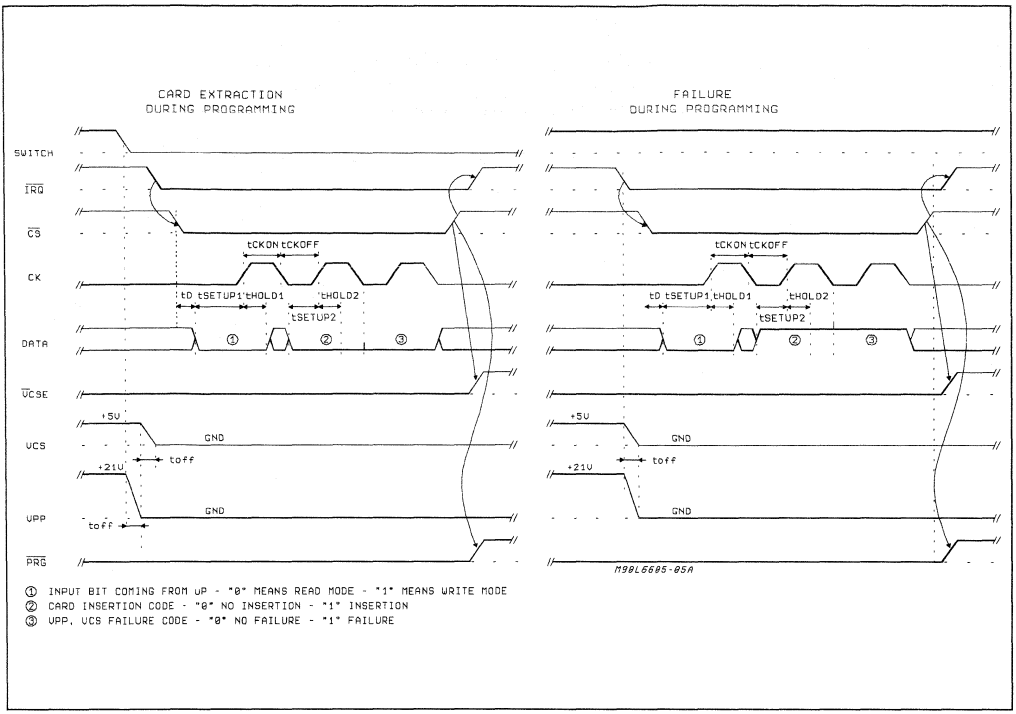
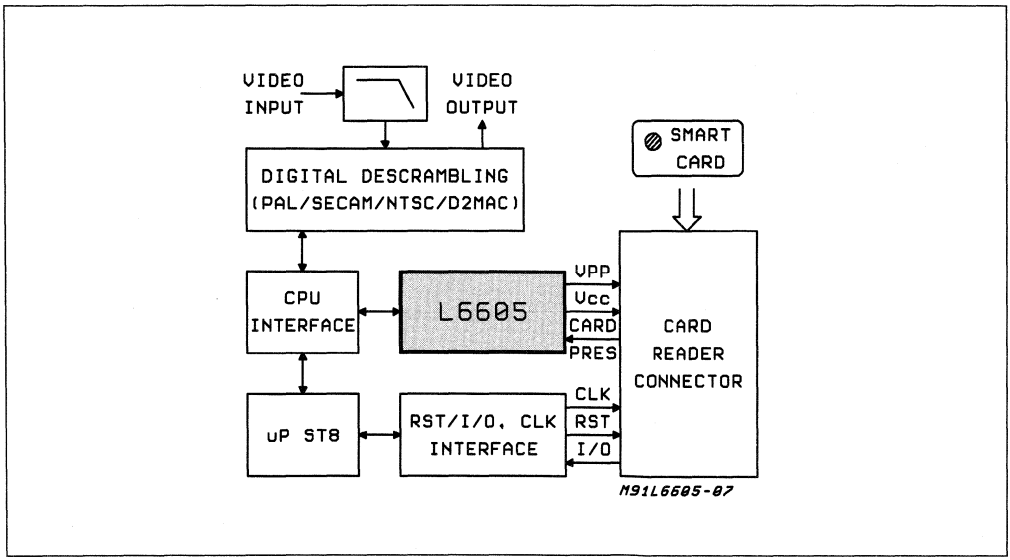


Figure 5: PAY-TV Application



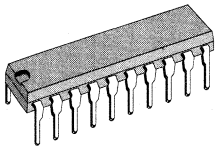
SGS-THOMSON MICROELECTRONICS

L6720
L6721

MINITEL INTERFACE

ADVANCE DATA

- ONE NON INVERTING LINE DRIVER
- ONE NON INVERTING LINE RECEIVER
- LINE TRANSCEIVER: (TOWARDS PERIPHERALS)
  - non inverter from Minitel to peripherals
  - inverter from peripherals to Minitel
- POWER SUPPLY
  - not regolated output voltage
  - internal low drop power switch with antisaturation circuit
  - output protected against short circuit
  - standby mode operation with an external signal
- AUDIO AMPLIFIER
  - one input, one output
  - one pin for supply rejection
  - internal fixed gain
- THERMAL SHUTDOWN



Powerdip 16+2+2

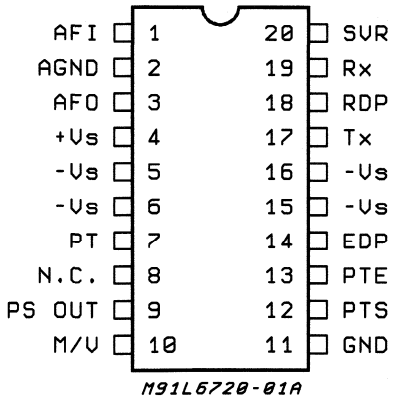
ORDERING NUMERS: L6720
L6721

DESCRIPTION

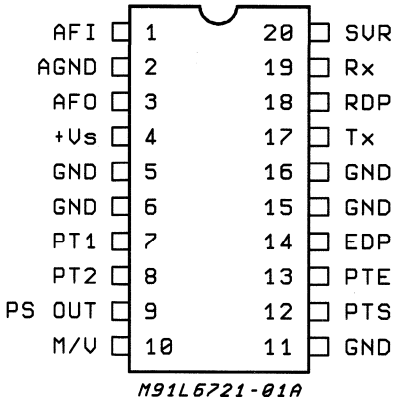
This device performs the functions of a complete interface for Minitel peripheral plug.

It integrates one line driver, one line receiver, one line transceiver, a power supply for peripherals, and an audio amplifier, Two version are provided:
- L6720 which needs a negative supply.
- L6721 which doesn't use a negative supply.

PIN CONNECTIONS



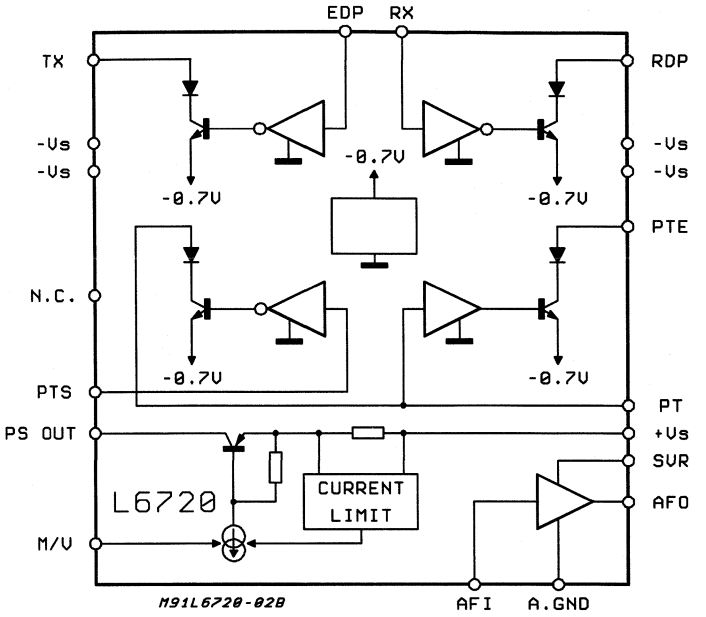
L6720

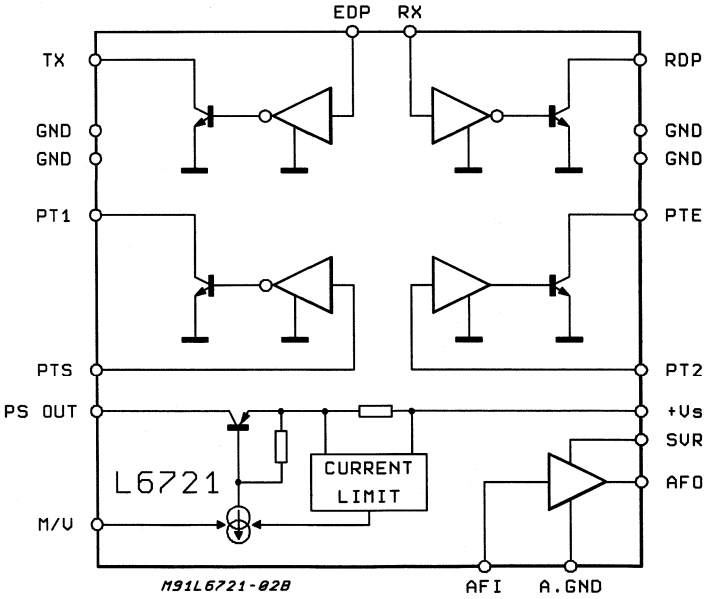


L6721

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
$+V_S$,(V_S)	Positive Supply Voltage	+15	V
$-V_S$	Negative Supply Voltage	-13	V
V_{OC}	Open Collectors Voltage	max 20	V
I_{OC}	Open Collectors Current	max 10	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	1.25	W
T_J	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

THERMAL DATA

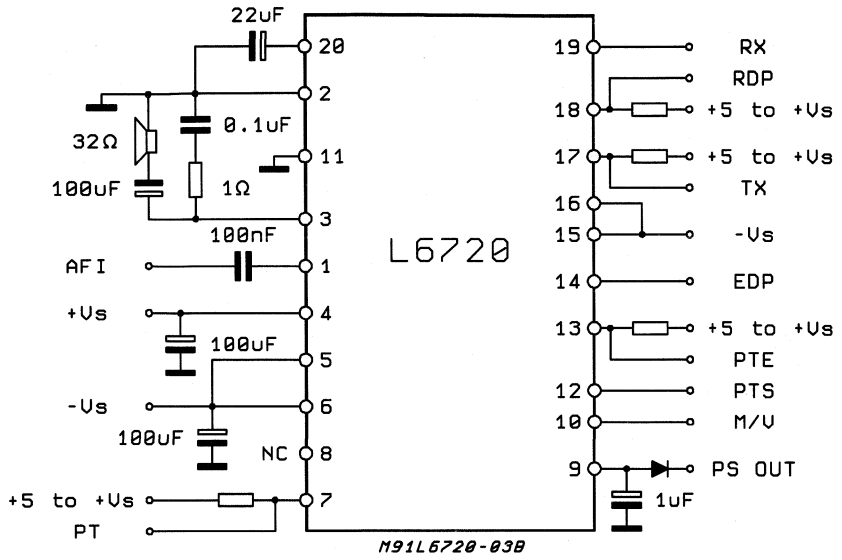
Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	(*)65	°C/W

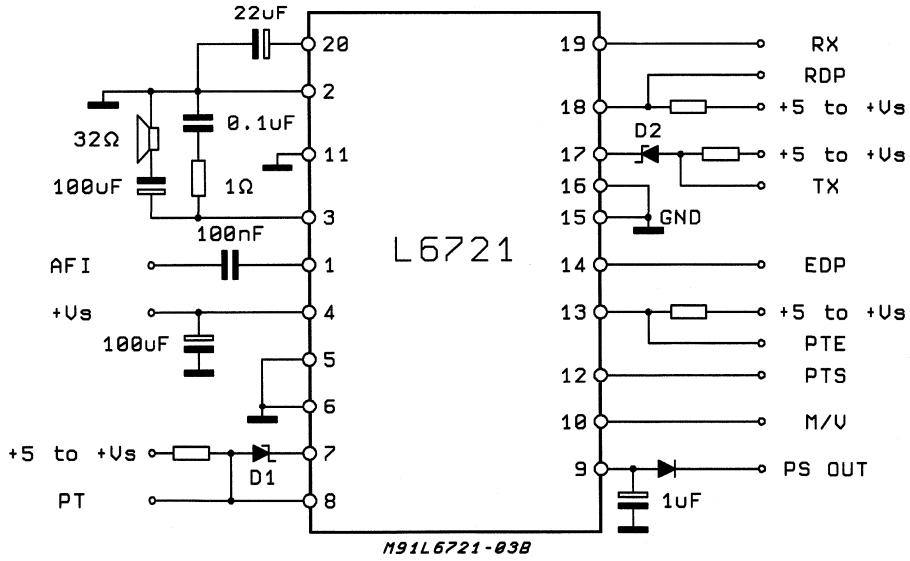
(*) Mounted on board with minimized dissipating copper area

PIN FUNCTIONS

Pin	Name	Function
1	AFI	Audio Frequency input
2	AGND	Audio Amplifier Ground
3	AFO	Audio amplifier output
4	$+V_S$,(V_S)	Power Supply Input (to plug)
5	$-V_S$,(GND)	Negative Supply (GND for L6721)
6	$-V_S$,(GND)	Negative Supply (GND for L6721)
7	PT	Transceiver Input/Output (L6720)
8	N.C.	Not Connected (L6720)
7	PT1	Transceiver Output (to plug) (L6721)
8	PT2	Transceiver Input (from plug) (L6721)
9	PSout	Power Supply Output (to plug)
10	M/V	Inhibition of peripheral output power
11	GND	Ground pin
12	PTS	Line Transceiver Input (from Minitel)
13	PTE	Line Transceiver Output (to Minitel)
14	EDP	Line Driver Input (from Minitel)
15	$-V_S$,(GND)	Negative Supply (GND for L6721)
16	$-V_S$,(GND)	Negative Supply (GND for L6721)
17	T_X	Line Driver Output (to plug)
18	RDP	Line Receiver Output (to Minitel)
19	R_X	Line Receiver Input
20	SVR	Supply Voltage Rejection

APPLICATION DIAGRAMS





D1-D2: SCHOTTKY VF ≤ 0.3V at 10mA
VR = 20Vmin

ELECTRICAL CHARACTERISTICS

I) LINE DRIVER, LINE RECEIVER, LINE TRANCEIVER

L6720: with negative supply

Test Conditions: 10V < $+V_S$ < 12V, -8V <- V_S < -4V, T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT	Pins V_S and $-V_S$ open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time			1		µs

L6721: without negative supply

Test Conditions: 10V < V_S < 12V, T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT2)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT2)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT2		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT2	Pins V_S and GND open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT1)	I_{LOAD} = 6mA			0.15	V
V_{OL}	Output Low Level (pins RDP, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PT1, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time	I_{LOAD} = 6mA C_{out} = 50pF		1		µs

II) POWER SUPPLY

L6720: $+V_S$ = 12V, $-V_S$ = -8V
L6721: V_S = 12V
T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_I - V_O	Dropout Voltage	I_{LOAD} = 1A		0.4	0.8	V
I_{SC}	Short Circuit Current		1	1.1	1.2	A
M/V_L	Low Level Disable Pin (1)				0.8	V
M/V_H	High Level Disable Pin (1)		2			V
I_L	Disable Pin Input Current	M/V = 0			100	µA
I_Q	Quiescent Current	I_{LOAD} = 1A I_{LOAD} = 0.25A			60 23	mA mA

Note (1) Power supply is disabled when a zero level voltage is applied on M/V Pin

III) AUDIO AMPLIFIER (2)

L6720: $+V_S$ = 12V, $-V_S$ = -8V
L6721: V_S = 12V
T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_i	Input Impedance		20			KΩ
AV	Voltage Gain		28	30	32	dB
BW	Bandwidth		10			KHz
P_O	Output Power	Distortion = 10%, f = 1KHz R_{LOAD} = 32Ω, 10V < V_{CC} < 14V	250			mW

Note (2): The output of the audio amplifier is protected against short circuits toward positive power supply and ground

IV) PROTECTIONS

1) L6720 (With negative supply)

Pins Rx, Tx, PT are protected against any DC voltage ranging from -18V to +18V, with the device supplied or not, without extra components.

2) L6721 (Without negative supply)

Pins Tx, PT1 are not protected: an external schottky diode must be added to protect them from -18V to +18V (see application diagram).
Pins Rx, PT2 are protected against any DC voltage ranging from -18V to +18V.

3) In Both Options

P. Supply pin is not protected: an external diode must be inserted to protect it (see application diagram).
The suggested electrical characteristic of the external diode are:

- $V_{REVERSE}$ > 20V
- Voltage drop at 1A max. 1.2V

4) Thermal Protection

This protection is operating when the chip temperature typically raises above 150°C (hysteresis 20°C Typ; this indicated value is valid with the application circuit on pag. 4), turning off both the power switch and the audio amplifier.

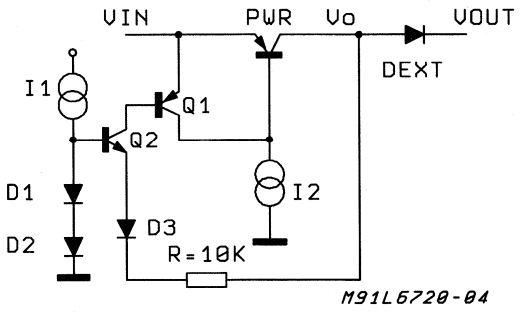
APPLICATION INFORMATION

The external diode on the output of the power switch has the fundamental function of protecting this pin against positive overvoltages.

However the voltage drop on this diode is also important in the correct definition of the thermal hysteresis. This can be understood by considering the circuit applied on the output of the power switch, which has the function of withstanding negative overvoltages.

Let's refer to fig. 1:

Figure 1



D_{EXT}: EXTERNAL DIODE; PWR: POWER TRANSISTOR; I_1, I_2: CURRENT GENERATORS; R: RESISTANCE; D1, D2, D3: DIODES; Q1, Q2: SIGNAL TRANSISTORS

When V_{OUT} = 0.7V Q2 and D3 turn on and also Q1 whose saturation turns off the power PWR. In this condition (BV_{CBO}) it can withstand the maximum negative overvoltage (-18V).

If we now have an overload on V_{OUT} (after the diode) for example with V_{IN} = 12V, V_{OUT} = 8V, P_d = 4W, the temperature of the chip increases to the thermal shutdown intervention, so that V_{OUT} = 0. However Q1 and Q2 cannot turn on because we have 2 diodes (D1 and D2) against 3 diodes (D3, D_{EXT}, Base-Emitter of Q2).
If the over load is on point V_O (before the external diode) as before the chip temperature increases until shutdown. But in that condition (with V_{OUT} = 0) we have now 2 diodes (D1, D2) against other 2 diodes (D3, Q2 Base-Emitter); than the power switch doesn't turn on because of a slight difference between the thermal coefficient of the 4 diodes.

We will have the new switching-on of power switch only when the chip temperature decreases of about 80°C (being kept off by Q1 and Q2).

In conclusion with or without the external diode the absolute value of the thermal shutdown is the same, but the hysteresis is higher without the external diode.

THERMAL CHARACTERISTICS

The transient thermal resistance of the 16+2+2 powerdip package is shown in Fig. 2: a typical $R_{th\ j\text{-}amb}$ of 50° C/W roughly can be seen.To be able to well sink out the heast from the inside of the package, the four control pins can be closely connected to a p.c.b. copper side. By considering the two square sides of Fig. 4, the thermal resistance junction-ambient can be reduced according to Fig. 3.

Figure 2: DIP 16+2+2 Transient Thermal Resistance for single pulses.

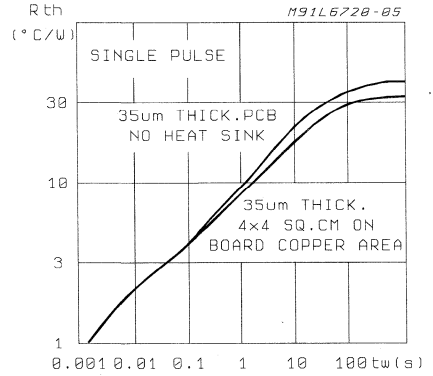


Figure 3: Typical R_{th} j-a of Powerdip 16+2+2 vs side 1 for heat sink on the PCB lower side.

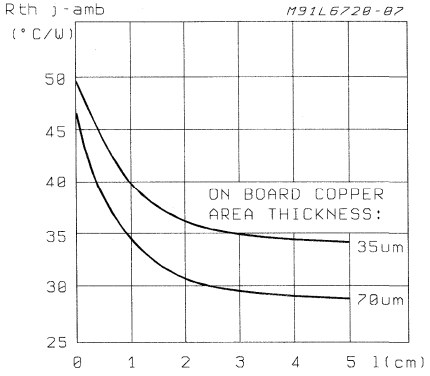
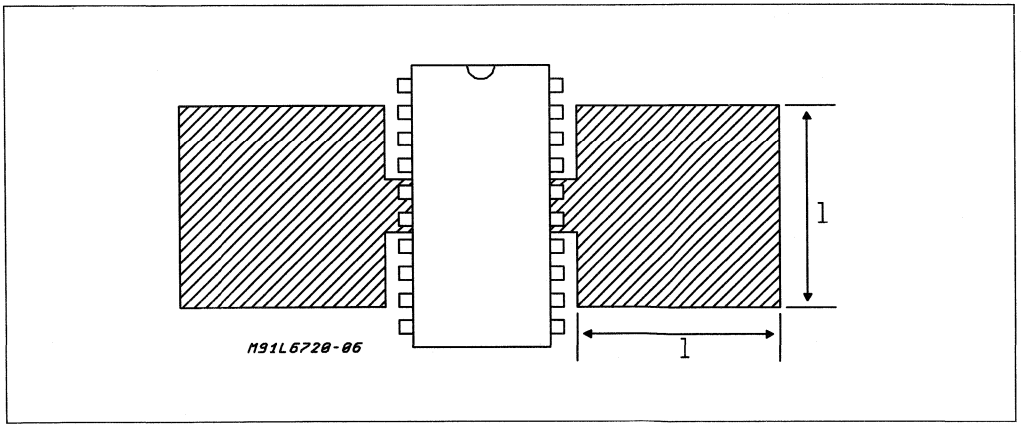


Figure 4: Two "On Board" square heat sink

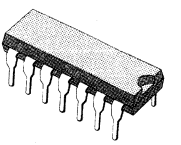


SGS-THOMSON MICROELECTRONICS

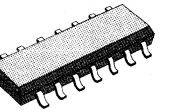
MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10 mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300 ΩMIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE



DIP-14 (0.25)
(Plastic and Ceramic)



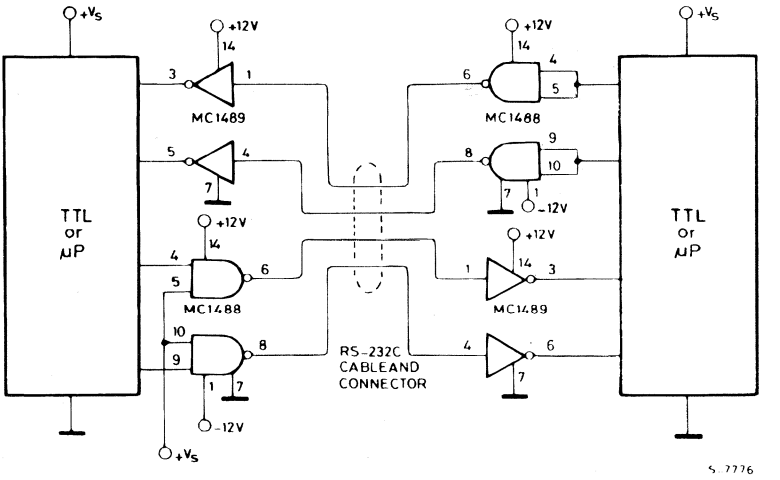
SO-14J

ORDER CODES : MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

DESCRIPTION

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.

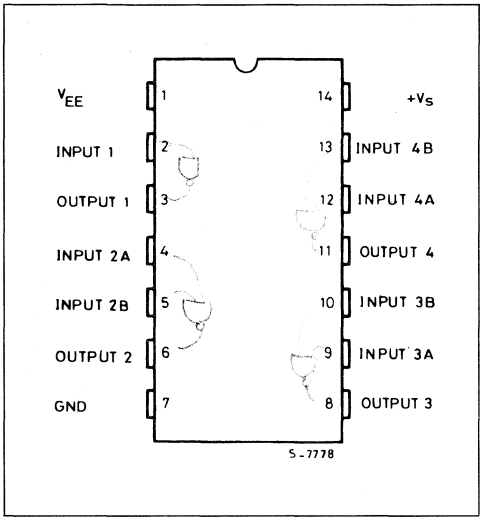
TYPICAL APPLICATION : RS232C Data Transmission.



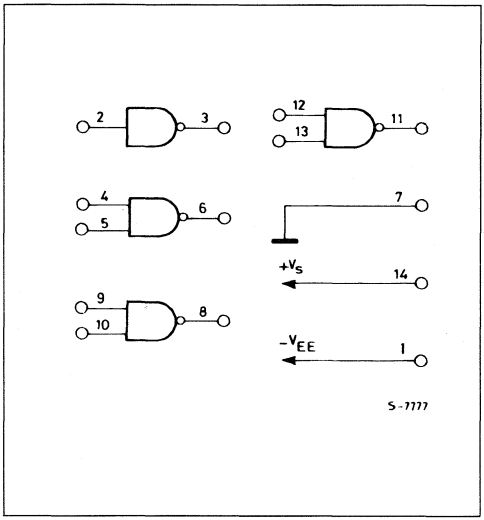
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	15	V
V_{EE}	Power Supply Voltage	− 15	V
V_{IR}	Input Voltage Range	$-15 \leq V_{IR} \leq 7$	V
V_O	Output Signal Voltage	± 15	V
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	− 65 to 150	°C

CONNECTION DIAGRAMS (top views)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP - 14	Ceramic DIP - 14	SO - 14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	200 °C/W	165 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (V_S= 9 ±10 % V, V_{EE}= − 9 ±10 % V, T_{amb}= 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL}	Input Current	Low Logic State (V_{IL} = 0V)		1	1.6	mA	1
I_{IH}	Input Current	High Logic State (V_{IH} = 5V)			10	µA	1
V_{OH}	Output Voltage	High Logic State R_L= 3KΩ V_{IL} = 0.8V, V_S = 9V, V_{EE} = –9V V_{IL} = 0.8V, V_S = 13.2V, V_{EE} = –13.2V	 6 9	 7 10.5	 	 V V	 2 2
V_{OL}	Output Voltage	Low Logic State R_L = 3 KΩ V_{IH} = 1.9V, V_{EE} = –9V, V_S = 9V V_{IH} = 1.9V, V_{EE} = –13.2V, V_S = 13.2V	 – 6 – 9	 – 7 – 10.5	 	 V V	 2 2
I_{OS+} *	Positive Output Short - circuit Current		6	10	12	mA	3
I_{OS-} *	Negative Output Short-circuit Current		– 6	– 10	– 12	mA	3
R_O	Output Resistance	V_S = V_{EE} = 0 |Vo| = ± 2V	300			Ω	4
I_s	Positive Supply Current (R_i = ∞)	V_{IH} = 1.9 V V_S = 9 V V_{IL} = 0.8 V V_S = 9 V V_{IH} = 1.9 V V_S = 12 V V_{IL} = 0.8 V V_S = 12 V V_{IH} = 1.9 V V_S = 15 V V_{IL} = 0.8 V V_S = 15 V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative Supply Current (R_L = ∞)	V_{IH} = 1.9 V V_{EE} = – 9 V V_{IL} = 0.8 V V_{EE} = – 9 V V_{IH} = 1.9 V V_{EE} = – 12 V V_{IL} = 0.8 V V_{EE} = – 12 V V_{IH} = 1.9 V V_{EE} = – 15 V V_{IL} = 0.8 V V_{EE} = – 15 V		– 13 – 18 	– 17 – 15 – 23 – 15 – 34 – 2.5	mA µA mA µA mA mA	5
P_c	Power Consumption	V_S = 9 V V_{EE} = – 9 V V_S = 12 V V_{EE} = – 12 V			333 567	mW	

SWITCHING CHARACTERISTICS (V_S = ± 9 ±1 % V, V_{EE} = – 9 ± 1 % V, T_{amb} = 25 °C)

t_{PLH}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		275	350	ns	6
t_{THL}	Fall Time	Z_i = 3 KΩ and 15 pF		45	75	ns	6
t_{PHL}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		110	175	ns	6
t_{TLH}	Rise Time	Z_i = 3 KΩ and 15 pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Figure 1 : Input Current.

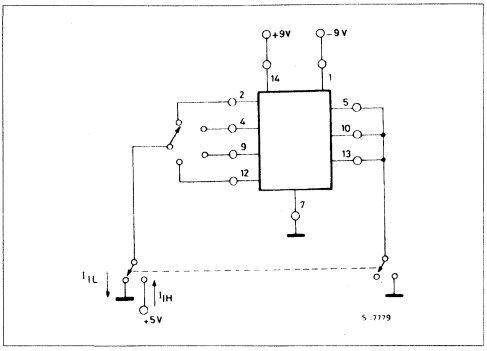


Figure 2 : Output Voltage.

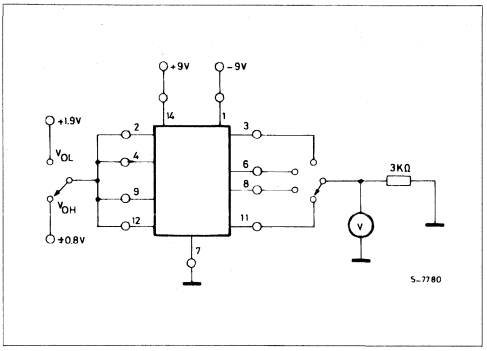


Figure 3 : Output Short-Circuit Current.

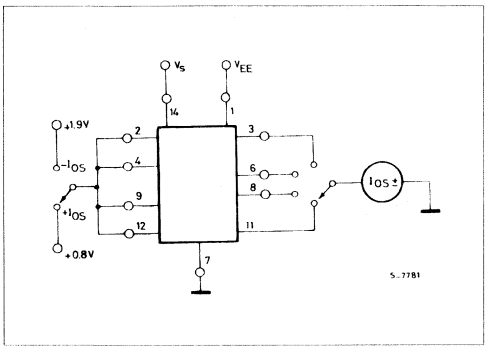


Figure 4 : Output Resistance (power off).

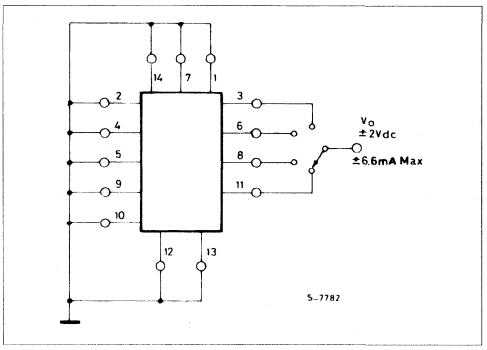


Figure 5 : Power Supply Currents.

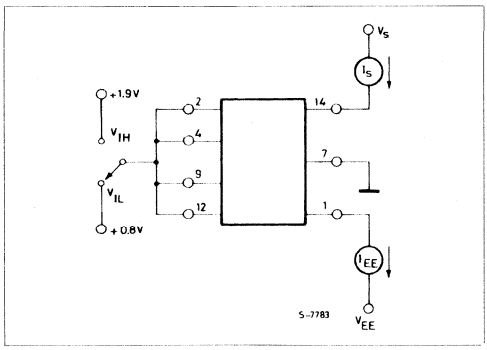


Figure 6 : Switching Response.

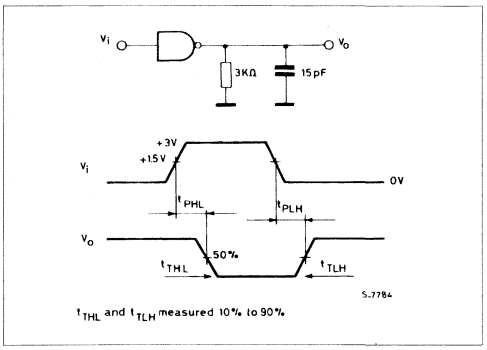


Figure 7 : Transfer Characteristics vs. Power Supply Voltage.

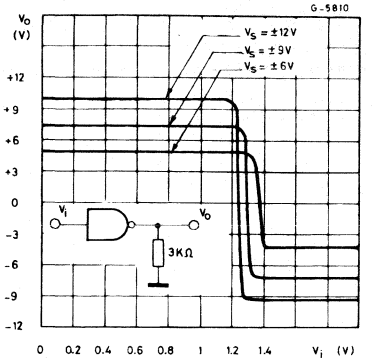


Figure 8 : Short-Circuit Output Current vs. Temperature.

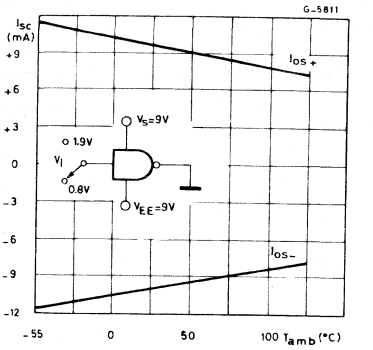


Figure 9 : Output Slew-Rate Load Capacitance.

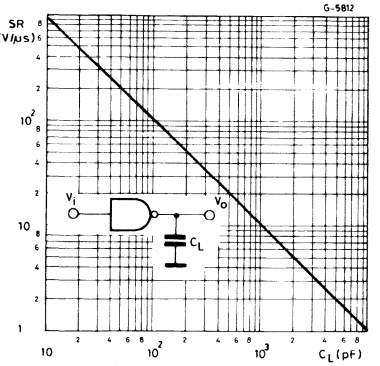


Figure 10 : Output Voltage and Current-Limiting Characteristics.

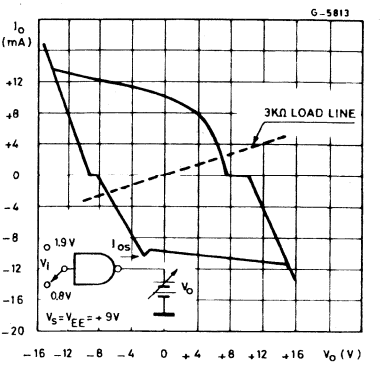
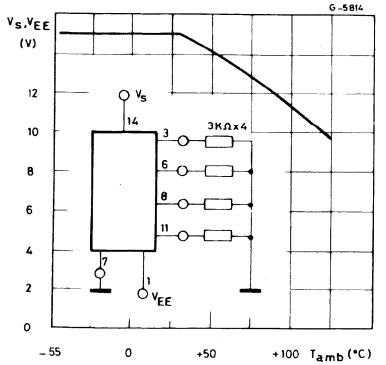


Figure 11 : Maximum Operating Temperature vs. Power-Supply Voltage.



APPLICATION INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15 V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 V per µs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per µs.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 V (i.e., $V_S \geq 9.0$ V ; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-suppies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±15 V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Figure 12 : Slew Rate vs. Capacitance for I_{SC} = 10mA.

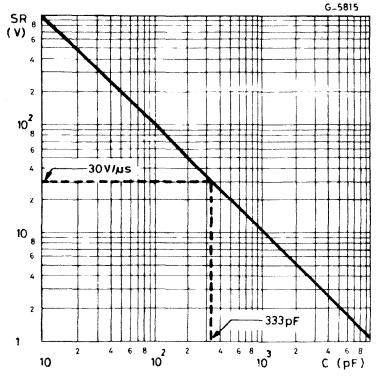
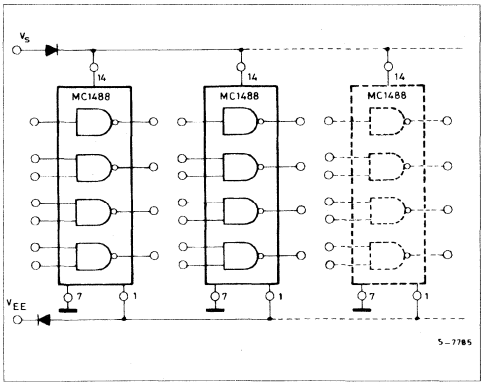


Figure 13 : Power Supply Protection to Meet Power-off Fault Conditions.



OTHER APPLICATION

The MC1488 is an extremely versatile line driver with a miriad of possible applications. Several features of the drivers enhance this versatility :

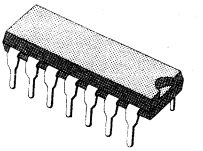
1. Output Current Limiting - this enables the circuit designer to define the ouptut voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.

2. Power-Supply Range - as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can very from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately - 2.5 V to the minimum specified - 15 V. The MC1488 will drive the ouptut to within 2 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.

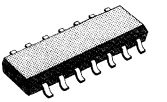
MC1489
MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE –3.0 K to 7.0 KΩ
- INPUT SIGNAL RANGE – ± 30 V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL :
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING



DIP-14
(Plastic (0.25) and Ceramic)



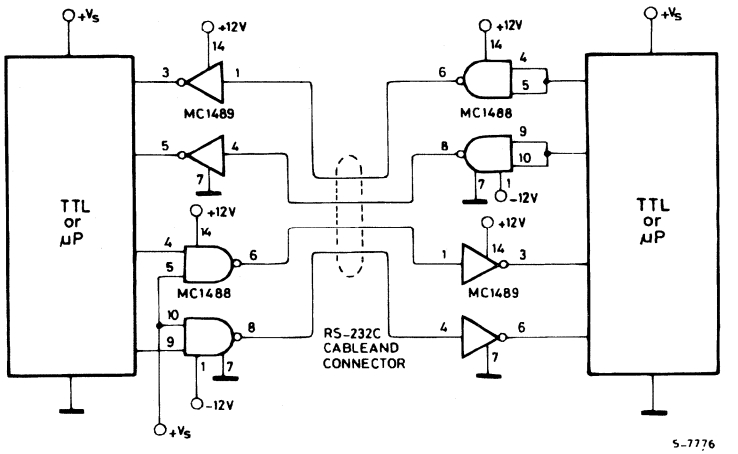
SO-14J

ORDER CODES : MC1489L, MC1489AL
(DIP–14 Ceramic)
MC1489P, MC1489AP
(DIP–14 Plastic)
MC1489D, MC1489AD (SO-14)

DESCRIPTION

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

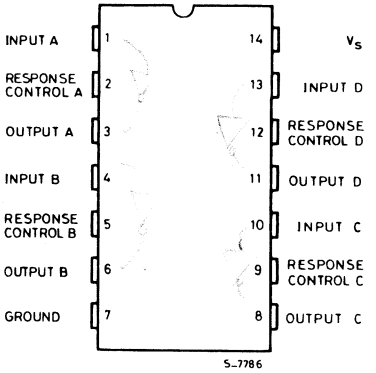
TYPICAL APPLICATION : RS232C Data Transmission



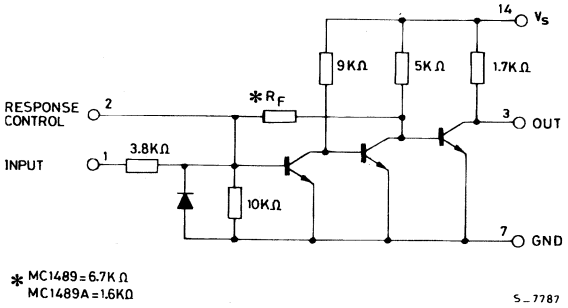
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	10	V
V_I	Input Voltage Range	± 30	V
I_{OL}	Output Load Current	20	mA
P_{tot}	Power Dissipation	1	W
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

CONNECTION DIAGRAMS (top view)



SCHEMATIC DIAGRAM (1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS (Response control pin is open V_S = 5 V (± 10%) T_{amb} = 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3 V	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = − 25 V V_{IL} = − 3 V	− 3.6 − 0.43		− 8.3	mA
V_{IH}	Input Turn-on Threshold Voltage	T_{amb} = 25 ° C V_{OL} ≤ 0.45 I_L = 10 mA for **MC1489** for **MC1489A**	1 1.75	 1.95	1.5 2.25	V
V_{IL}	Input Turn-off Threshold Voltage	T_{amb} = 25 ° C V_{OH} ≥ 2.5 V I_L = − 0.5 mA	0.75		1.25	V
V_{OH}	Ouptut Voltage High	V_{IH} = 0.75 V I_L = − 0.5 mA I_L = 0.5 mA Input Open Circuit	2.5 2.5	4 4	5 5	V V
V_{OL}	Output Voltage Low	V_{IL} = 3 V I_L = 10 mA		0.2	0.45	V
I_{OS}	Output Short Circuit Current			− 3	− 4	mA
I_{CC}	Power Supply Current	All gates "on" I_O = 0 mA V_{IH} = 5 V		16	26	mA
P_C	Power Consumption	V_{IH} = 5 V		80	130	mW

SWITCHING CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 ° C, see Fig. 1)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay Time	R_L = 3.9 KΩ		25	85	ns
t_{TLH}	Rise Time	R_L = 3.9 KΩ		120	175	ns
t_{PHL}	Propagation Delay Time	R_L = 390 Ω		25	50	ns
t_{THL}	Fall Time	R_L = 390 Ω		10	20	ns

TEST CIRCUITS

Figure 1 : Switching Response.

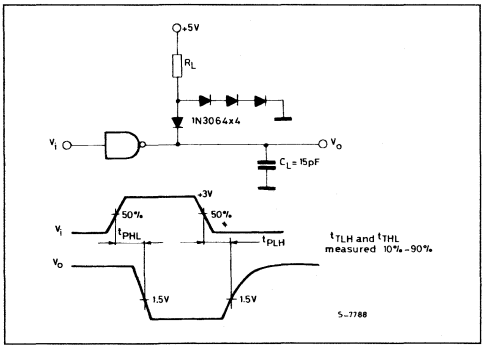
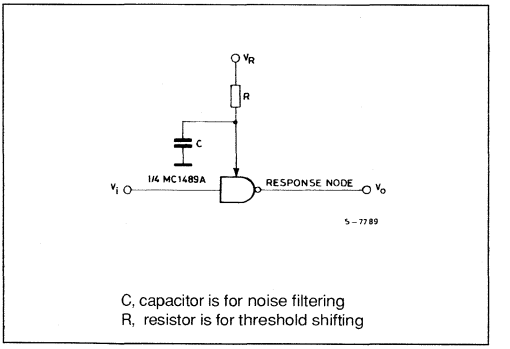


Figure 2 : Response Control Node.



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Figure 3 : Input Current.

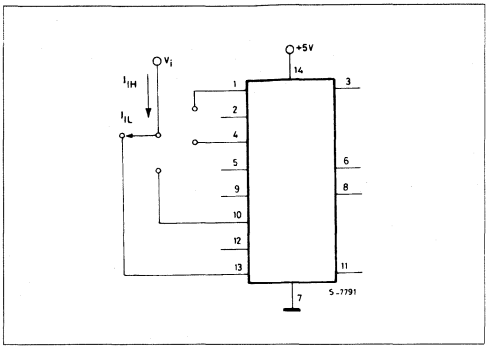


Figure 4 : Output Short-Circuit Current.

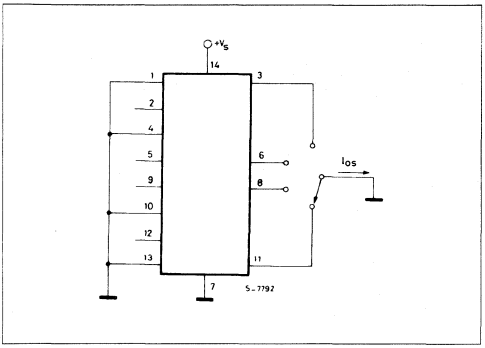


Figure 5 : Output Voltage and Input Threshold Voltage.

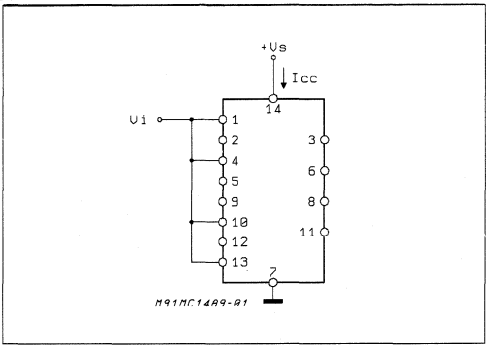
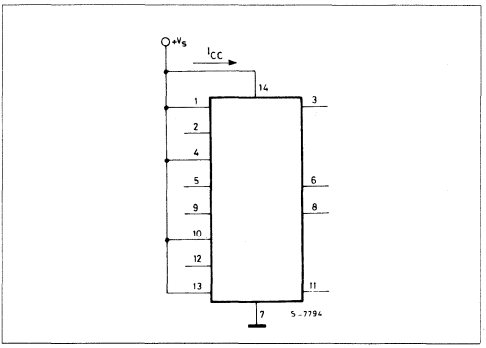


Figure 6 : Power Supply Current.



TYPICAL CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C unless otherwise specified)

Figure 7 : Input Current.

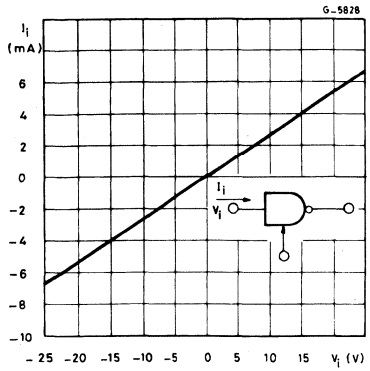


Figure 8 : MC1489 Input Threshold Voltage Adjustament.

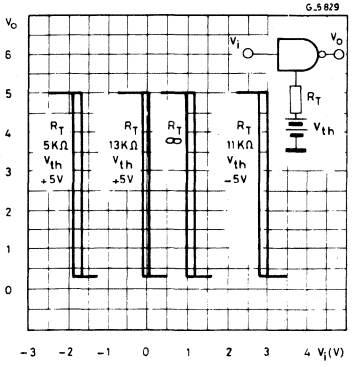


Figure 9 : MC1489A Input Threshold Voltage Adjustment.

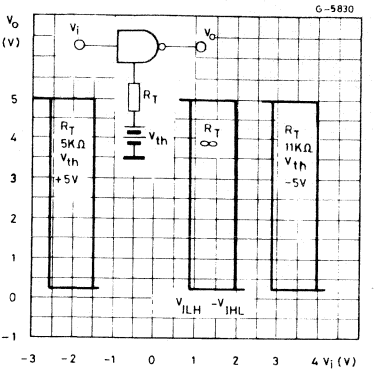


Figure 10 : Input Threshold Voltage vs. Temperature.

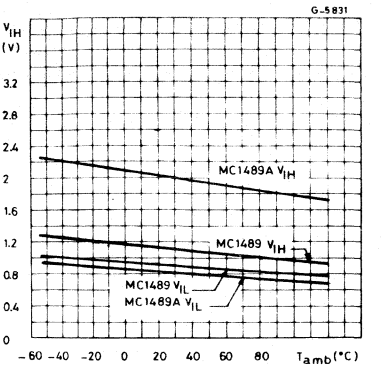
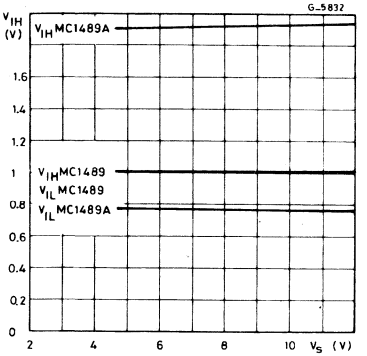


Figure 11 : Input Threshold vs. Power-Supply Voltage.



APPLICATION INFORMATION

GENERAL INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude ; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between - 3.0 and - 25 V as a Logic "1" and inputs between + 3.0 and + 2.5 V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For the reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

DEVICE CHARACTERISTICS

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of the high-frequency, high-energy noise pulses. Figure 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for may combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropiate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Figure 12 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

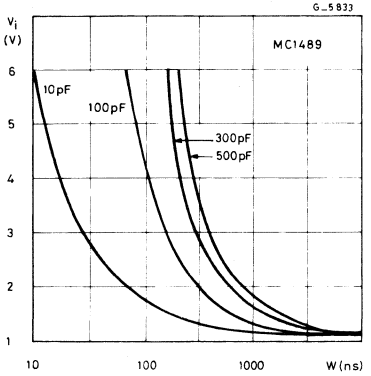


Figure 13 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

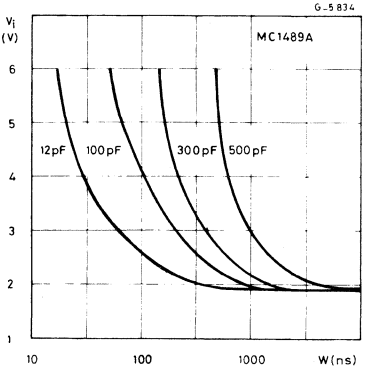
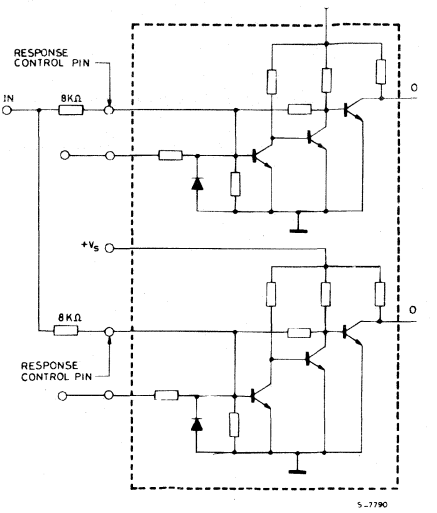


Figure 14: Typical Paralleling of Two MC1489/A Receivers to Meet RS-232C.

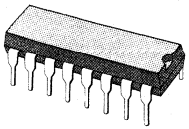


SGS-THOMSON MICROELECTRONICS

MC3479C

STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION + 7.2 V TO + 16 V
- 350 mA/ COIL DRIVE CAPABILITY
- BUILT IN FAST PROTECTION DIODES
- SELECTABLE $\overline{CW}$/CCW AND $\overline{FULL}$/HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS : 250 mV TYP.
- $\overline{PHASE}$ LOGIC CAN BE INITIALIZED TO $\overline{PHASE\ A}$
- $\overline{PHASE\ A}$ OUTPUT DRIVE STATE INDICATION



Powerdip
12 + 2 + 2

ORDER CODE : MC3479C

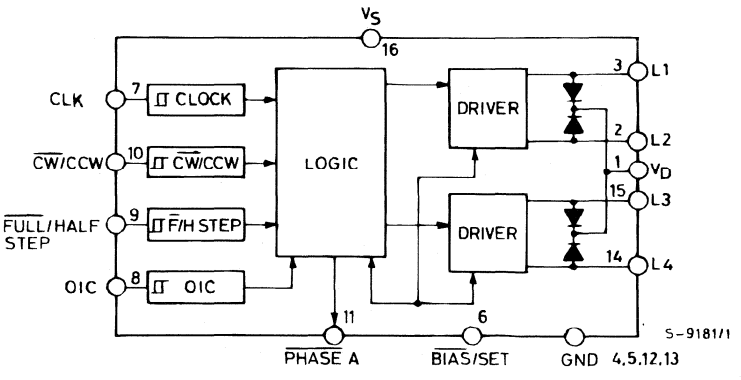
DESCRIPTION

The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.

INPUT TRUTH TABLE

	INPUT LOW	INPUT HIGH
CW/CCW	CW	CCW
F/HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	

BLOCK DIAGRAM



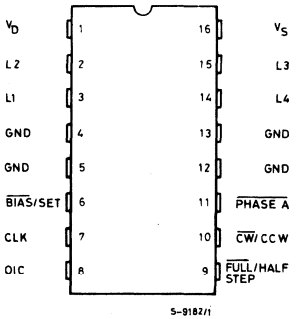
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V_{DC}
V_D	Clamp Diode Cathode Voltage (pin 1)	V_S	V_{DC}
V_{OD}	Driver Output Voltage (pins 2, 3, 14, 15)	V_S	V_{DC}
I_{OD-}	Driver Output Current/Coil	± 500	mA
V_{IN}	Input Voltage (pins 7, 8, 9, 10)	– 0.5 to 7	V_{DC}
I_{BS}	$\overline{\text{Bias/Set}}$ Current (pin 6)	10	mA
V_{OA}	$\overline{\text{Phase A}}$ Output Voltage (pin 11)	16	V_{DC}
I_{OA}	$\overline{\text{Phase A}}$ Sink Current (pin 11)	20	mA
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature range	– 55 to 150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage (DC)	7.2	16	V
V_D	Clamp Diode Cathode Voltage (DC)	–	V_S	V
I_{OD}	Driver Output Current (per coil)	–	350	mA
V_I	DC Input Voltage (pin 7, 8, 9, 10)	0	5.5	V
I_{BS}	$\overline{\text{Bias/Set}}$ Current (outputs active)	– 300	75	µA
I_{OA}	$\overline{\text{Phase A}}$ Sink Current	0	8	mA
T_{amb}	Operating Ambient Temperature	0	70	°C

CONNECTION DIAGRAMS



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

PIN DESCRIPTION

Symbol	Name	Pins	Description
V_S	POWER SUPPLY	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2 V to 16 V.
GND	GROUND	4-5-12-13	Ground Pins for the Logic Circuit and the Motor Coil Current. The physical configuration of the pins dissipating heat from within the package.
V_D	CLAMP DIODE	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and pin 16. See figure 5.
L1, L2, L3, L4	DRIVER OUTPUTS	2-3 14-15	High Current Outputs for the Motor Coils. L1 and L2 are connected to one coil and L3 and L4 to the other coil.
$\overline{B}$/S	$\overline{BIAS}$/SET	6	This pins is typically 0.7 V below V_S. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CK	CLOCK	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if pin 6 is open.
$\overline{F}$/HS	$\overline{FULL}$/HALF STEP	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. (see figure 4 for sequence).
$\overline{CW}$/CCW	$\overline{CLOCKWISE}$ COUNTERCLOCKWISE	10	This input allows reversing the rotation of the rotation of the motor. (see figure 4 for sequence).
OIC	OUT IMPEDANCE CONTROL	8	This input is relevant only in the half step mode (pin 9 > 2 V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S. (see figure 4).
$\overline{Ph\ A}$	$\overline{PHASE\ A}$	11	This outputs indicate (when low) that the driver outputs are in the phase A condition (L1 = L3 = V_{OHD} ; L2 = L4 = V_{OLD}).

DC ELECTRICAL CHARACTERISTICS(Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT LOGIC LEVEL						
V_{TLH}	Threshold Voltage (low to high)				2	V
V_{THL}	Threshold Voltage (high to low)		0.8			V
V_{HYS}	Hysteresis		0.4			V
I_{IL} I_{IH1} I_{IH2}	Current	V_I = 0.4 V V_I = 5.5 V V_I = 2.7 V	– 100		 100 20	µA
DRIVER OUTPUT LEVELS						
V_{OHD}	Output High Voltage	I_{OD} = – 350 mA I_{OD} = – 0.1 mA I_{BS} = – 300 µA	V_S – 2.0 V_S – 1.2			V V
V_{OLD}	Output Low Voltage	I_{BS} = – 300 µA I_{OD} = – 350 mA			0.8	V
D_{VOD}	Difference Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = 350 mA			0.15	V
C_{VOD}	Common Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = – 0.1 mA			0.15	V
I_{OZ1}	Out Leakage-HiZ State	0 < V_D < V_M, I_{BS} = 5 µA	– 100		+ 100	µA
I_{OZ2}	Out Leakage-HiZ state	0 < V_{OD} < V_M, I_{BS} = – 300 µA Pin 9 = 2 V Pin 8 = 0.8 V	– 100		+ 100	µA
CLAMP DIODES						
V_{DF}	Forward Voltage	I_D = 350 mA		2.5	3	V
I_{DR}	Leakage Current	V_R = 21 V			100	µA
PHASE A OUTPUT						
V_{OLA}	Out Low Voltage	I_{OA} = 8 mA			0.4	V
	Off State Leakage Current	V_{OA} = 16.5 V			100	µA
POWER SUPPLY						
I_{SSB}	Power Supply Current in Stand by State	V_{BS} = V_S			12	mA
I_S	Power Supply Current (I_{OD} = 0) ; I_{BS} = – 300 µA)	L1 = V_{OHD} L2 = V_{OLD} L3 = V_{OHD} L4 = V_{OHD}			75	mA

BIAS SET CURRENT

I_{BS}	Bias Set Current	to set $\overline{\text{PHASE A}}$	– 5			µA

Notes : 3. DVOD = | VOD1.2 - VOD3.4 |
VOD1.2 = (VOHD1 - VOHD2) or (VOHD2 - VOLD1) AND VOD3.4 = (VOHD3 - VOHD4) OR (VOHD4 - VOHD3)
4. CVOD = | VOHD1 - VOHD2 or VOHD3 - VOHD4 |

AC SWITCHING CHARACTERISTICS (T_{amb} = 25 °C ; V_M = 12 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CK}	Clock Frequency		0		30	KHz
PWCKH	Clock Pulse Width	HIGH	10			µs
PWCKL	Clock Pulse Width	LOW	20			µs
t_{SU}	Set-up Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		5			µs
t_{HO}	Hold Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		10			µs
t_{PCD}	Propagation Delay CLK-to Driver Out			8		µs
t_{PBSD}	Propagation Delay $\overline{\text{Bias}}$/Set to Driver Output			1		µs
t_{PHLA}	Propagation Delay CLK-to Phase A LOW			12		µs
t_{PLHA}	Propagation Delay CLK-to Phase A HIGH			5		µs

Figure 1: AC Test Circuit.

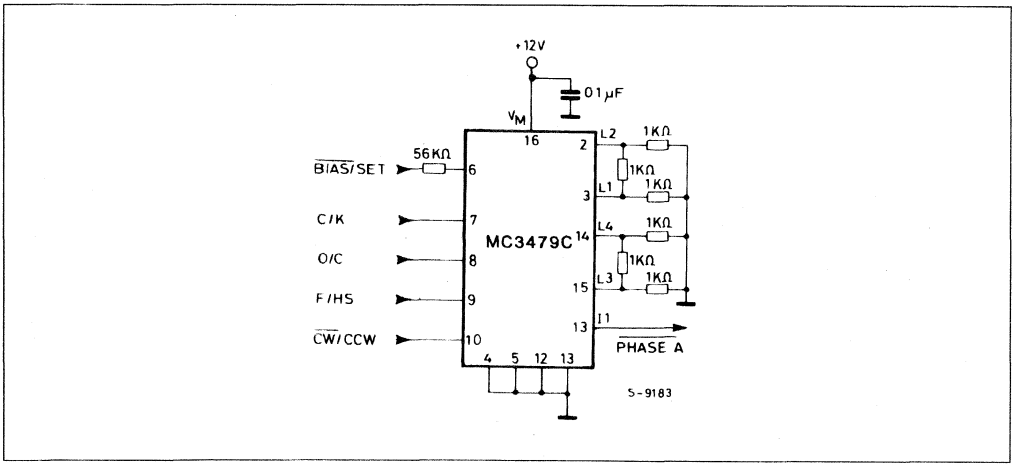


Figure 2 : Typical Application Circuit.

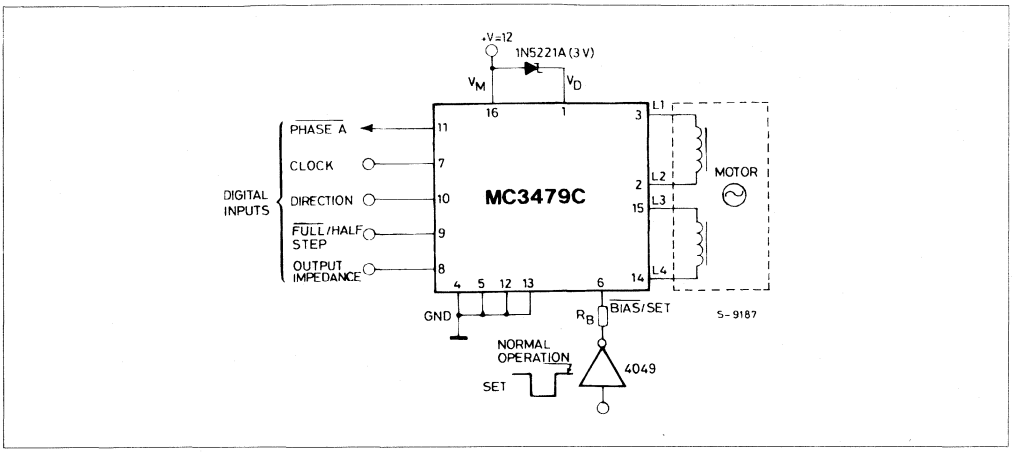


Figure 3 : Bias/Set Timing (refer to fig.1).

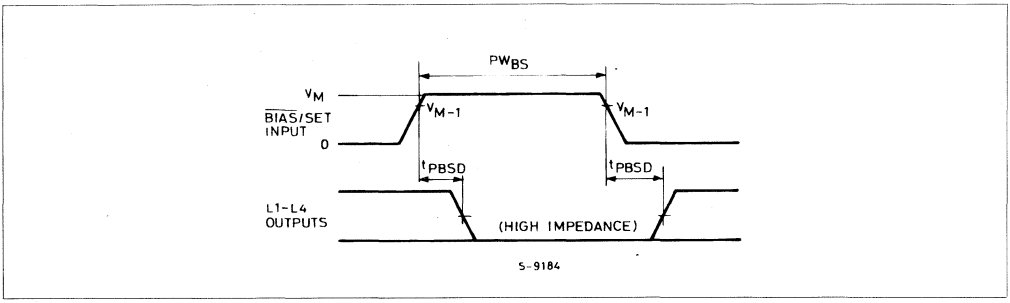


Figure 4 : Clock Timing (refer to fig.1).

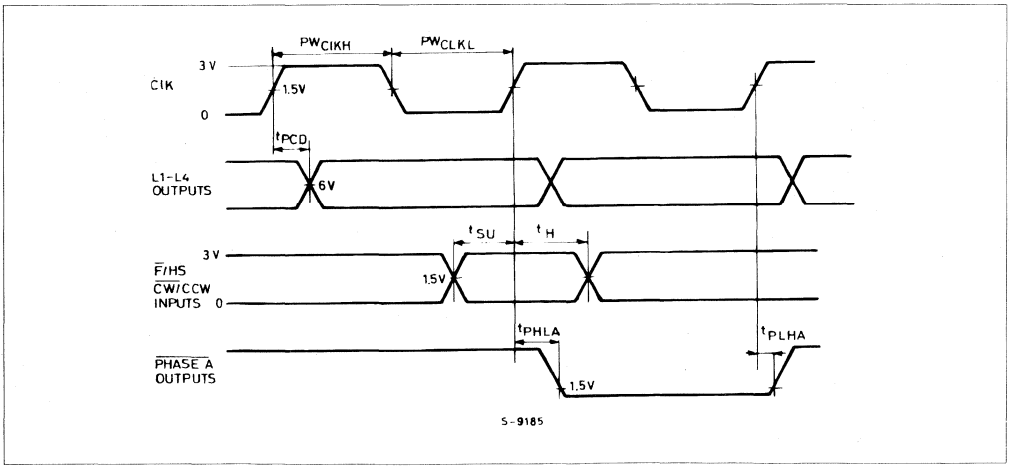
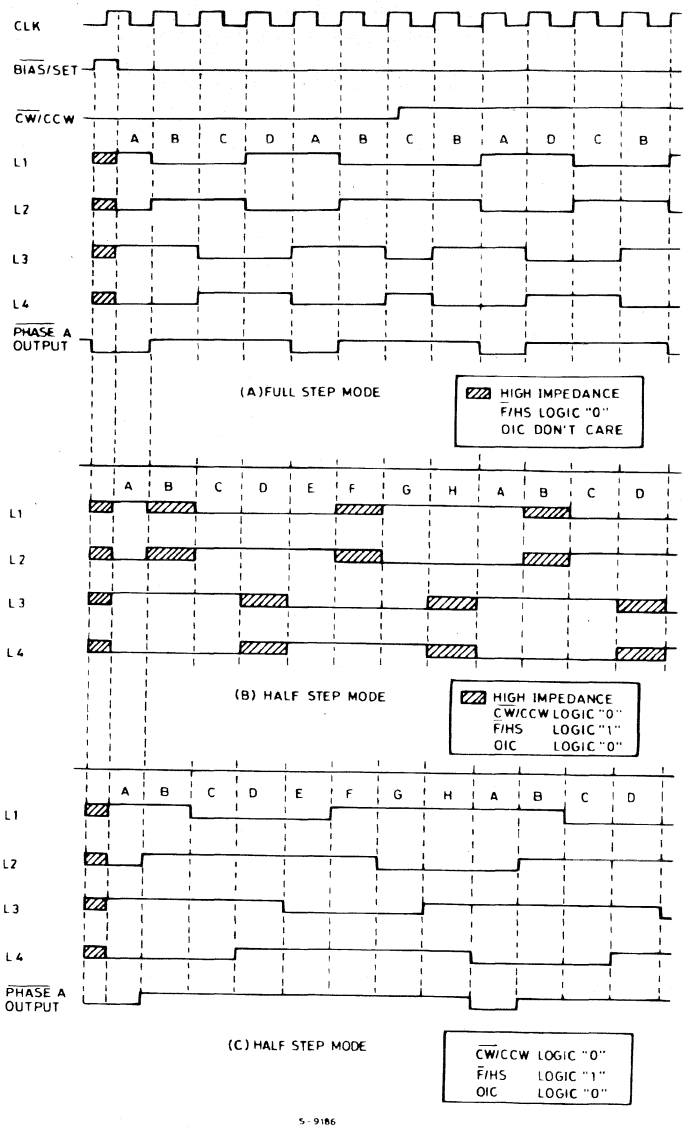


Figure 5 : Output Sequence.



SGS-THOMSON MICROELECTRONICS

PBL3717A

STEPPER MOTOR DRIVER

- FULL STEP - HALF STEP - QUARTER STEP OPERATING MODE
- BIPOLAR OUTPUT CURRENT UP TO 1 A
- FROM 10 V UP TO 46 V MOTOR SUPPLY VOLTAGE
- LOW SATURATION VOLTAGE WITH INTEGRATED BOOTSTRAP
- BUILT IN FAST PROTECTION DIODES
- EXTERNALLY SELECTABLE CURRENT LEVEL
- OUTPUT CURRENT LEVEL DIGITALLY OR ANALOGUE CONTROLLED
- THERMAL PROTECTION WITH SOFT INTERVENTION

DESCRIPTION

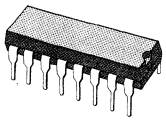
The PBL3717A is a monolithic IC which controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow.

A monostable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two PBL3717As and few external components form a complete stepper motor drive subsystem.

The raccomended operating ambient temperature ranges is from 0 to 70 °C.

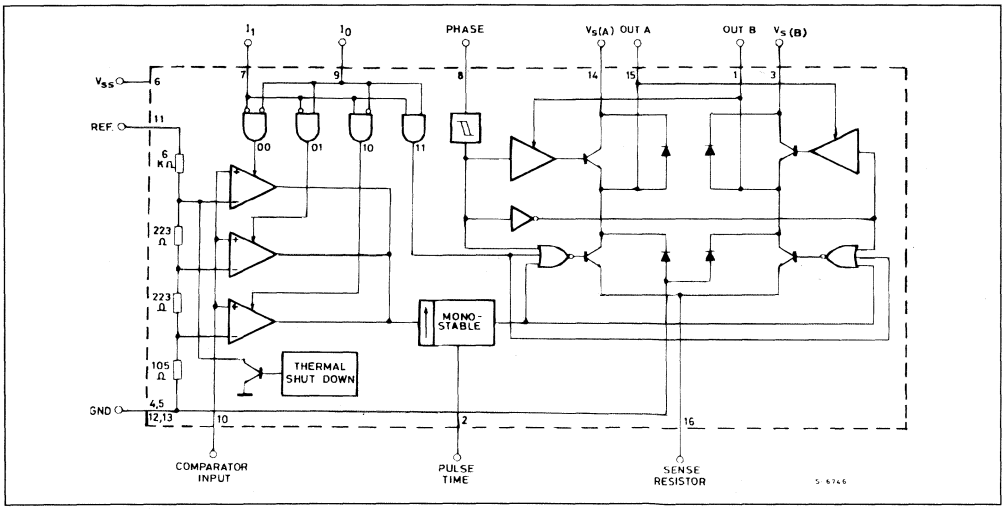
The PBL3717A is supplied in a 12 + 2 + 2 lead Powerdip package.



Powerdip 12 + 2 + 2

ORDER CODE : PBL3717A

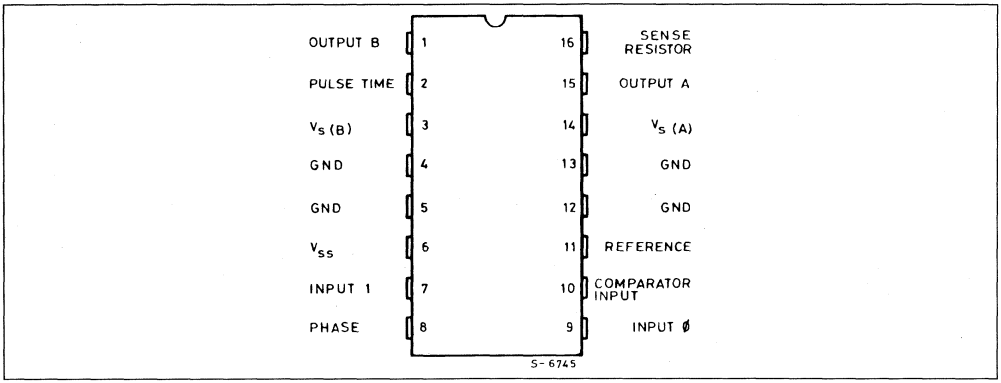
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage (pins 14, 3)	50	V
V_{ss}	Logic Supply Voltage (pin 6)	7	V
V_i	Logic Input Voltage (pins 7, 8, 9)	6	V
V_c	Comparator Input (pin 10)	V_{ss}	
V_r	Reference Input Voltage (pin 11)	15	V
I_o	Output Current (DC operation)	1.2	A
T_{stg}	Storage Temperature	– 55 to + 150	°C
T_j	Operating Junction Temperature	150	°C

CONNECTION DIAGRAM (top view)



TRUTH TABLE

Input 0 (pin 9)	Input 1 (pin 7)	
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	High Current

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	11	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient*	40	°C/W

* Soldered on a 35µ thick 20 cm^2 P.C. board copper area.

PIN FUNCTIONS

N°	Name	Function
1	OUTPUT B	Output Connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69\ R_T\ C_T$).
3	SUPPLY VOLTAGE B	Supply Voltage Input for Half Output Stage. See also pin 14.
4	GROUND	Ground Connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7) .
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter $R_C\ C_C$. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T\ C_T$, $t_{off} = 0.69\ R_T\ C_T$.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_S and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE A	Supply Voltage Input for Half Output Stage. See also pin 13.
15	OUTPUT A	See pin 1.
16	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor.

Figure 1 : Test and Application Circuit.

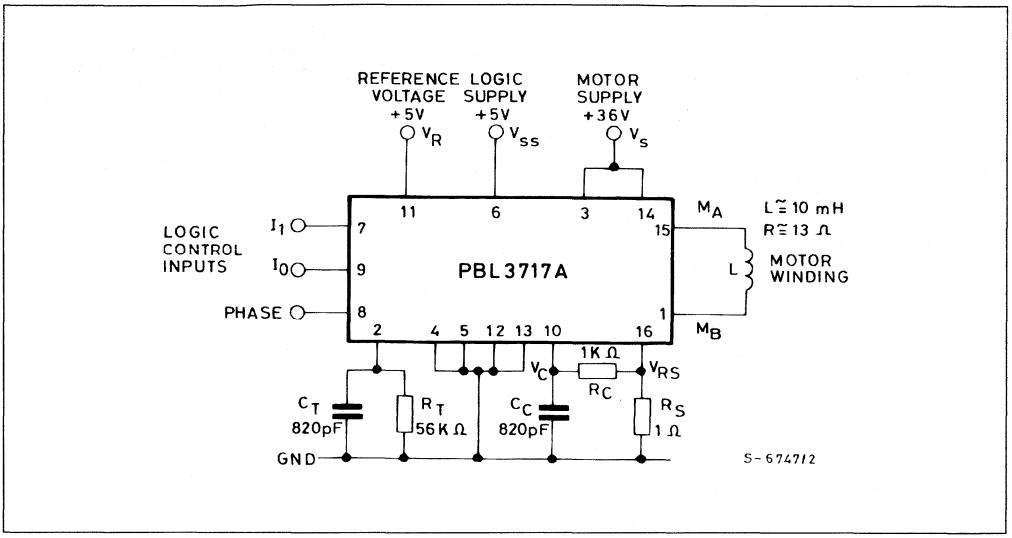
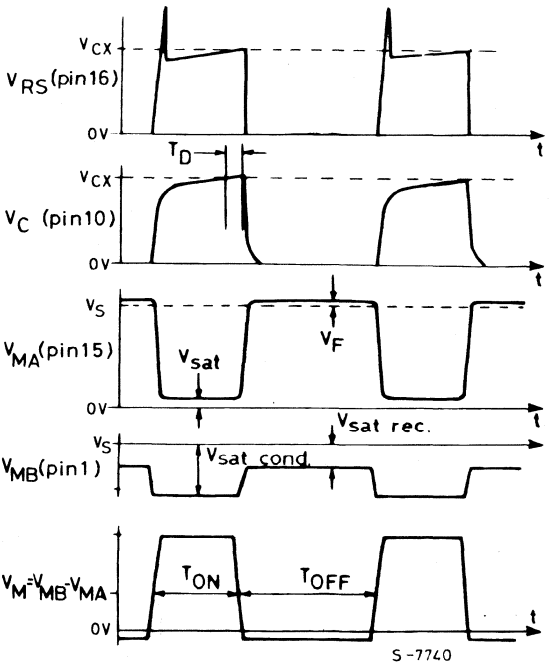


Figure 2 : Waveforms with MA Regulating (phase = 0).



ELECTRICAL CHARACTERISTICS (refer to the test circuit V_s = 36 V, V_{ss} = 5 V, Tamb = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_s	Supply Voltage (pin 3, 14)			10		46	V
V_{ss}	Logic Supply Voltage (pin 6)			4.75		5.25	V
I_{ss}	Logic Supply Current (pin 6)				7	15	mA
I_R	Reference Input Current (pin 11)	V_R = 5 V			0.75	1	mA
LOGIC INPUTS							
V_{iL}	Input Low Voltage (pins 7, 8, 9)					0.8	V
V_{iH}	Input High Voltage (pin 7, 8, 9)			2		V_{ss}	V
I_{iL}	Low Voltage Input Current (pins 7, 8, 9)	V_i = 0.4 V	pin 8			− 100	µA
			pins 7, 9			− 400	µA
I_{iH}	High Voltage Input Current (pins 7, 8, 9)	V_i = 2.4 V				10	µA
COMPARATORS							
V_{CL}	Comparator Low Threshold Voltage (pin 10)	V_R = 5 V	I_o = L, I_1 = H	66	78	90	mV
V_{CM}	Comparator Medium Threshold Voltage (pin 10)	V_R = 5 V	I_o = H, I_1 = L	236	251	266	mV
V_{CH}	Comparator High Threshold Voltage (pin 10)	V_R = 5 V	I_o = L, I_1 = L	396	416	436	mV
I_C	Comparator Input Current (pin 10)					± 20	µA
t_{off}	Cutoff Time	R_T = 56 KΩ	C_T = 820 pF	25		35	µs
t_d	Turn Off Delay	(see fig. 2)				2	µs
I_{off}	Output Leakage Current (pins 1, 15)	I_o = H	I_1 = H			100	µA
SOURCE DIODE-TRANSISTOR PAIR							
V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 0.5 A (see fig. 2)	Conduction Period		1.7	2.1	V
			Recirculation Period		1.1	1.35	
V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 1 A (see fig. 2)	Conduction Period		2.1	2.8	V
			Recirculation Period		1.7	2.5	
I_{LK}	Leakage Current	V_s = 46 V				300	µA
V_F	Diode Forward Voltage	I_M = − 0.5 A			1	1.25	V
		I_M = − 1 A			1.3	1.7	
I_{SLK}	Substrate Leakage Current when Clamped	I_M = − 0.5 A				2	mA
		I_M = − 1A				5	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

SINK DIODE-TRANSISTOR PAIR

V_{sat}	Saturation Voltage (pins 1, 15)	I_M = 0.5 A		1.1	1.35	V
		I_M = 1 A		1.6	2.3	V
I_{LK}	Leakage Current	V_S = 46 V			300	µA
V_F	Diode Forward Voltage	I_M = 0.5 A		1.1	1.5	V
		I_M = 1 A		1.4	2	

APPLICATION CIRCUIT

Figure 3 : Two Phase Bipolar Stepper Motor Driver.

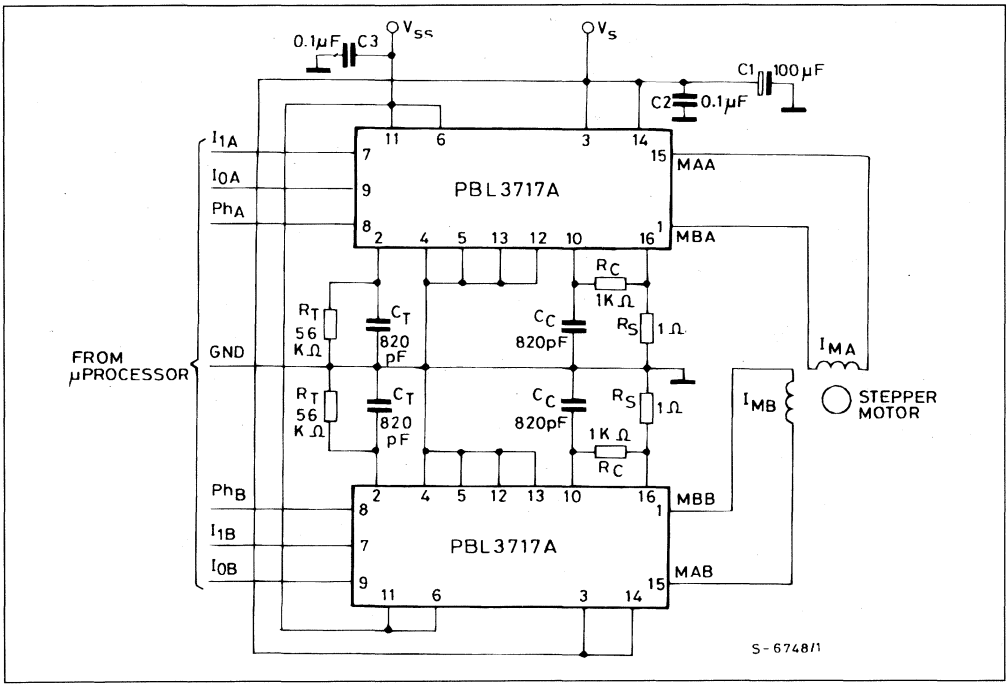


Figure 4 : P.C. Board and Component Layout of the Circuit of fig. 3 (1 : 1 scale).

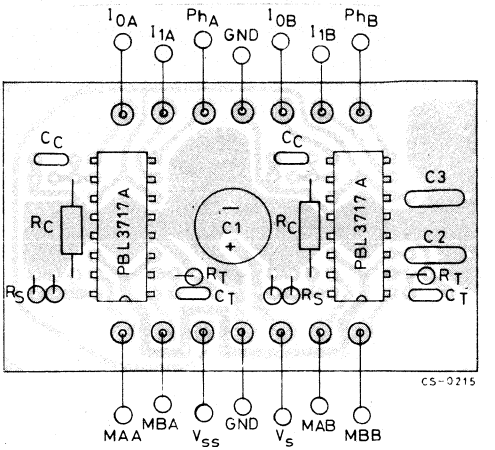
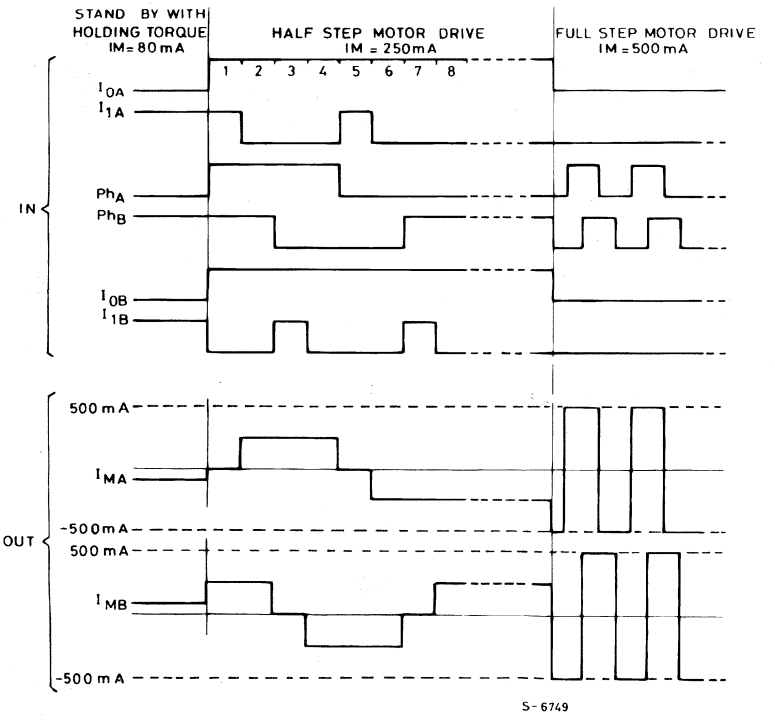


Figure 5 : Input and Output Sequences for Half Step and Full Step Operation.



APPLICATION INFORMATIONS

Fig. 3 shows a typical application in which two PBL3717A control a two phase bipolar stepper motor.

PROGRAMMING

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B ; a low level from output B to output A.

It is recommended that unused inputs are tied to pin 6 (V_{ss}) or pin 4 (GND) as appropriate to avoid noise problem.

The current levels can be varied continuously by changing the ref. voltage on pin 11.

CONTROL OF THE MOTOR

The stepper motor can rotate in either directions according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

FULL STEP OPERATION

Both the windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$.

I_0 and I_1 remain fixed at whatever torque value is required.

Calling A the condition with winding A energized in one direction and $\overline{A}$ in the other direction, the sequence for full step rotation is :

$$AB \rightarrow \overline{A}B \rightarrow \overline{AB} \rightarrow A\overline{B} \text{ etc.}$$

For the rotation in the other direction the sequence must be reserved.

In the full step operation the torque is constant each step.

HALF STEP OPERATION

Power is applied alternately to one winding then both according to the sequence :

$AB \rightarrow B \rightarrow \overline{A}B \rightarrow \overline{A} \rightarrow \overline{AB} \rightarrow \overline{B} \rightarrow A\overline{B} \rightarrow A$ etc.

Like full step this can be done at any current level ; the torque is not constant but it is lower when only one winding is energized.

A coil is turned off by setting I_0 and I_1 both high.

QUARTER STEP OPERATION

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.

The extra quarter steps are added to the half steps sequence by putting one coil on half current according to the sequence.

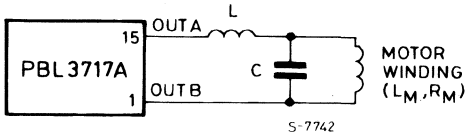
$$AB \rightarrow \frac{A}{2} B \rightarrow B \rightarrow \frac{\overline{A}}{2} B \rightarrow \overline{A}B \rightarrow \overline{A}\,\frac{B}{2} \rightarrow \overline{A} \text{ etc.}$$

MOTOR SELECTION

As the PBL3717A provides constant current drive, with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor over heat.

L -C FILTER

To reduce EMI and chopping losses in the motor a low pass L -C filter can be inserted across the outputs of the PBL3717A as shown on the following picture.



$$L \cong \frac{1}{10} LM \qquad C \cong \frac{4 \cdot 10^{-10}}{L}$$

Figure 6 : Source sat. Voltage vs. Output Current (recirc. period).

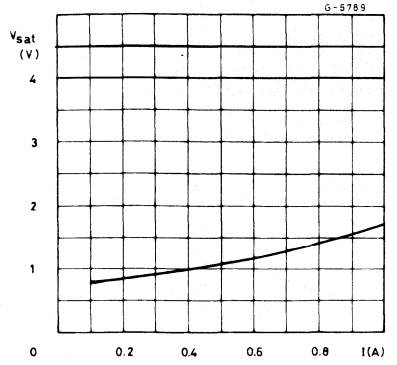


Figure 7 : Source sat. Voltage vs. Output Current (conduction period).

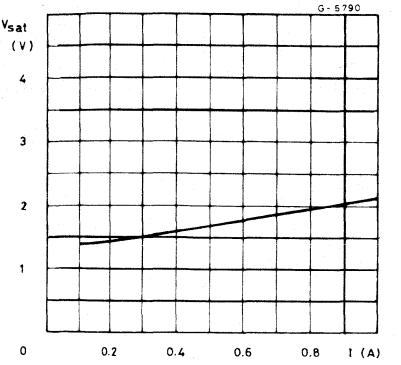


Figure 8 : Sink sat. Voltage vs. Output Current.

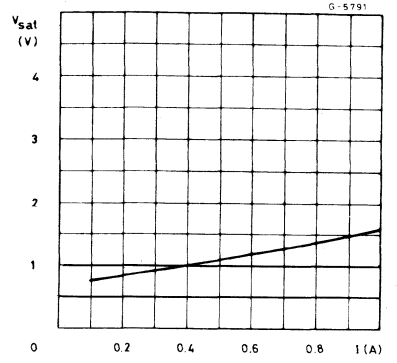
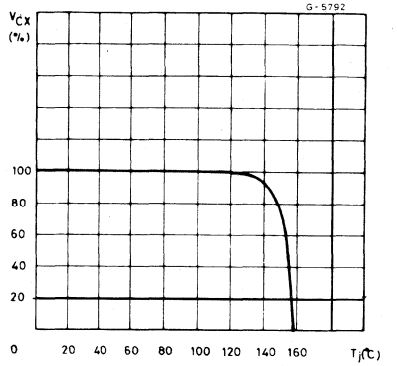


Figure 9 : Comparator threshold vs. Junction Temperature.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the PBL 3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 11 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thichkness of 35μ (see fig. 10).

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 10 : Example of P.C. Board Copper Area Which is Used as Heatsink.

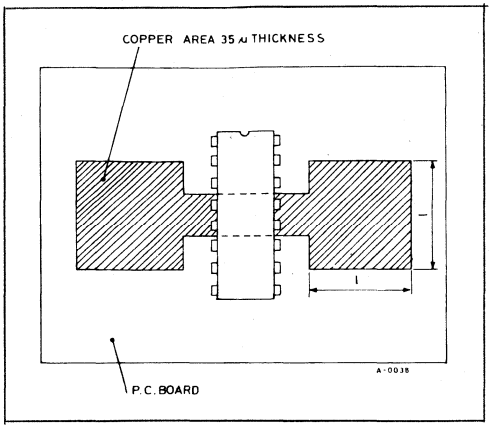
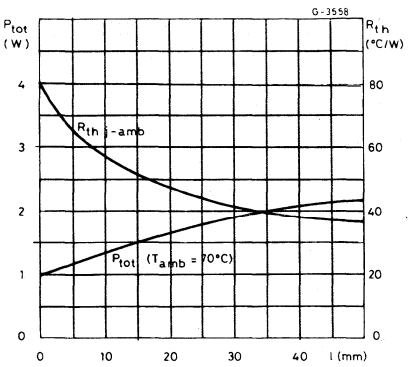


Figure 11 : Max. Dissipable Power and Junction to Ambient Thermal Resistance vs. size "α".

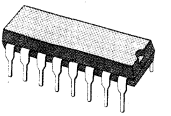


REGULATING PULSE WIDTH MODULATORS

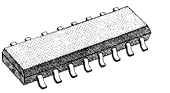
- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT .. 8 mA TYPICAL
- OPERATION UP TO 300 KHz
- 1 % MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

DESCRIPTION

The SG1524 , SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



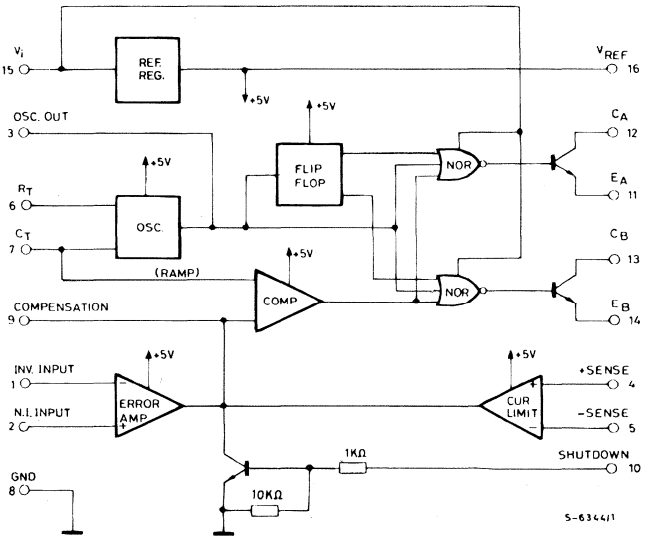
DIP-16
(Plastic –0.25– and Ceramic)



SO16 J

ORDER CODES : SG1524J – SG2524J – SG3524J (Ceramic)
SG2524N – SG3524N (Plastic)
SG2524P – SG3524P (SO–16J)

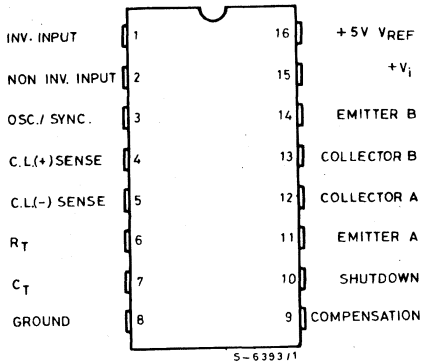
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Supply Voltage	40	V
I_C	Collector Ouptut Current	100	mA
I_R	Reference Output Current	50	mA
I_T	Current Through C_T Terminal	– 5	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	1000	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature Range **SG1524** **SG2524** **SG3524**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

CONNECTION DIAGRAMS



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO16J
$R_{th\ j\text{-}amb}$	Themal Resistance Junction-ambient	Max	80 °C/W	150 °C/W	–
$R_{th\ j\text{-}aluminia}$	Themal Resistance Junction-aluminia	Max	–	–	50 °C/W

* Thermal resistance junction–alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

ELECTRICAL CHARACTERISTICS (unless otherwise stated , these specifications apply for T_j = – 55 °C to+ 125 °C for the SG1524, – 25 °C to + 85 °C for the SG2524, and 0 °C to + 70 °C for the SG3524, V_N = 20 V, and f = 20 KHz).

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40 V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
	Ripple Rejection	f = 120 Hz, T_j = 25 °C		66			66		dB
	Short Circuit Current Limit	V_{REF} = 0, T_j = 25 °C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 125 °C, t = 1000 Hrs		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001 µF, R_T = 2 kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40 V, T_j = 25 °C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25 °C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01 µF, T_j = 25 °C		0.5			0..5		µs
ERROR AMPLIFIER SECTION									
V_{OS}	Input Offset Voltage	V_{CM} = 2.5 V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2.5 V		2	10		2	10	µA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25 °C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25 °C		70			70		dB
B	Small Signal Bandwidth	A_v = 0 dB, T_j = 25 °C		3			3		MHz
V_O	Output Voltage	T_j = 25 °C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2 V With Error Amplifier Set for Max. Out, Tj = 25 °C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		− 1		+ 1	− 1		+ 1	
OUTPUT SECTION (each output)									
	Collector-emitter Volt.		40			40			V
	Collector Leackage Cur.	V_{CE} = 40 V		0.1	50		0.1	50	µA
	Saturation Voltage	I_c = 50 mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20 V	17	18		17	18		V
t_r	Rise Time	R_c = 2 KΩ, T_j = 25 °C		0.2			0.2		µs
t_f	Fall Time	R_c = 2 KΩ, T_j = 25 °C		0.1			0.1		µs
I_q*	Total Standby Curr.	V_{IN} = 40 V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Figure 1 : Open-loop Voltage Amplification of Error Amplifier vs. Frequency.

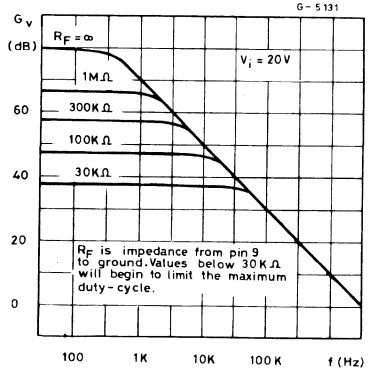


Figure 2 : Oscillator Frequency vs. Timing Components.

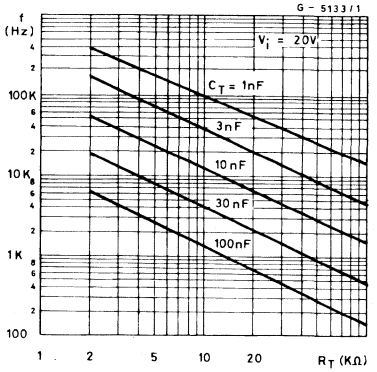


Figure 3 : Output Dead Time vs. Timing Capacitance Value.

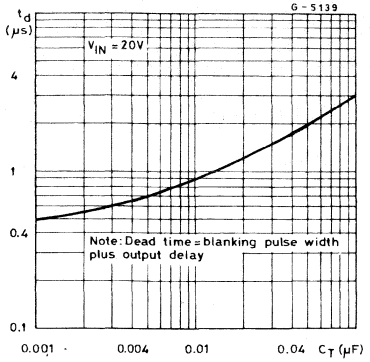


Figure 4 : Output Saturation Voltage vs. Load Current .

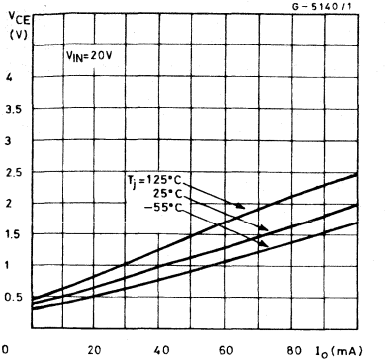
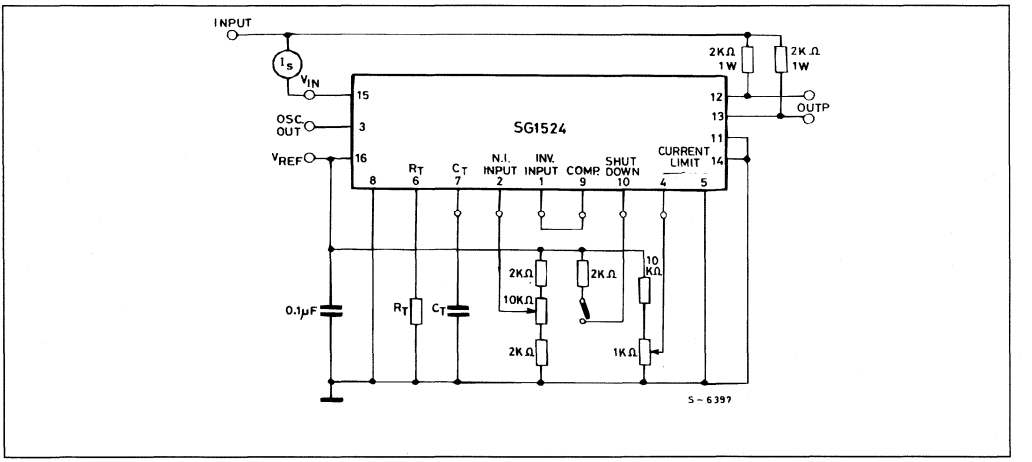


Figure 5 : Open Loop Test Circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T. This results in a linear voltage ramp at CT, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5 V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generale a feedback signal to error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both output are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs

may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	- 0.03 to - 2	mA
Timing Resistor, R_T	1.8 to 100	KΩ
Timing Capacitor, C_T	0.001 to 0.1	µF

TYPICAL APPLICATIONS DATA

OSCILLATOR

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula :

$$f \approx \frac{1.18}{R_T C_T}$$

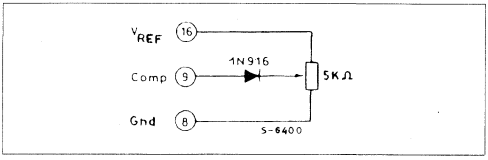
where R_T is in KΩ
C_T is in µF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1 µF. Pratical values of R_T fall between 1.8 and 100 KΩ. This results in a frequency range typically from 120 Hz to 500 KHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below :

Figure 6.



SYNCHRONOUS OPERATION

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator ouptut terminal. The impedance to ground at this point is approximately 2 KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Figure 7: Flyback Converter Circuit.

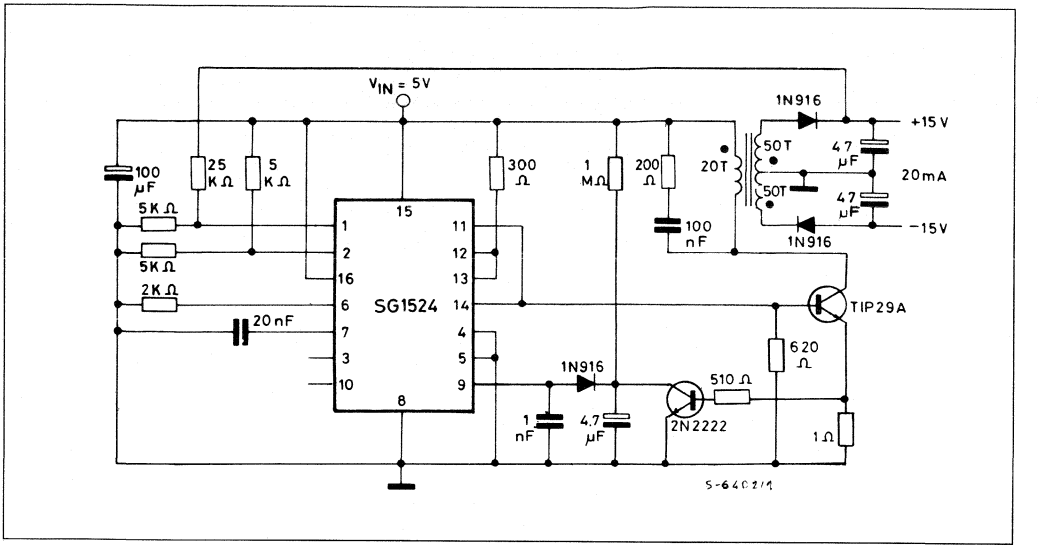
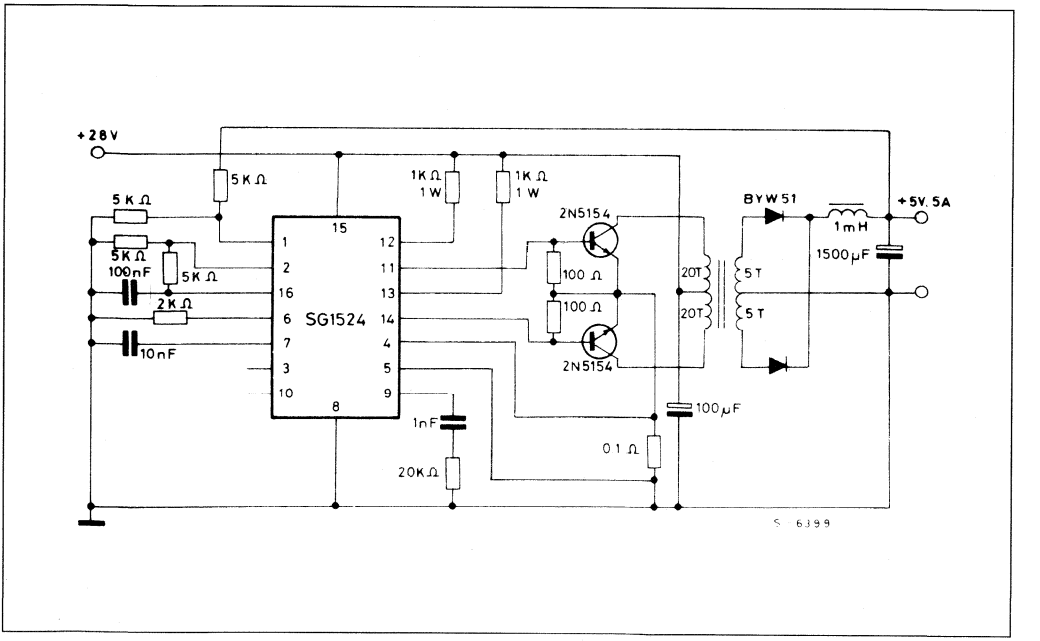


Figure 8: PUSH-PULL transformer-coupled circuit.



SGS-THOMSON MICROELECTRONICS

SG1525A/27A
SG2525A-3525A/27A

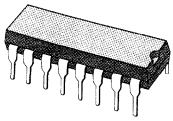
REGULATING PULSE WIDTH MODULATORS

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

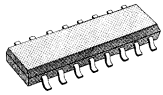
DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

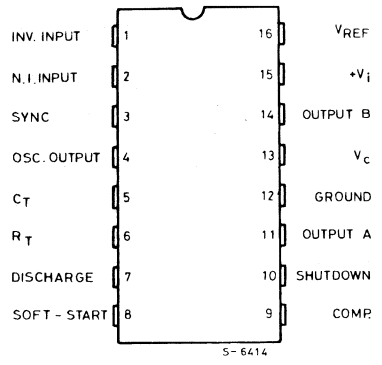
DIP-16
(Plastic -0.25 and Ceramic)



SO16J



CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	Plastic DIP	Ceramic DIP	SO16J
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_I	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **SG1525A/27A** **SG2525A/27A** **SG3525A/27A**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

THERMAL DATA (DIP-16)

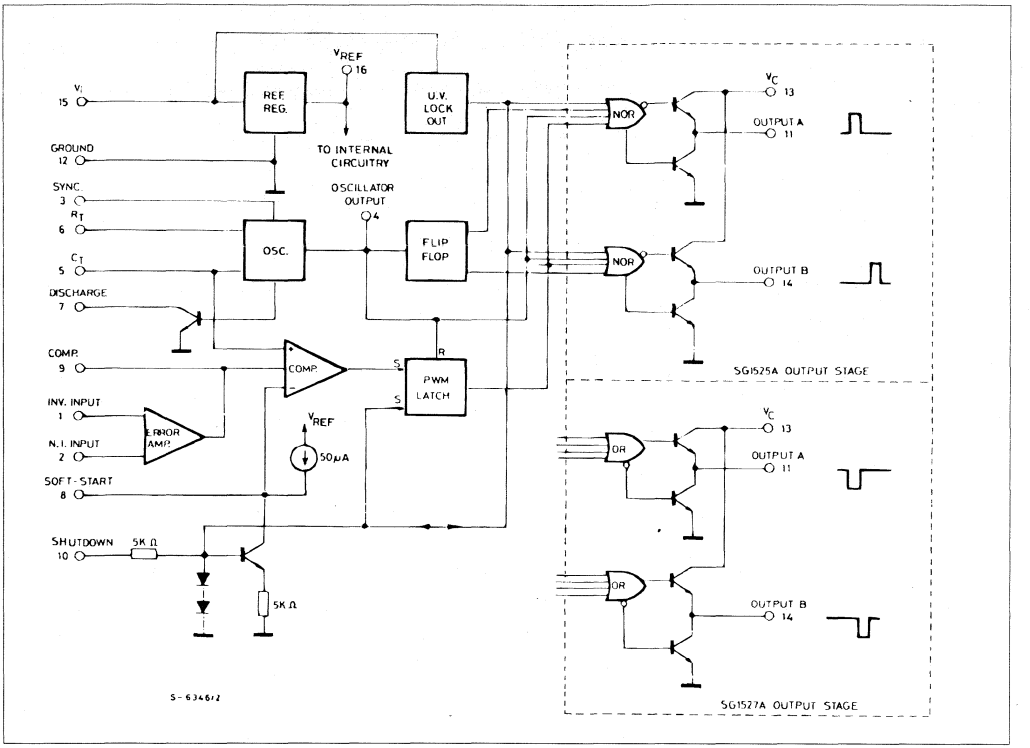
			Ceramic	Plastic
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	–	50 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150 °C/W	80 °C/W

THERMAL DATA (SO16J)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 × 20 mm ; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V_i = 20 V, and over operating temperature, unless otherwise specified)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_j = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_j = 25 °C		40	200		40	200	µVrms
ΔV_{REF}*	Long Term Stability	T_j = 125 °C, 1000 hrs		20	50		20	50	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OSCILLATOR SECTION**									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	%
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 µF			120			120	Hz
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			KHz
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock Amplitude		3	3.5		3	3.5		V
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	µs
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	mV
I_b	Input Bias Current			1	10		1	10	µA
I_{os}	Input Offset Current				1			1	µA
	DC Open Loop Gain	$R_L \geq$ 10 MΩ	60	75		60	75		dB
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		MHz
*, z	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		ms
	Output Low Level			0.2	0.5		0.2	0.5	V
	Output High Level		3.8	5.6		3.8	5.6		V
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		dB
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		dB
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	%
	Maximum Duty-cycle		45	49		45	49		%
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	V
*	Input Bias Current			0.05	1		0.05	1	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SHUTDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_j = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_j = 25 °C		0.2	0.5		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
I_C	Collector Leakage	V_C = 35 V			200			200	µA
t_r*	Rise Time	C_L = 1 nF, T_j = 25 °C		100	600		100	600	ns
t_f*	Fall Time	C_L = 1 nF, T_j = 25 °C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_S	Supply Current	V_i = 35 V		14	20		14	20	mA

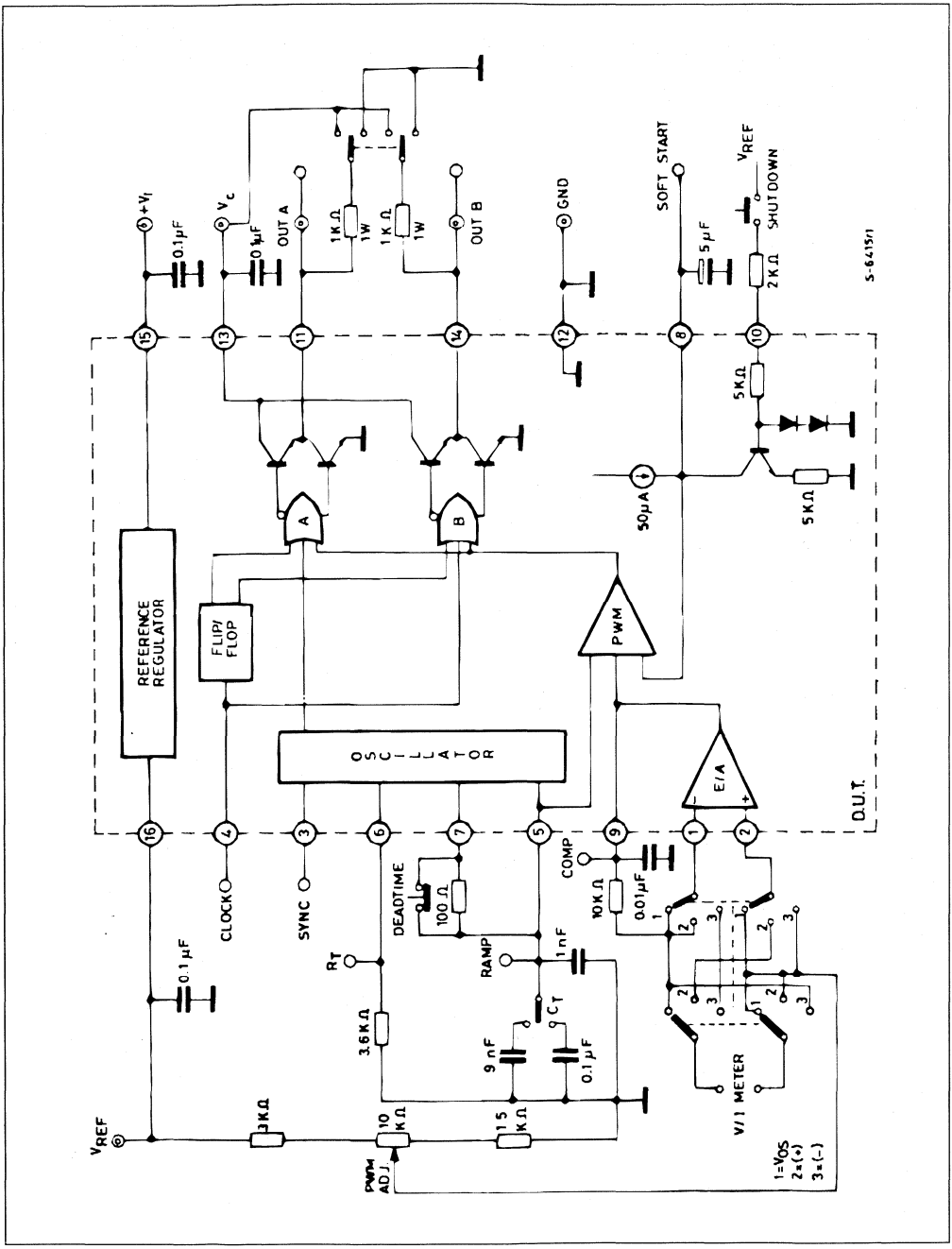
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

• Tested at f_{osc} = 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 µF, R_D = 0 Ω). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T (0.7\, R_T + 3\, R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_v) according to the following equation : $G_v = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.

TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS (•)

Parameter	Value
Input Voltage (V_i)	8 to 35 V
Collector Supply Voltage (V_C)	4.5 to 35 V
Sink/Source Load Current (steady state)	0 to 100 mA
Sink/Source Load Current (peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 KHz
Oscillator Timing Resistor	2 KΩ to 150 KΩ
Oscillator Timing Capacitor	0.001 µF to 0.1 µF
Dead Time Resistor Range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

Figure 1 : Oscillator Charge Time vs. R_T and C_T.

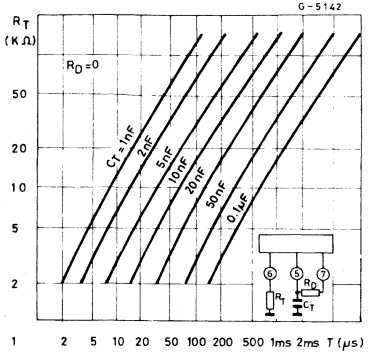


Figure 2 : Oscillator Discharge Time vs. R_D and C_T.

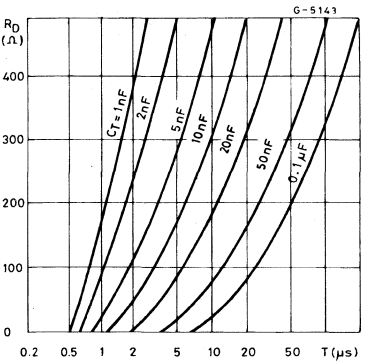


Figure 3 : SG1525A Output Saturation Characteristics.

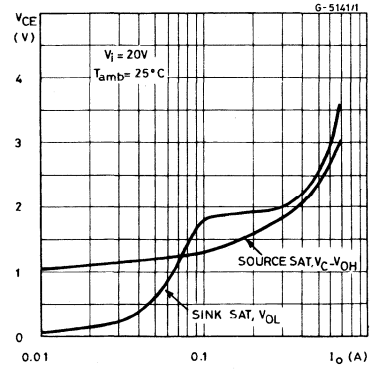


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

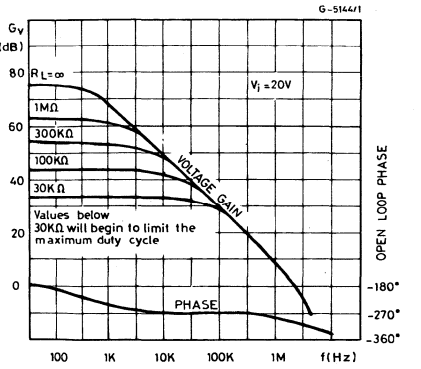
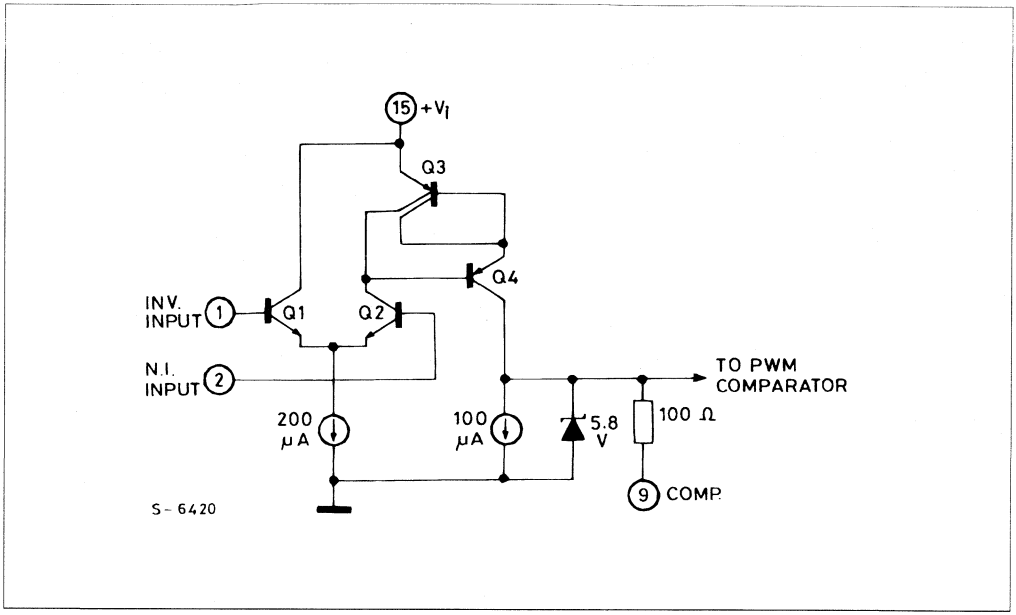


Figure 5 : SG1525A Error Amplifier.



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to the outputs ; and a 150 µA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Figure 6 : SG1525A Oscillator Schematic.

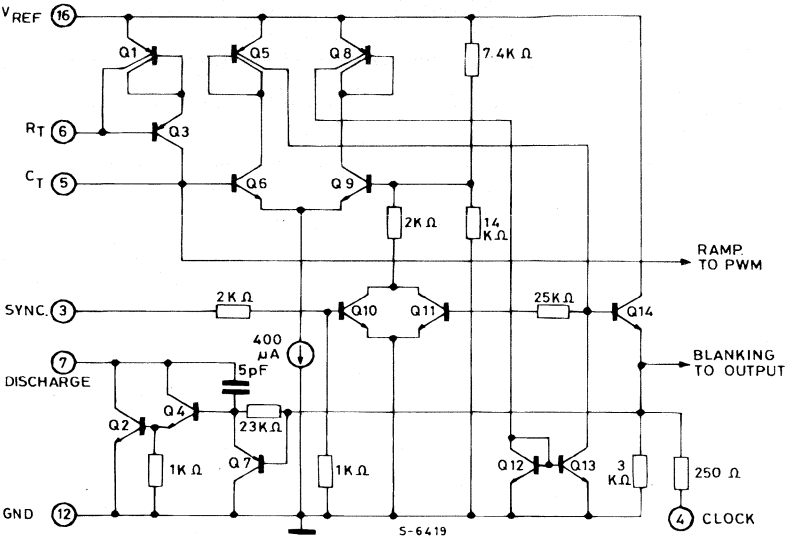


Figure 7 : SG1525A Output Circuit (1/2 circuit shown).

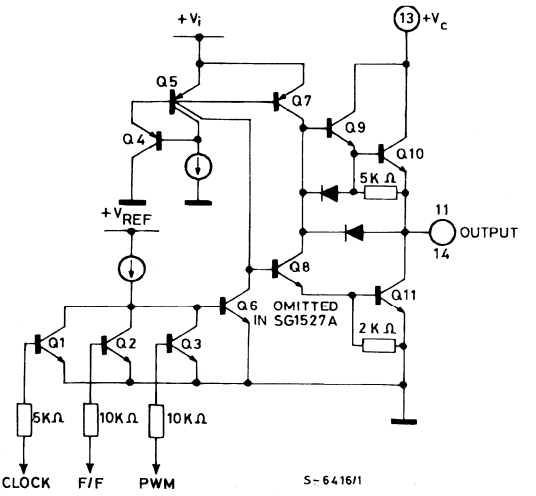
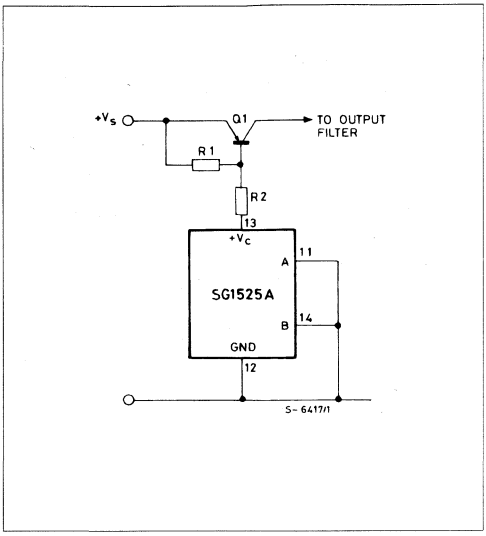
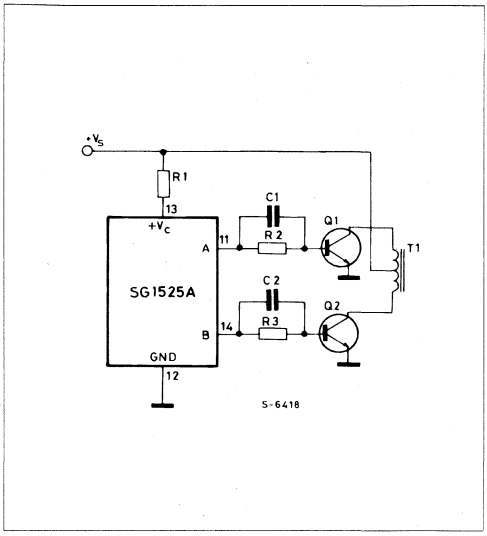


Figure 8.



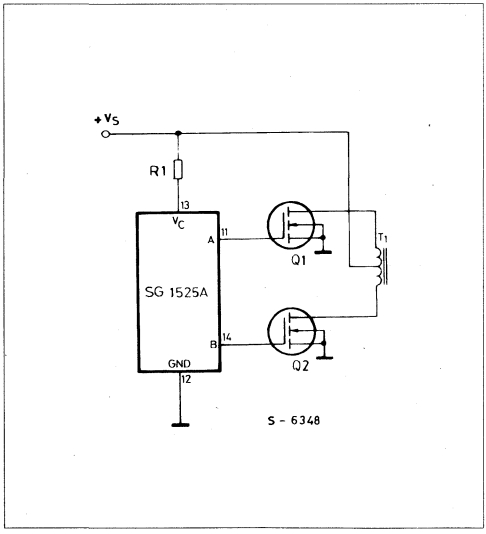
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9.



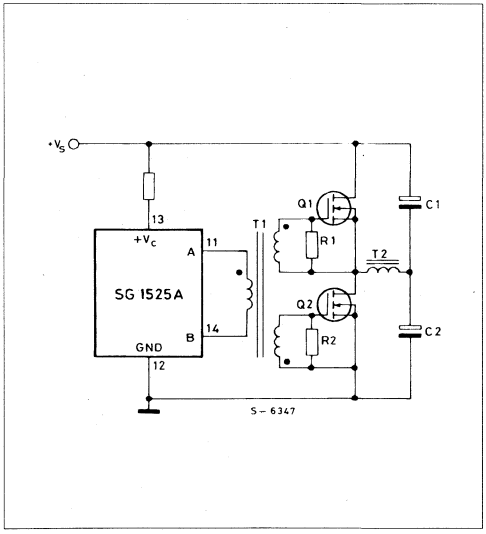
In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Figure 10.



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 11.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

SGS-THOMSON MICROELECTRONICS

TDA0161

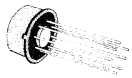
PROXIMITY DETECTORS

- OUTPUT CURRENT : 10 mA
- OSCILLATOR FREQUENCY : 10 MHz
- SUPPLY VOLTAGE : + 4 TO + 35 V

MINIDIP/2

SO-8J

TO-99



ORDER CODES : TDA0161DP (Minidip)
TDA0161FP (SO-8J)
TDA0161CM (TO-99)

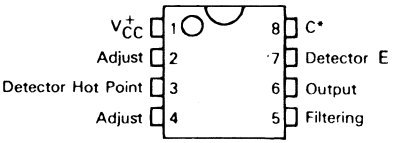
DESCRIPTION

These monolithic integrated circuits are designed for metallic body detection by detecting the variations in high frequency Eddy current losses. With an external tuned circuit they act as oscillators. Output signal level is altered by an approaching metallic object.

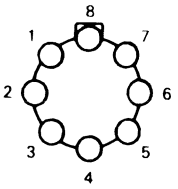
Output signal is determined by supply current changes. Independent of supply voltage, this current is high or low according to the presence or the absence of a close metallic object.

PIN CONNECTIONS (top views)

MINIDIP/SO-8



TO-99



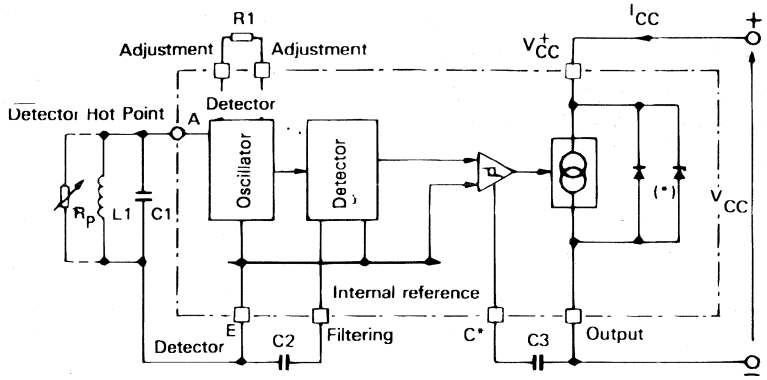
1 - Detector Hot Point
2 - Adjust
3 - Filtering
4 - Output
5 - Detector E
6 - C
7 - V_{CC}^{+}
8 - Adjust

Pin 4 connected to case

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		35	V
T_j	Junction Temperature	DP, FP Suffix CM Suffix	+ 150 + 175	°C
T_{stg}	Storage Temperature Range		– 55 to + 150	°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

TDA0161DP : - 40 °C < T_{amb} < + 100 °C
TDA0161FP : - 40 °C < T_{amb} < + 100 °C
TDA0161CM : - 40 °C < T_{amb} < + 140 °C
P_{tot} < 150 mW
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	TDA0161	4	–	35	V
–	Reverse Voltage Limitation (I_{CC} = - 100 mA)		–	– 1	–	V
I_{CC}	Supply Current, Close Target (T_{amb} = + 25 °C) + 4 V < V_{CC} < + 35 V	TDA 0161	8	10	12	mA
I_{CC}	Supply Current, Remote Target + 4 V < V_{CC} < + 35 V	TDA 0161	–	–	1	mA
–	Supply Current Transition Time C3 = 0 C3 ≠ 0		 – –	 1 [100 x C3(nF)]	 –	µs
f_{osc}	Oscillator Tuning Frequency		–	–	10	MHz
f_O	Output Frequency (C3 = 0)		0	–	10	kHz
ΔI_{CC}	Output Current Ripple - C3 = 0, C2 (pF) > 150/f_{osc} (MHz)		–	–	20	µA
R_n	Negative Resistance on Terminals A and E (4 kΩ < R1 < 50kΩ, f_{osc}< 3 MHz)		0.9 R1	R1	1.1 R1	–
H_{yst}	Hysteresis at Detection Point C2 (Pf) > 150/f_{osc} (MHz)		0.5	–	5	%

* If the circuit is used at a frequency higher than 3 MHz, it is recommended to connect a capacitor of 100 pF between terminals E and D.

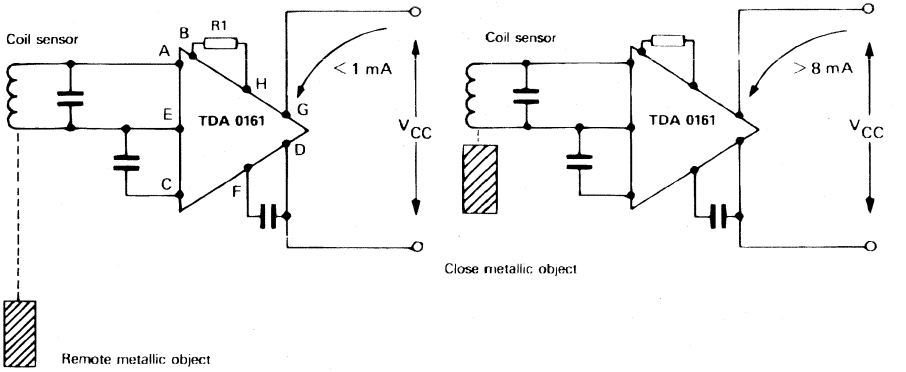
OPERATING MODE

Between terminals A and E, the integrated circuit acts like a negative resistance equal to the external resistor R1 connected between terminals B and H.

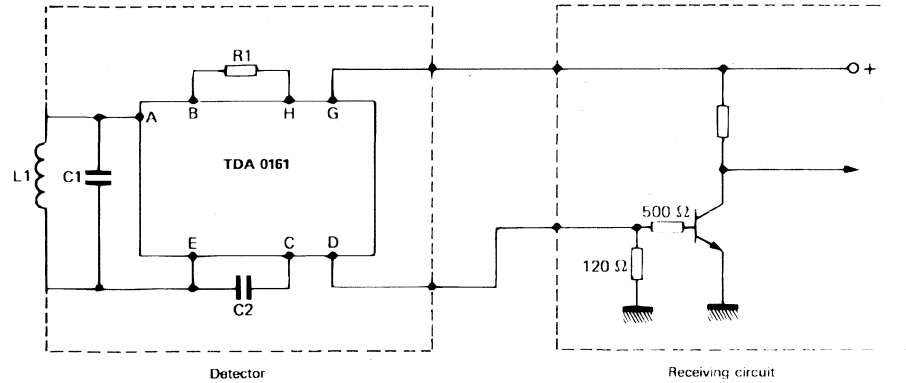
The oscillation stops when loss resistance Rp of tuned circuit becomes smaller than R1. Then, the supply current will be I_{CC} = 10 mA (pins G and D).

The oscillation sustains when loss resistance Rp of tuned circuit becomes higher than R1. Then, the supply current will be I_{CC} 1 mA (pins G and D).

Eddy currents induced by coil L1 in a metallic body, determine loss resistance Rp.



TYPICAL APPLICATIONS



Detection Range (*)	L1 (μH)		C1 (pF)	f_{osc} (kHz)	R1 (kΩ)	C2 pF
2 mm	30	(1)	120	2650	6.8	47
5 mm	300	(2)	470	425	27	470
10 mm	2160	(3)	4700	50	27	3300

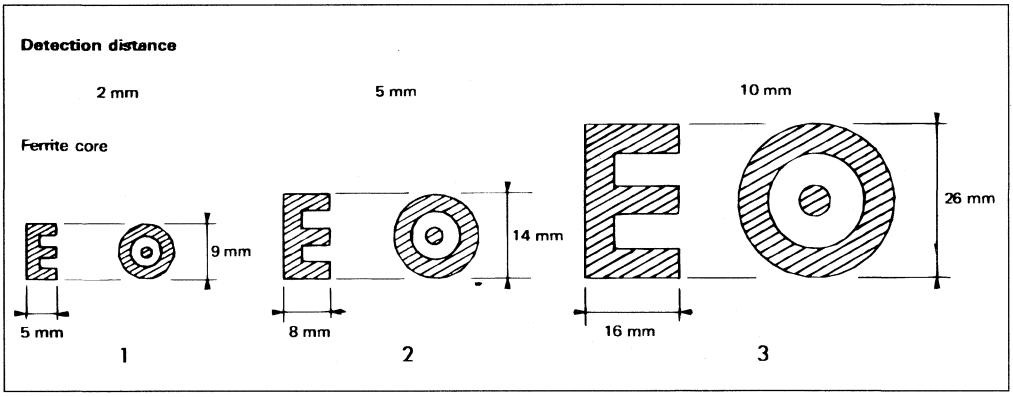
(*) Ingot steel target.

COIL CHARACTERISTICS

	Core	Coil Former	Wire**	Number of Turns
1	Cofelec 432 FP 9 x 5 SE	1/2 CAR 091 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	40
2	Cofelec 432 FP 14 x 8 SE	1/2 CAR 142 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	100
3	Cofelec 432 FP 26 x 16 SE	1/2 CAR 262 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	200

** The above results are obtained with single wire coil. When using Litz wire instead of single wire, the parallel resistance of the coil becomes higher and the value of R1 may be increased, resulting in better sensitivity.

TYPICAL APPLICATION EXAMPLES



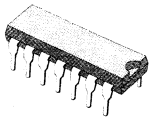
SGS-THOMSON MICROELECTRONICS

TDE0160

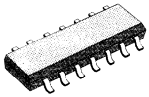
PROXIMITY DETECTOR

- SUPPLY VOLTAGE : + 4 TO + 36 V
- SUPPLY CURRENT : < 1.2 mA
- OUTPUT TRANSISTORS : I = 20 mA ; $V_{CE\ (sat)} \leq 1100$ mV
- OSCILLATOR FREQUENCY : < 1 MHz
- LOSS RESISTANCE : 5 TO 50 kΩ.

DIP-14/2
(Plastic)



SO-14J



ORDER CODES : TDE0160DP (DIP-14)
TDE 0160FP (SO-14J)

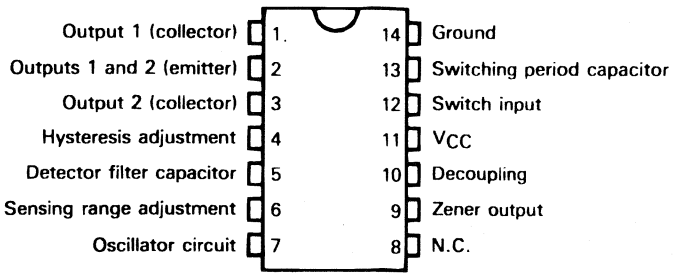
DESCRIPTION

The TDE0160 is designed to detect metal bodies by the effect of Eddy currents on the HF losses of a coil. It has two complementary open collector outputs with peak limiting. Hysteresis is adjustable, and an electronic switching circuit is incorporated for disabling both outputs.

An internal zener diode maintains the supply voltage to the circuit in "dipole" operation.

PIN CONNECTION

DIP-14 / SO-14J

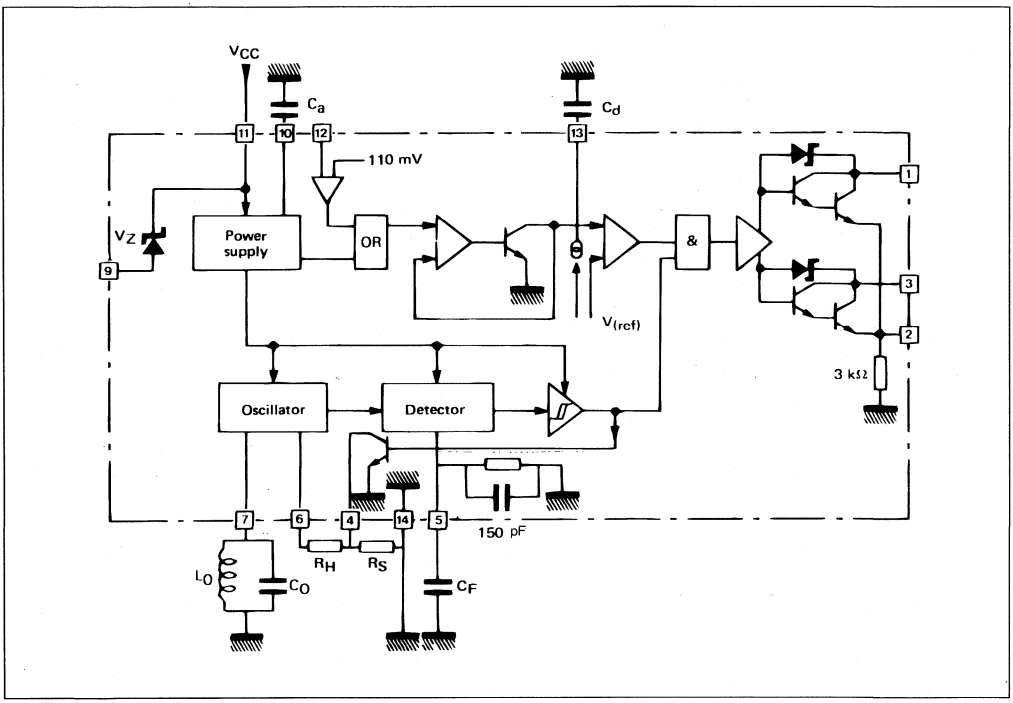


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_{O^*}	Output Voltage*	36	V
I_O (I_1-I_3)	Output Current (I_1-I_3)	40	mA
I_Z	Zener Current	40	mA
T_j	Junction Temperature	+ 150	°C
T_{oper}	Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Internal peak limiting to protect against transient voltage surges.

SCHEMATIC DIAGRAM

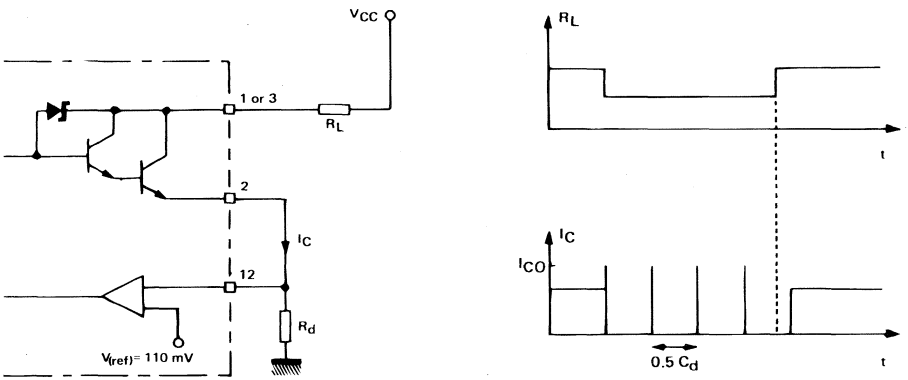


ELECTRICAL CHARACTERISTICS (T_{amb} = + 25 °C unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	Pin 11	4	–	36	V
V_Z	Zener Voltage (I_Z = 20 mA)	Pins 9–11	3	–	4	V
I_{CC}	Supply Current	Pin 11	–	–	1.2	mA
–	Limiting (I = 0.1 mA)	Pin 1 or 3	–	42	–	V
–	Output Transistor Saturation Voltage (I_1 or I_3 = + 20 mA)	Pin 1 or 3	–	0.9	1.1	V
–	Output Transistor Leakage Current (V = + 30 V)	Pin 1 or 3	–	–	2	µA
–	Switching Threshold	Pin 12	90	110	130	mV
R_n	Negative Resistance* (5 kΩ < R_H < 50 kΩ; f = 100 kHz ; R_S = 0)		–	$R_n = R_H$	–	–
–	Inherent Hysteresis (R_2 = 0)		–	1	2	%
–	Programmed Hysteresis (H < 15 %)		–	$\frac{R_S}{R_S + R_H}$	–	%
f_{osc}	Oscillation Frequency		–	–	1	MHz
–	Switching Frequency (with matched oscillator circuit)		–	750	–	Hz
–	Switching Time-delay		–	0.5 C_d (µF)	–	s
–	Switching Response Time (C_d = 10 nF ; V_{CC} = + 20 V)		–	10	–	µs

* See characteristic curves

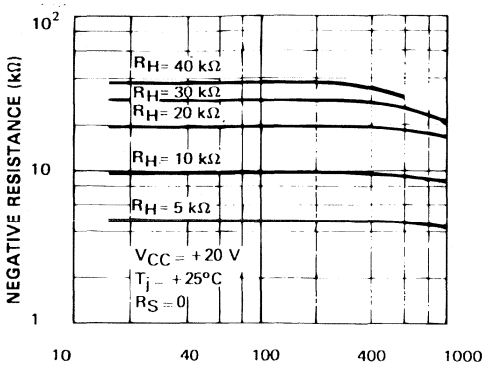
SWITCHING OPERATION



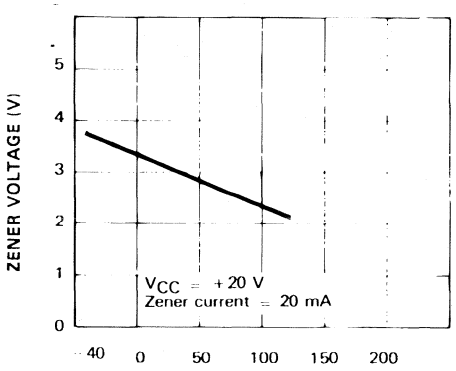
If I_C exceeds I_{CO}, where $I_{CO} = \frac{V_{(ref)}}{R_d}$, the switch cuts off the output transistors and tests the value of current I_C, with time constant 0.5 C_d.

On power up the internal start system cuts off the output transistors until V_{CC} reaches a value permitting normal operation of the circuit.

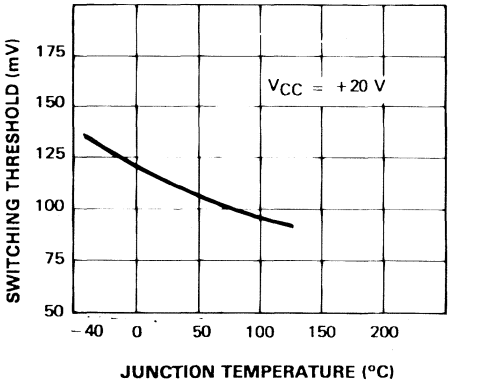
NEGATIVE RESISTANCE
vs
FREQUENCY



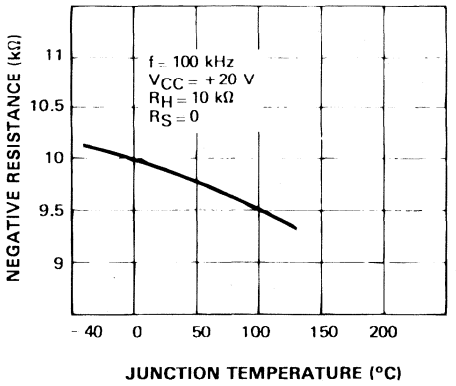
ZENER VOLTAGE
vs
JUNCTION TEMPERATURE



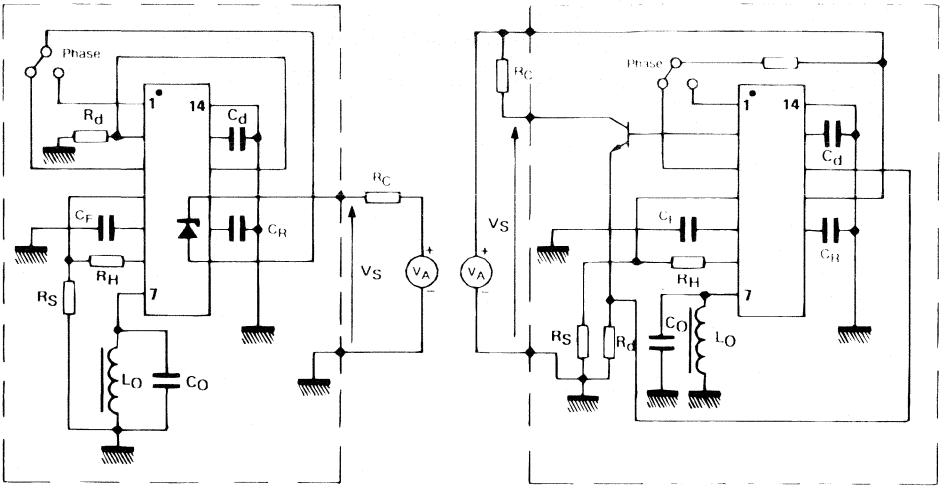
SWITCHING THRESHOLD
vs
JUNCTION TEMPERATURE

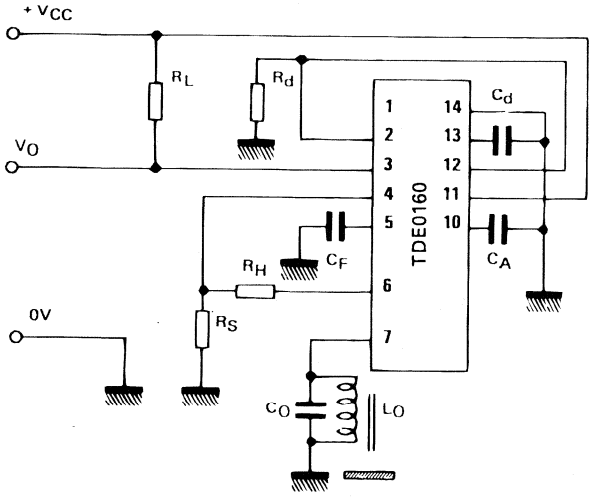


NEGATIVE RESISTANCE
vs
JUNCTION TEMPERATURE



TYPICAL APPLICATION DIAGRAMS





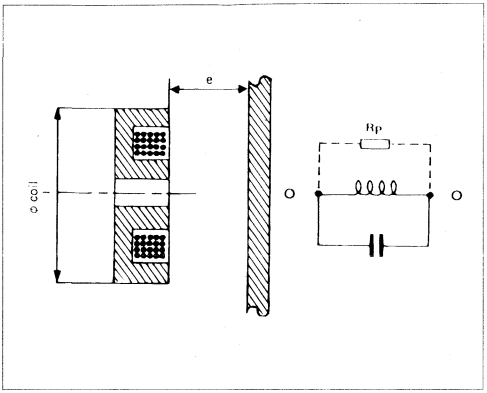
c)

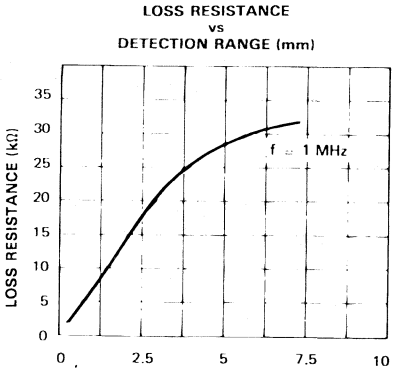
C_a : 10 nF
C_f : 1 nF
C_d : 10 nF
C_0 : 390 pF
L_0 : 65 µH to 1 MHz
R_d : 10 Ω
R_H : 15 kΩ
R_S : 3 kΩ
R_L : 2.2 kΩ

V_{CC} : 20 V
$f_0 \approx$ 1MHz
e_{mean} = 2.5mm

Φ coil :14 mm
Core COFELEC 432 FP
Turns : 47
Stranded wire : 15 x 5/100

MILD STEEL


e
ø coil
Rp


LOSS RESISTANCE
vs
DETECTION RANGE (mm)
LOSS RESISTANCE (kΩ)
35
30
25
20
15
10
5
0
0
2.5
5
7.5
10
f = 1 MHz

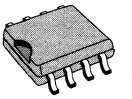
SGS-THOMSON MICROELECTRONICS

TDE1707

INTELLIGENT POWER SWITCH

ADVANCE DATA

- 0.5A OUTPUT CURRENT
- LOW SIDE OR HIGH SIDE SWITCH CONFIGURATION
- 6V TO 48V SUPPLY VOLTAGE RANGE
- OVERLOAD AND SHORT CIRCUIT PROTECTIONS
- INTERNAL VOLTAGE CLAMPING
- SUPPLY AND OUTPUT REVERSAL PROTECTION
- THERMAL SHUTDOWN
- GND AND V_S OPEN WIRE PROTECTION
- ADJUSTABLE DELAYED SWITCH ON
- INDICATOR STATUS LED DRIVER
- +5V REGULATED AUX. VOLTAGE



SO8

ORDERING NUMBER: TDE1707FP

Two output configurations are possible:

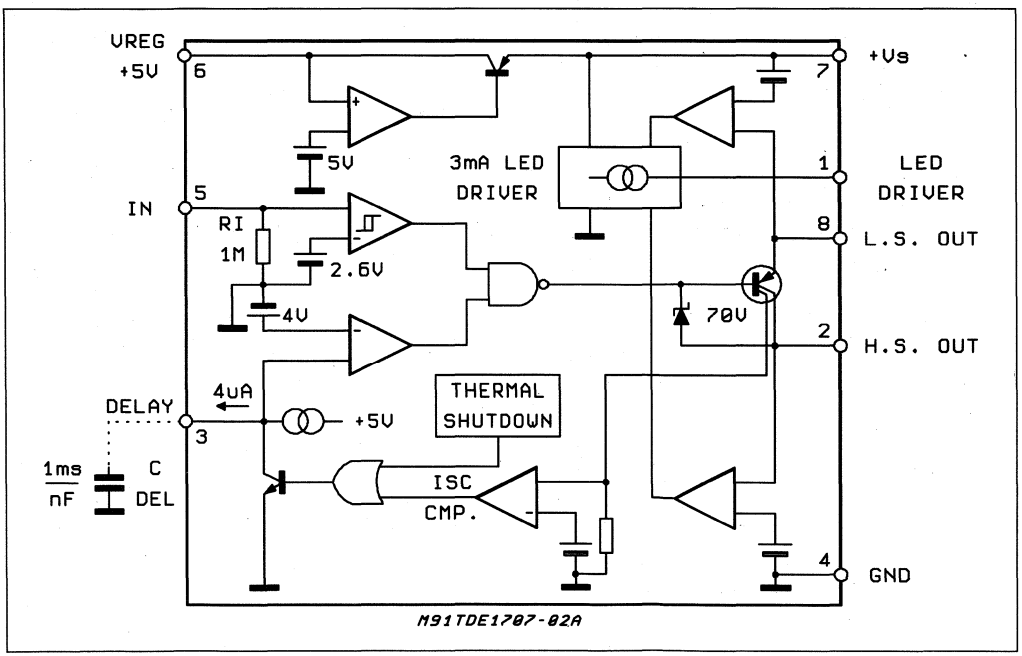
- Load to Gnd. (High Side Mode)
- Load to V_S (Low side Mode)

Especially dedicated to proxmity detectors, it can drive resistive or inductive loads.

DESCRIPTION

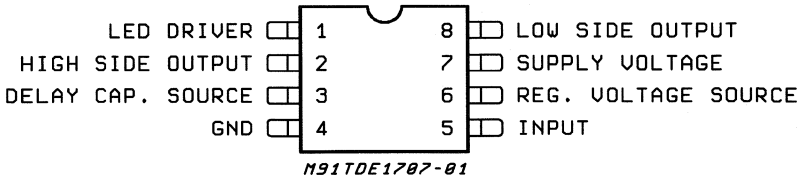
The TDE1707 is a 0.5A Integrated Power Switch with up to 48V Power supply capability.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
V_{Sr}	Supply Reverse Voltage	50	V
I_O	Output Current	internally limited	A
V_{reg}	Regulated Voltage Pin	0 to 7	V
V_{delay}	Delay Cap. Surce Pin	0 to 5	V
V_O	Output Diff. Voltage	55 (internally limited)	V
V_i	Input Voltage	-10 to 50	V
T_{op}	Operating Temperature Range	-25 to +85	°C
T_{stg}	Storage Temperature	-55 to 150	°C
P_{tot}	Power Dissipation	internally limited	W
E_I	Energy Induct. Load	150	mJ

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	150	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 24V; T_j = –25 to +85°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_s 7	Supply Voltage		6		48	V
I_{sr} 7	Supply Reverse Current	V_{SR} = –48V			1.5	mA
I_q 7	Quiescent Current	$I_{reg} = I_{led} = 0$; $V_i > 2V$; V_S = 6 to 48V			1.5	mA
I_o 8/2	Output Current	V_s = 6V to 32V			500	mA
I_o 8/2	Output Current	Vs = 32V to 48V			300	mA
V_{sat} 8/2	Output Voltage Drop V_{8-2}	I_o = 500mA		1.1	1.6	V
V_{sat} 8/2	Output Voltage Drop V8-2	Io = 300mA			1.5	V
I_{sc} 8/2	Short Circuit Current		0.5	0.8	2	A
V_{cl} 8/2	Internal Voltage Clamp	I_{CL} = 10mA	55	65		V
I_{olk} 8/2	Output Leakage	(Pin 2) $V_i < 2V$; V_o = 0 to V_s (Pin 8)		100	300 100	µA µA
V_{ith} 5	Input Voltage Threshold		2		3	V
V_{ihis} 5	Input Threshold Hysteresis			300		mV
I_{lk} 5	Input Current	V_i = 5V		2	5	µA
V_{reg} 6	Regulated Output Voltage	I_{reg} < 5mA	4.5	5	5.5	V
I_{scr} 6	Short Circuit Regulated		6	30	50	mA
I_{reg} 6	Ouput Regulator Current	V_s = 35V V_s = 48V			6 4	mA mA
I_{old} 1	Current Surce Sink Led Driver	Output ON (±)	2	3	4	mA
V_{old} 1	Voltage Drop Led Driver	I_{os} = 2mA (±)		1.2	1.6	V
Oldlk 1	Lead Driver (off) Leak.	$V_i < 2V$; $R_L < 1K\Omega$			10	µA
I_{dch} 4	Del. Cap. Charge Current	T_J = 25°C	2	4	6	µA
V_{dth} 4	Delay Voltage Trigger	T_J = 25°C		4		V

DYNAMIC CHARACTERISTICS (V_S = 24V; R_L = 48Ω; T_J = 25°C)

t_{on}	Propagation Turn on Time	V_i = 0 to 5V		15		µs
t_{off}	Propagation Turn off Time	V_i = 5 to 0V		15		µs
t_{don}	Delayed Turn on Time / nF Delay Capacitor		0.65	1	2	ms
$t_{d\ min}$	Minimum Delayed t_{on} Delay Capacitor = 0			25		µs

APPLICATION CIRCUIT

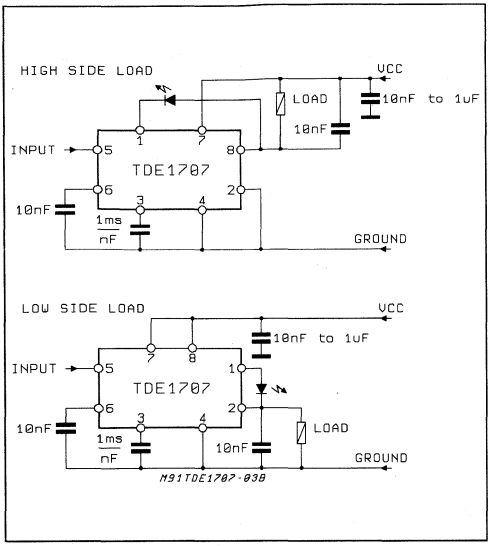


Figure 1: Input Thresholds Voltage vs. Temperature (V_S = 24V)

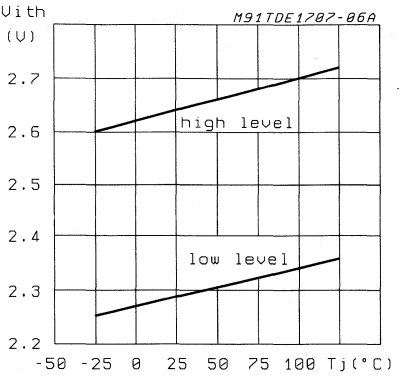


Figure 2: Saturation Voltage vs. Temperature (V_S = 24V; I_O = 500mA)

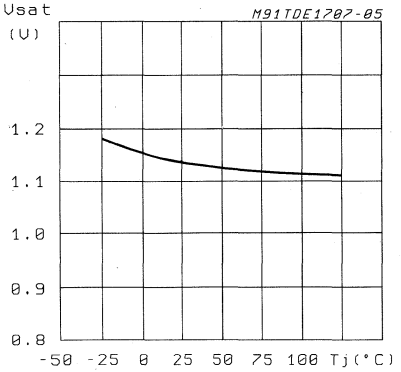
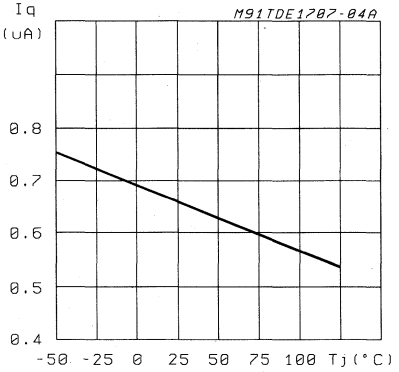


Figure 3: Quiescent Current) vs.Temperature (V_S = 24V)



INTERFACE CIRCUIT - RELAY AND LAMP-DRIVER

- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 8 V to + 45 V

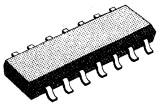
DESCRIPTION

The TDE1737-TDF1737 is a monolithic amplifier designed for high current and high voltage applications, specifically to drive lamps, relays and control of stepper motors.

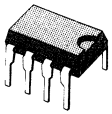
This device is essentially blow-out proof. Current limiting is available to limit the peak output current to a safe value, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from overheating. If internal dissipation becomes too great, the driver will shut down to prevent excessive heating.

The output is also protected against short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 used for industrial electronic systems.



SO-14 J
FP SUFFIX



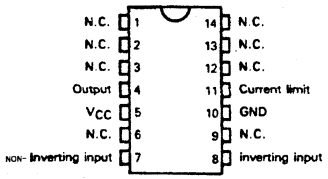
MINIDIP/2
DP SUFFIX

ORDER CODES

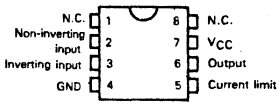
Part Number	Temperature Range	Package	
		DP	FP
TDE1737	– 25 °C to + 85 °C	•	•
TDF1737	– 40 °C to + 85 °C	•	•
Example : TDE1737DP			

PIN CONNECTION (top views)

SO-14



MINIDIP



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		50	V
V_I	Input Voltage		50	V
V_{ID}	Differential Input Voltage		50	V
I_O	Output Current		1000	mA
P_{tot}	Power Dissipation		Internally Limited	W
T_{oper}	Operating Free–air Temperature Range	TDE1737	– 25 to + 85	°C
T_{oper}	Operating Free–air Temperature Range	TDF1737	– 40 to + 85	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	MINIDIP	50	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	MINIDIP	120	°C/W
	Junction-ceramic Substrate (case glued to substrate)	SO14	90	°C/W
	Junction–ceramic Substrate (case glued to substrate, substrate temperature maintened constant)	SO14	65	°C/W

ELECTRICAL CHARACTERISTICS

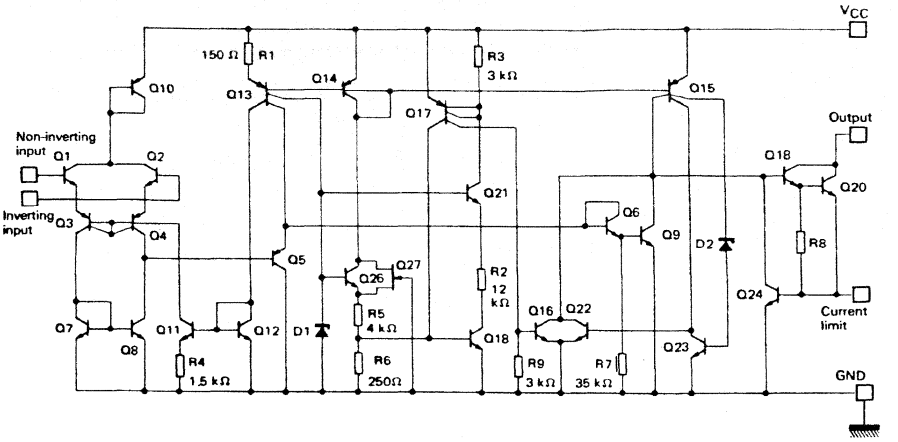
TDE1737 – 25 °C ≤ T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ + 150 °C
(unless otherwise specified)

TDF1737 – 40 °C ≤ T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ 150 °C

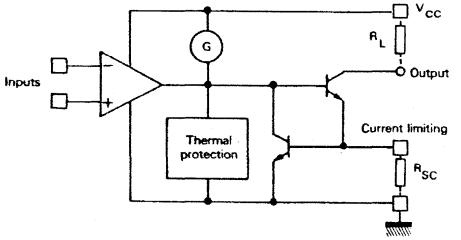
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage - (note 1)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	µA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0)	–	3	5	mA
V_{CM}	Common-mode Input Voltage Range	2	–	V_{CC}–2	V
I_{SC}	Short-circuit Current Limit (R_{SC} = 1.5 Ω, T_{case} = + 25 °C)	–	500	–	mA
V_{CC}–V_O	Output Saturation Voltage (output low) ($V_I^+ - V_I^- \geq 50$ mV I_O = 300 mA, R_{SC} = 0)	–	1	1.5	V
I_{OL}	Output Leakage Current (output high) ($V_O = V_{CC}$ = + 24 V, T_{amb} = + 25 °C)	–	–	10	µA

Notes : 1. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.
2. Devices bonded on a 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of cooper.

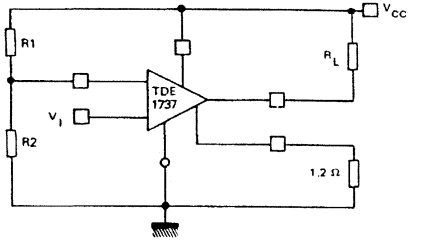
SCHEMATIC DIAGRAM



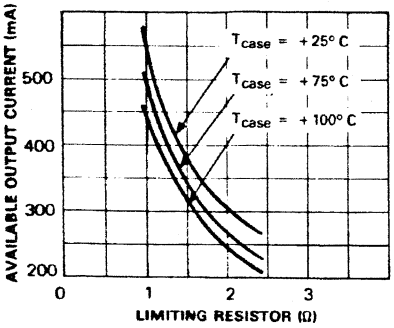
SIMPLIFIED SCHEMATIC



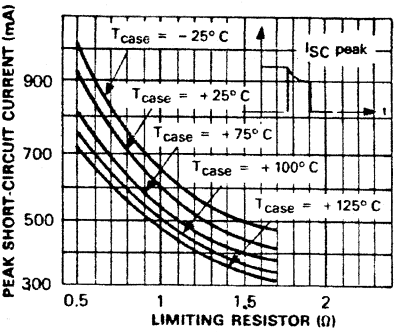
TYPICAL APPLICATION -



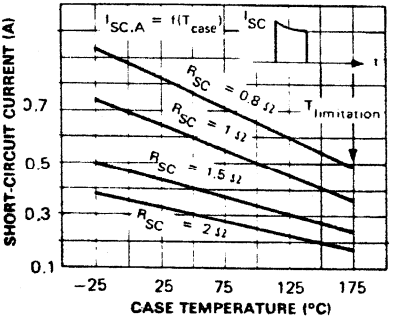
Available output current versus limiting resistors



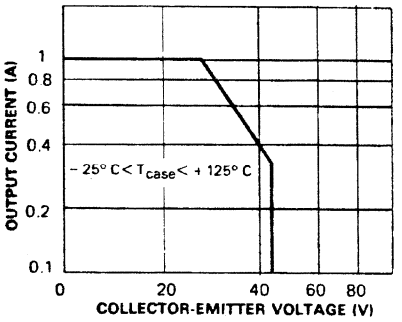
Peak short-circuit current versus limiting resistor



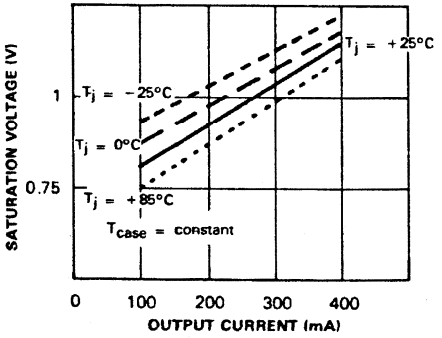
Short-circuit current versus case temperature



Safe operating area (non repetitive overload)

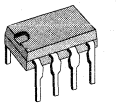


Saturation voltage versus output current

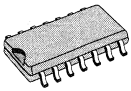


INTERFACE CIRCUIT – RELAY AND LAMP – DRIVER

- OPEN GROUND PROTECTION
- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION TO GROUND
- THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 45 V
- SHORT-CIRCUIT PROTECTION TO V_{CC}



Minidip (DP)



SO14 (FP)

ORDERING NUMBERS:
TDE1747DP
TDE1747FP
TDF1747DP

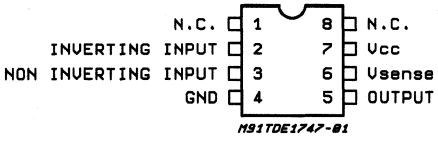
DESCRIPTION

The TDE/TDF1747 is a monolithic comparator designed for high current and high voltage applications, specifically to drive lamps, relays, stepping motors.

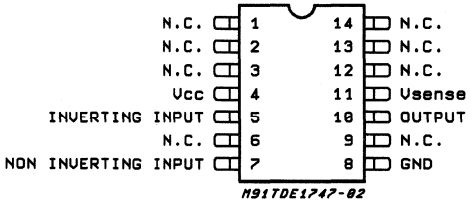
These device is essentially blow-out proof. Current limiting is available to limit the peak output current to safe values, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from overheating. If internals dissipation becomes too great, the driver will shut down to prevent excessive heating. TDE1747 has an open ground protection. The output is also protected from short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 used for industrial electronic systems.

PIN CONNECTIONS (Top view)



Minidip



SO14

ABSOLUTE MAXIMUM RATINGS

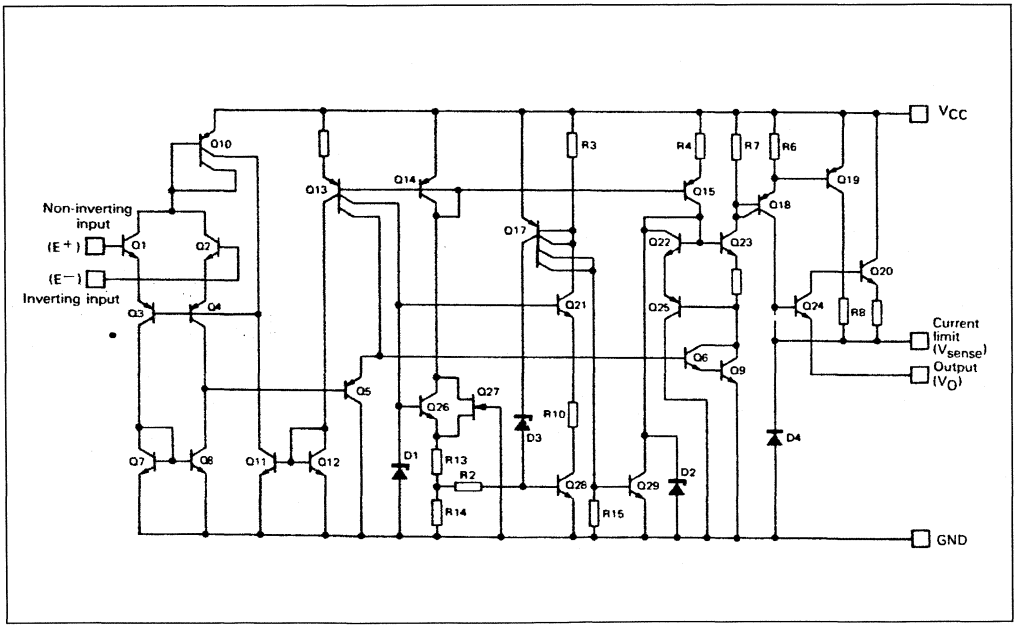
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	50 *	V
V_{ID}	Differantial Input Voltage	50	V
V_I	Input Voltage	50	V
I_O	Output Current	1	A
P_{tot}	Power Dissipation (T_{amb} = + 25 °C)	Internally Limited	W
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_{oper}	Operating Ambient Temperature Range TDE1747 TDF1747	 – 25 to + 85 – 40 to + 85	 °C °C

(*) 60V, t â 10ms

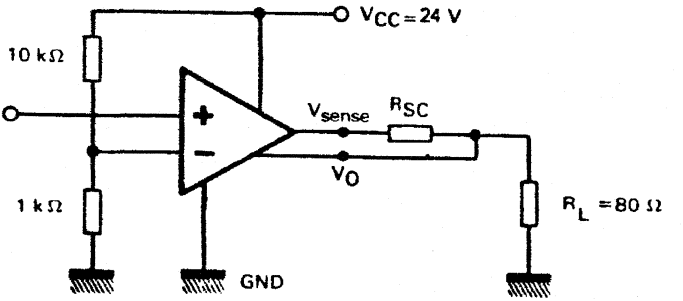
THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	50	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	120	°C/W
R_{th}	Junction-ceramic Substrate (case glued to substrate) SO14	90	°C/W
R_{th}	Junction-ceramic Substrate (case glued to substrate, substrate temperature maintened constant) SO14	65	°C/W

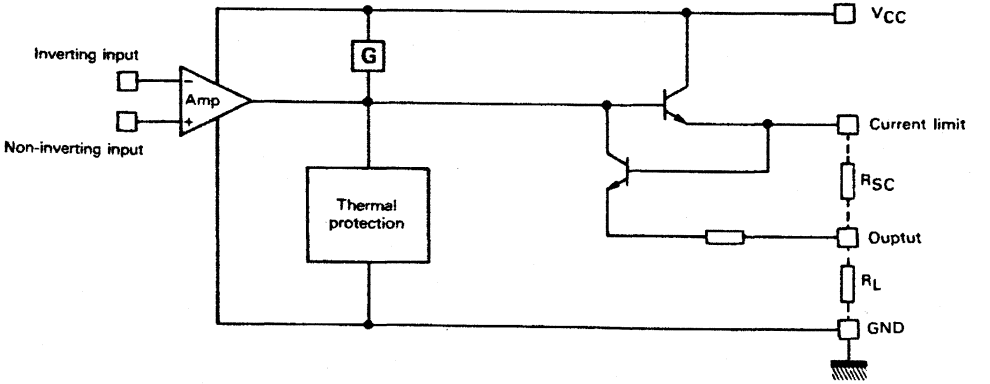
SCHEMATIC DIAGRAM



TEST CIRCUIT



SIMPLIFIED CIRCUIT



ELECTRICAL CHARACTERISTICS T_j = – 25 to +85 °C, V_{CC} = 8 to 45 V, unless otherwise specified (note 1).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage - (note 2)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	mA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0) High Level Low Level	 – –	 4 2	 6 4	 mA mA
$V_{I(max)}$	Common-mode Input Voltage Range	2	–	V_{CC}–2	V
I_{SC}	Short-circuit Current Limit (T_{amb} = + 25 °C, V_{CC} = + 24) R_{SC} = 1.5 Ω TDE1747 R_{SC} = ∞	 – –	 480 35	 – 50	 mA mA
V_{CC}–V_O	Output Saturation Voltage (output high) (R_{SC} = 0, V_{I+}–V_{I-} ≥ 50 mV) I_O = 300 mA, T_j = + 25 °C T_j = + 150 °C	 – –	 1.15 1.05	 1.4 1.3	 V V
I_{OL}	Low Level Output Current (V_O = 0, V_{CC} = + 24 V) T_j = + 25 °C	–	0.01	10	µA

Notes :

1) For operating at high temperature, the TDE/TDF1747, must be derated based on a + 150 C maximum junction temperature and a junction-ambient thermal resistance of 120 °C/W for Minidip and 100 °C/W for the SO14.

2) The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.

Figure 1: Available Output Current vs. Limiting Resistor

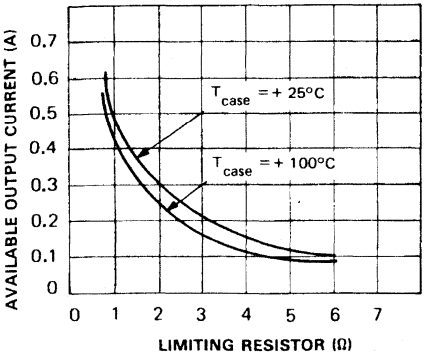


Figure 2: Peak Short-circuit Output Current vs. Limiting Resistor

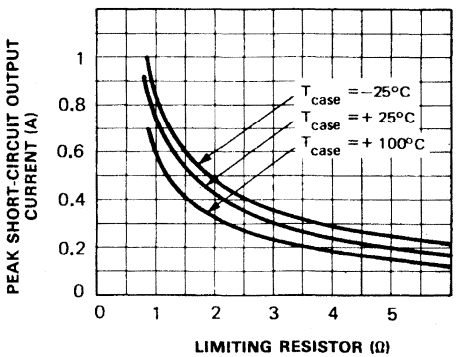


Figure 3: Short-circuit Current vs. Case Temperature

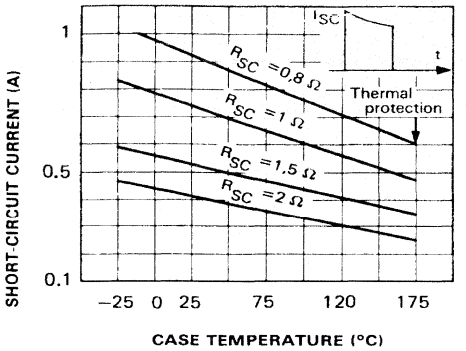


Figure 4: Minimum Limiting Resistor Value vs. Supply Voltage

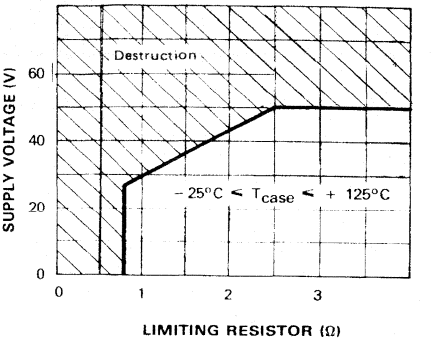


Figure 5: Output Current vs. Output Saturation Voltage

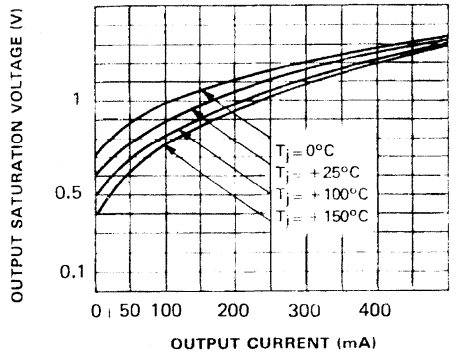


Figure 6: Supply Current vs. Supply Voltage

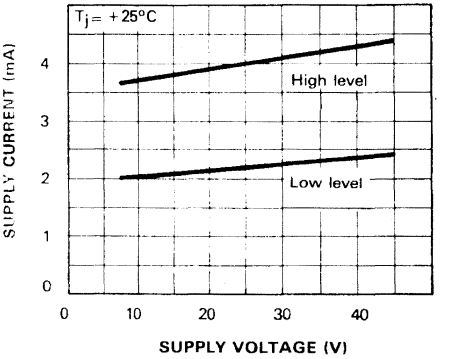


Figure 7: Supply Current vs. Junction Temperature

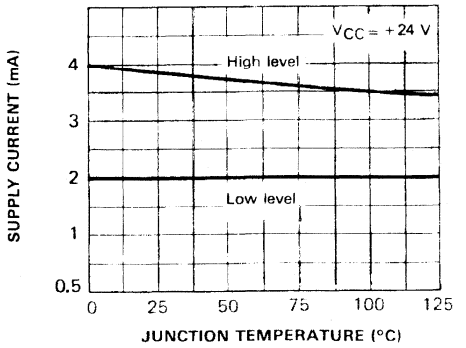


Figure 8: Safe Operating Area (non repetitive surge)

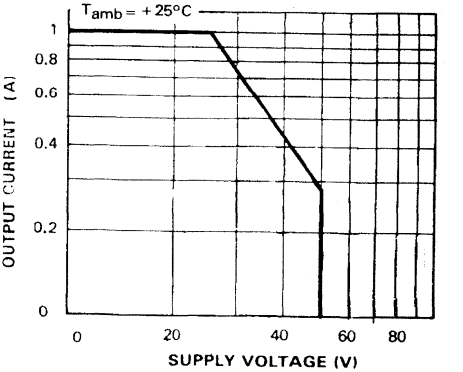
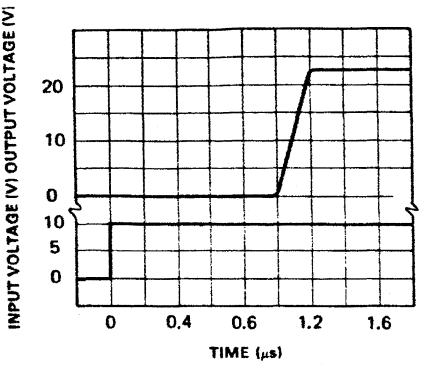
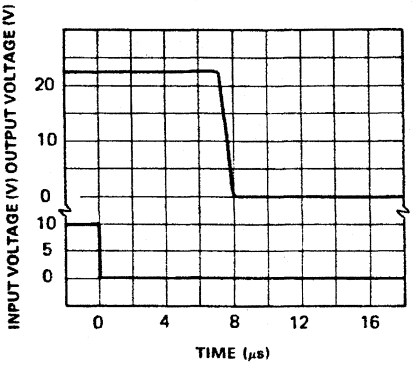


Figure 9: Response Time





TYPICAL APPLICATIONS

Figure 10: Base Circuit

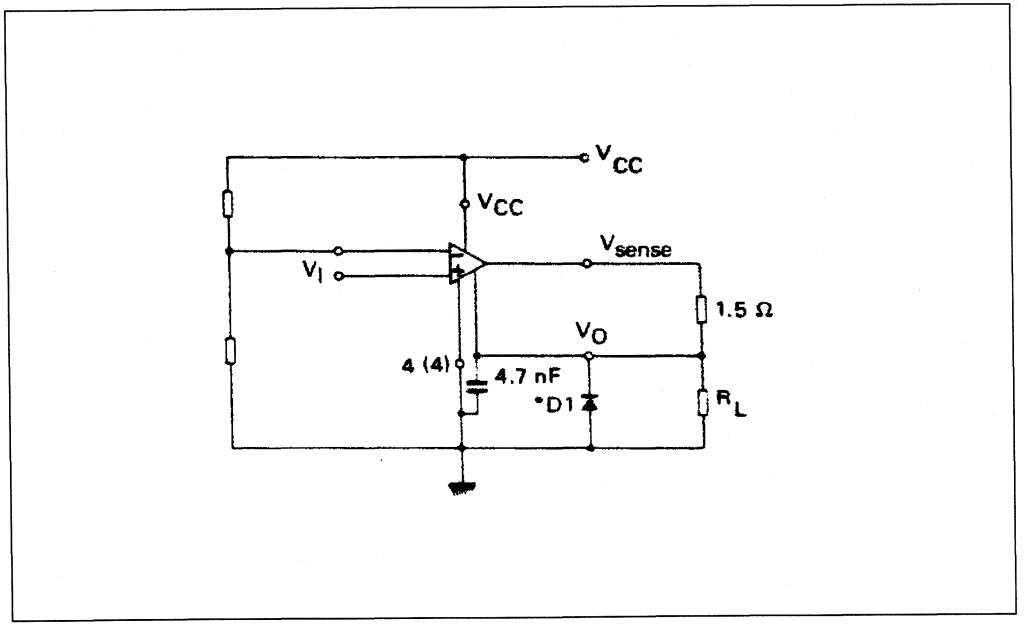


Figure 11: Output Current Extension (5A)

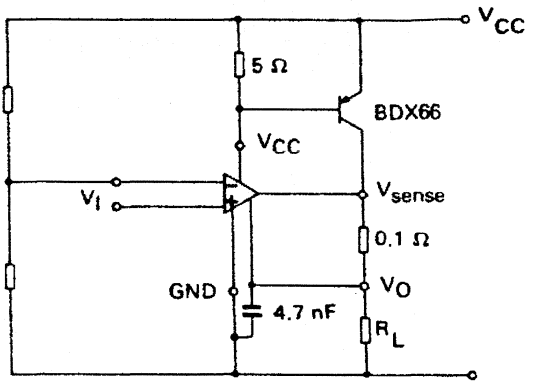
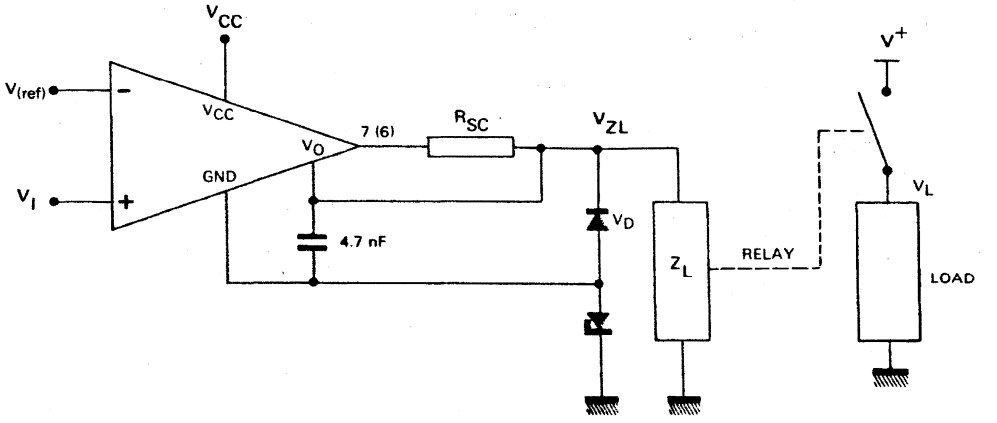
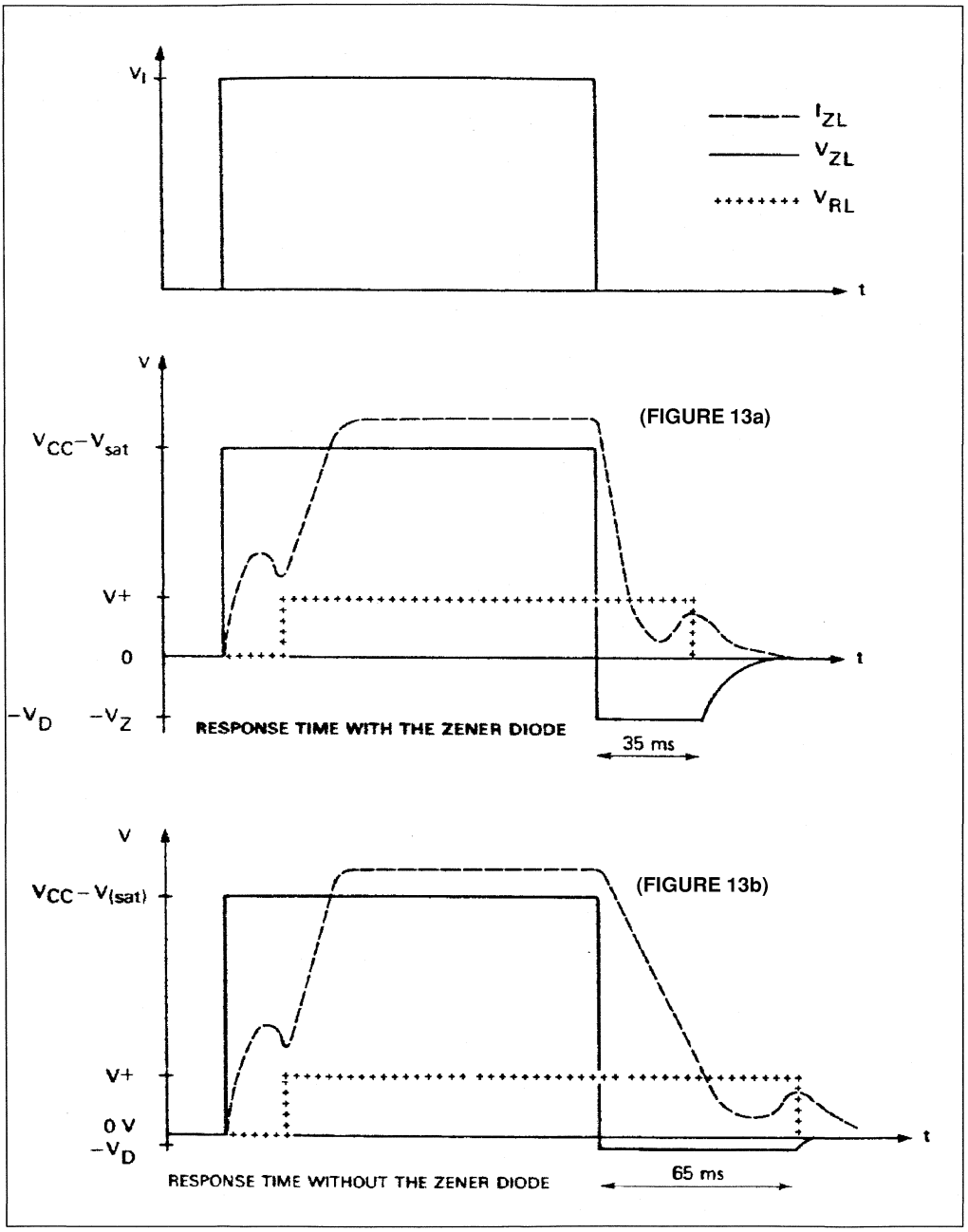


Figure 12: Driving Low Impedance Relays (I_O = 300mA)



The device in the above application operates at: V_{CC} = +45V, I_O = 300mA with a heatsink such that $R_{th(j-a)} \leq 80°C/W$. The device supports an output voltage of $V_{CC} = V_Z$ during the current cut off time, which is decreased by the zener diode. Thisvoltage must be ≤ to the maximum supply voltage.

Figure 13: Waveforms



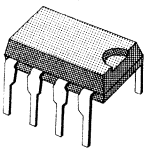
SGS-THOMSON MICROELECTRONICS

TDE1767,A
TDE1787,A

INTERFACE CIRCUIT (RELAY AND LAMP-DRIVER)

- OPEN GROUND PROTECTION
- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- INTERNAL THERMAL PROTECTION WITH EXTERNAL RESET
- LARGE SUPPLY VOLTAGE RANGE
- ALARM OUTPUT
- INPUT VOLTAGE CAN BE HIGHER THAN V_{CC}
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND ($V_{CC} - V_O \leq V_{CC}$ [max])

MINIDIP/2



ORDER CODES : TDE1767 DP
TDE1767 ADP
TDE1787 DP
TDE1787 ADP

DESCRIPTION

The TDE1767,A/TDE1787,A are monolithic amplifiers designed for high current and high voltage applications, specifically to drive lamps, relays, stepping motors.

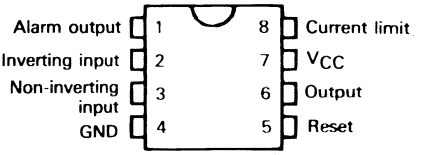
These devices are essentially blow-out proof. The output is protected from short-circuits with the positive supply or ground. In addition thermal shut down is provided to keep the IC from overheating. If internal dissipation becomes too high, the driver will shut down to prevent excessive heating. The output stays null after the overheating is off, if the reset input is low. If high the output will alternatively switch-on and off until the overload is removed.

The device operates over a wide range of supply voltages from standard 15 V operational amplifier supplies to the single + 6 V or + 48 V used for industrial electronic systems. Input voltages can be higher than the V_{CC}.

An alarm output suitable for driving a LED is provided. This LED, normally on (if referred to ground), will die out or flash during an overload depending on the state of the reset input.

The output is low in open ground conditions.

PIN CONNECTION (top view)



THERMAL DATA

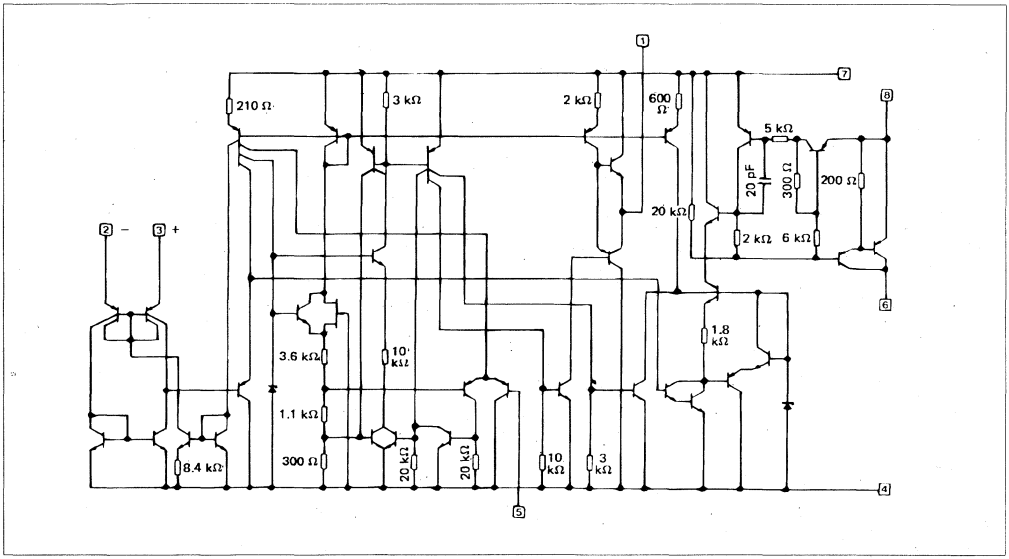
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	30	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance*	80	°C/W

* Devices bonded on a 40 cm2 glass-epoxy printed circuit 0.15 cm thick with 4 cm2 of copper.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TDE1767A/TDE1787A	TDE1767/TDE1787	Unit
V_{CC}	Supply Voltage	60	50	V
V_{ID}	Input Differential Voltage	60	50	V
V_I	Input Voltage	− 10 to + 60	− 10 to + 50	V
I_O	Output Current	1.2	1.2	A
$V_{I(reset)}$	Reset Input Voltage	− 0.5 to + 60	− 0.5 to + 50	V
I_{OA}	Alarm Output Current	− 10 to + 20	− 10 to + 20	mA
P_{tot}	Power Dissipation	Internally Limited		mW
T_{oper}	Operating Ambient Temperature Range	− 25 to + 85	− 25 to + 85	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	− 65 to + 150	°C

SCHEMATIC DIAGRAM



EQUIVALENT SCHEMATIC

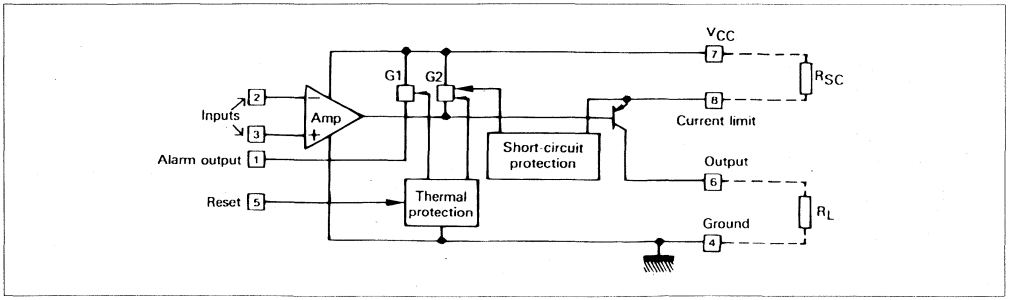
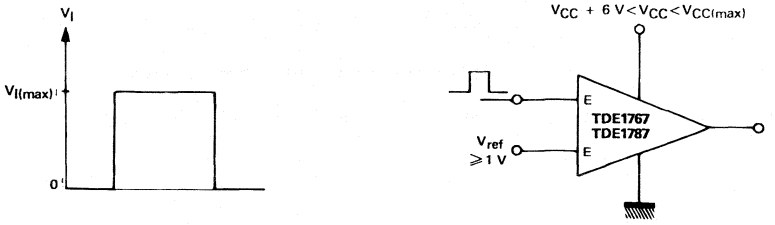


Figure 1.



The reference input can be the inverting or non-inverting one.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

TDE1767A : − 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 55 V, I_O ≤ 500 mA, T_j ≤ + 150 °C
TDE1767 : − 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 500 mA, T_j ≤ + 150 °C
TDE1787A : − 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 55 V, I_O ≤ 300 mA, T_j ≤ + 150 °C
TDE1787A : − 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ + 150 °C

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage - (note 1)			2	50	mV
I_{CC}	Power Supply Current (measured on pin 4)					mA
	Output High (T_{amb} = + 25 °C)		−	5.8	8	
	Output High (V_{CC} = $V_{CC\ (max)}$, T_j = + 150 °C)		−	5	7	
	Output Low (V_{CC} = $V_{CC\ (max)}$, T_{amb} = + 25 °C)		−	1.5	4	
I_{IB}	Input Bias Current		−	15	100	µA
V_{CM}	Common-mode Input Voltage Range	**TDE1787A, TDE1767A**	1	−	60	V
		TDE1787, TDE1767	1	−	45	
V_I	Input Voltage Range (V_{ref} ≥ + 1 V)	**TDE1787A, TDE1767A**	0	−	60	V
	(figure 1, note 2)	**TDE1787, TDE1767**	0	−	45	
I_{SC}	Short-circuit Output Current					mA
	(V_{CC} = + 35 V, t = 10ms)					
	R_{SC} = 0.22 Ω	**TDE1767A**	−	700	−	
	R_{SC} = 0.33 Ω	**TDE1787A**	−	380	−	
V_{sense}	Current Limit Sense Voltage: V_O = V_{CC} − 2 V, t = 10 ms		130	150	170	mV
	(V_O = V_{CC} − 2 V) : V_O = 0 V, t = 10 ms		120	140	165	
$V_{O(sat)}$	Output Saturation Voltage (output high $V_I^+ - V_I^- \geq 50$ mV,					V
	R_{SC} = 0, V_{CC} = + 30 V)					
	T_j = + 25 °C	**TDE1787A, TDE1767A**	−	1	1.1	
		TDE1787, TDE1767	−	1	1.2	
	T_j = + 150 °C	**TDE1787A, TDE1767A**	−	1.1	1.2	
		TDE1787, TDE1767	−	1.1	1.3	
I_{OL}	Output Leakage Current (output low)		−	−	100	µA
I_A	Available Alarm Output Current					mA
	Output Source Current (V_{AH} = V_{CC} − 2.5 V)		− 4	− 5	−	
	Output SInk Current (in thermal shut-down) V_A = 1.4 V		5	10	−	
I_{reset}	Reset Input Current		−	2	40	µA
$V_{th\ (reset)}$	Reset Threshold		−	1.4	−	V
−	Output Leakage Current (open ground)		−	10	−	µA

Notes : 1. The offset voltage given is the maximum value of differential input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.
2. Input voltage range is independent of the supply voltage.

Fig. 2 – PEAK SHORT-CIRCUIT CURRENT vs LIMITING RESISTOR.

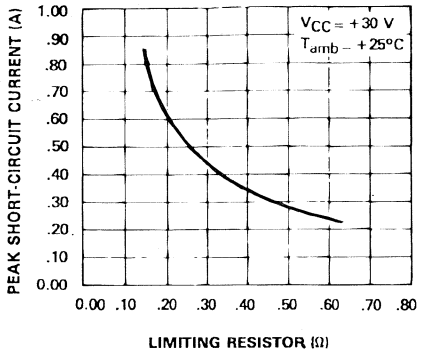


Fig. 3 – AVAILABLE OUTPUT CURRENT vs LIMITING RESISTOR.

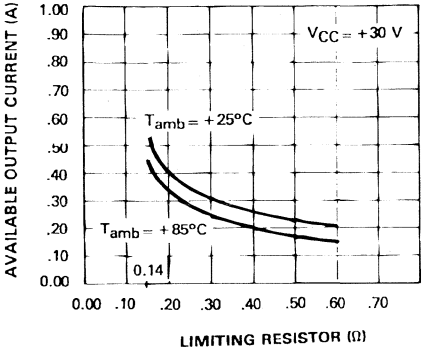


Fig. 4 – POWER SUPPLY CURRENT (pin 4).

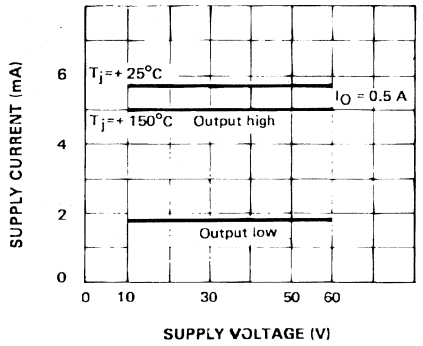


Fig. 5 – OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT.

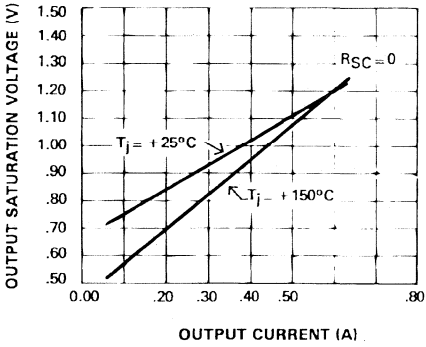


Fig. 6 – OUTPUT TRANSISTOR SAFE OPERATING AREA (pulsed).

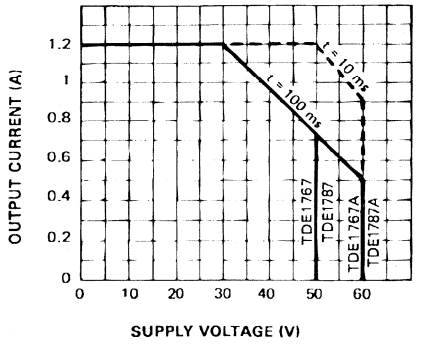
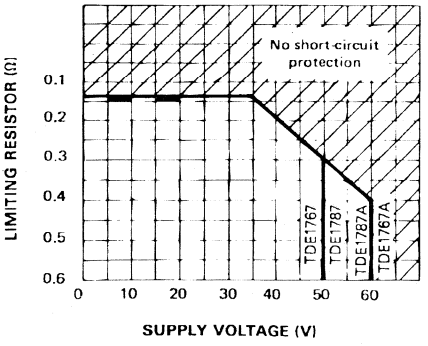


Fig. 7 – NORMAL OPERATING AREA (short-circuit protected).



ALARM OUTPUT CAPABILITY CURRENT

Fig. 8 CURRENT SINKING.

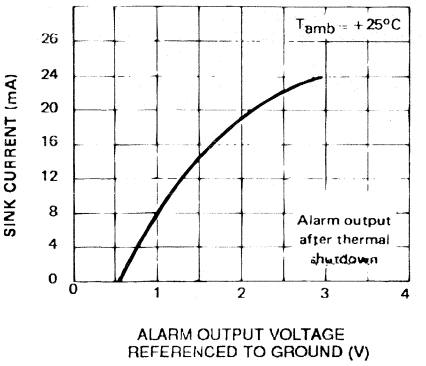


Fig. 9 – CURRENT SOURCING

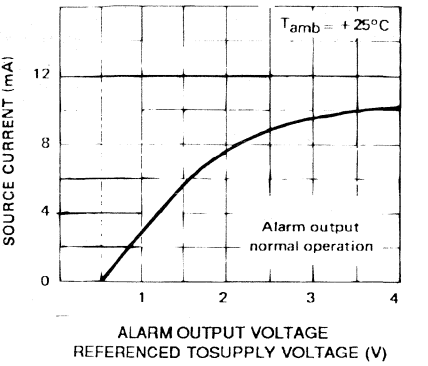


Fig. 10 – RESPONSE TIME.

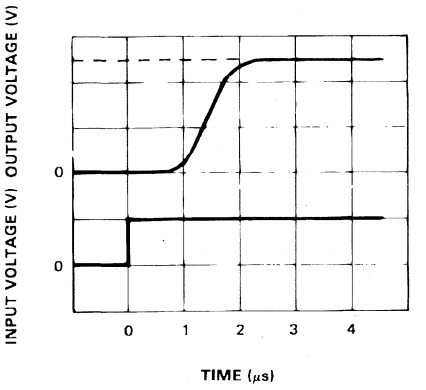


Fig. 11 – RESPONSE TIME.

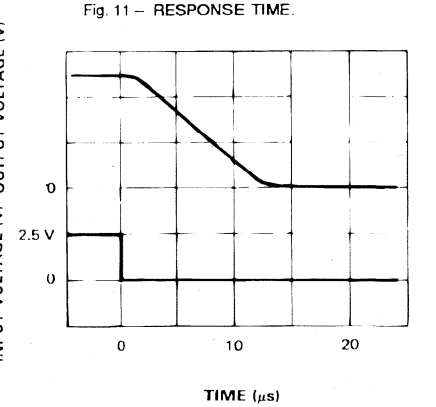
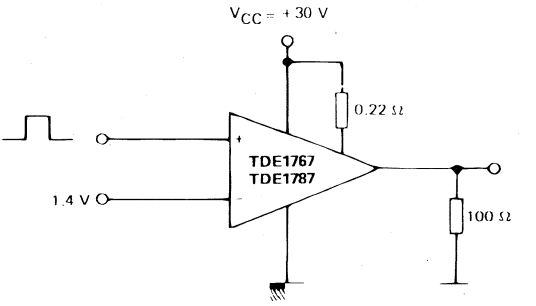


Figure 12 : Test Circuit.



TYPICAL APPLICATIONS

Figure 13 : Open Load Detection.

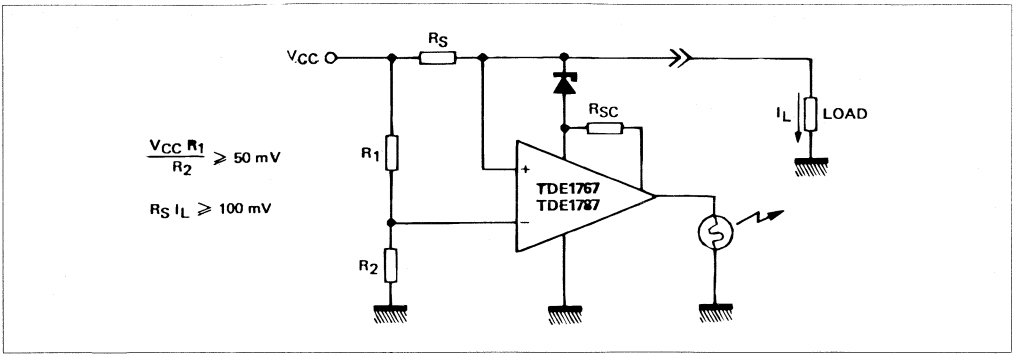


Figure 14 : Driving Lamps, Relays, Etc...

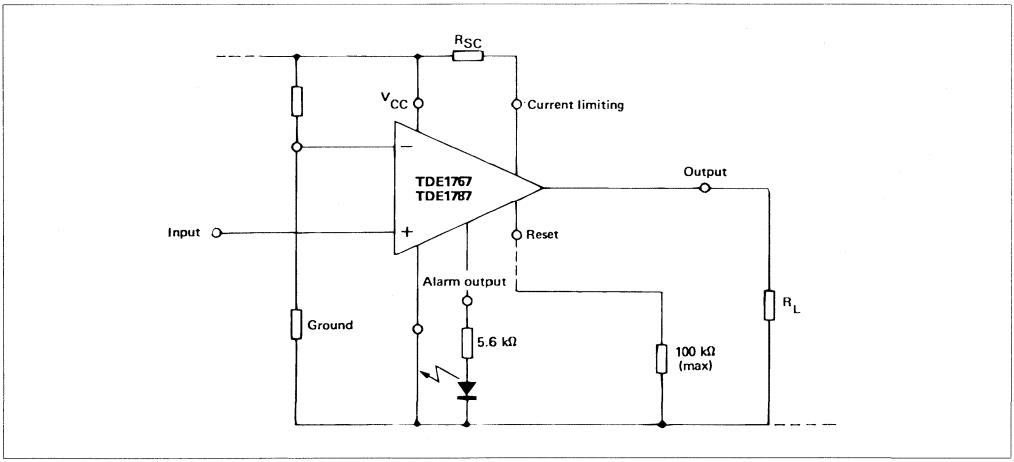


Figure 15 : Common Reset.

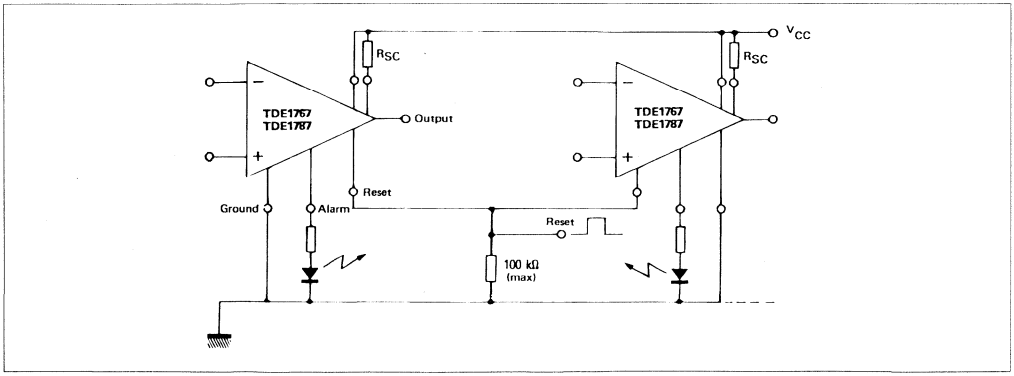
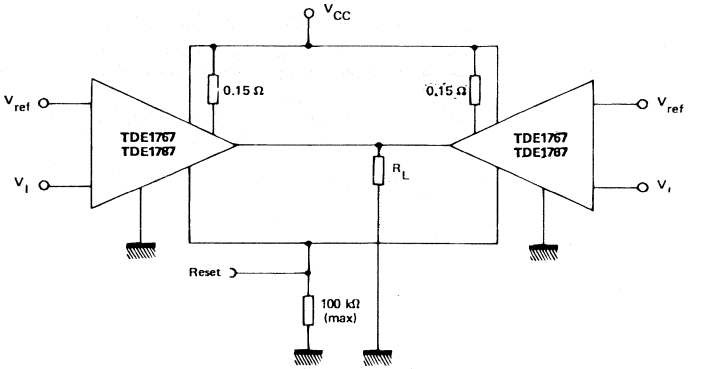


Figure 16 : Parallel Driving of Loads Up to 1 A.



USING ALARM OUTPUT

Figure 17 : Parallel Alarm Outputs.

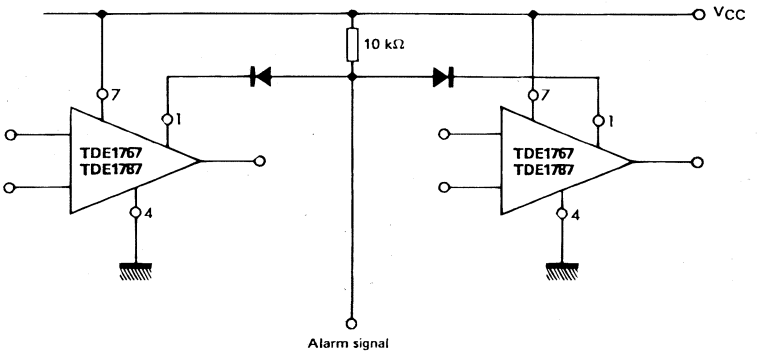


Figure 18 : Led to VCC.

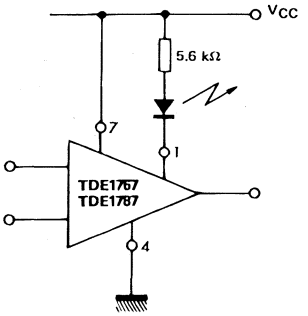


Figure 19 : Led to Ground.

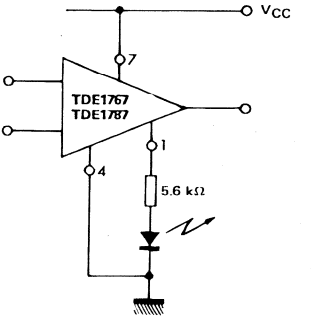


Figure 20 : Interface between High Voltage and Low Voltage Systems.

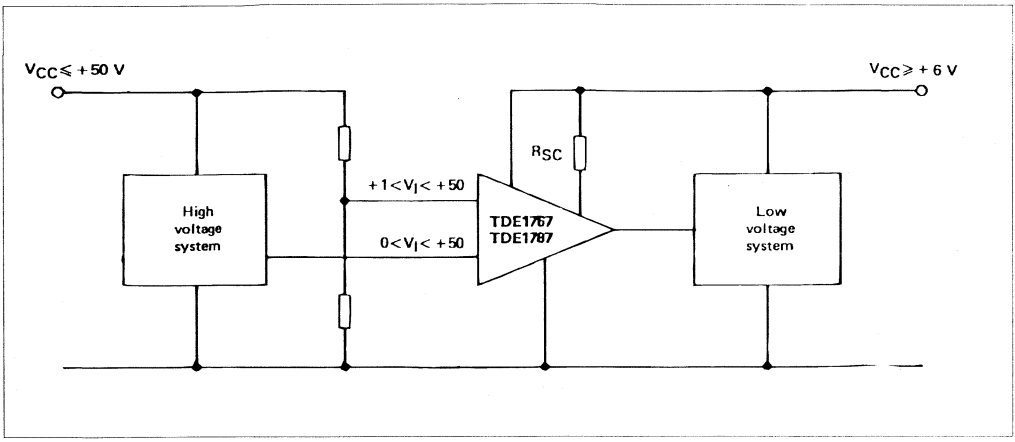
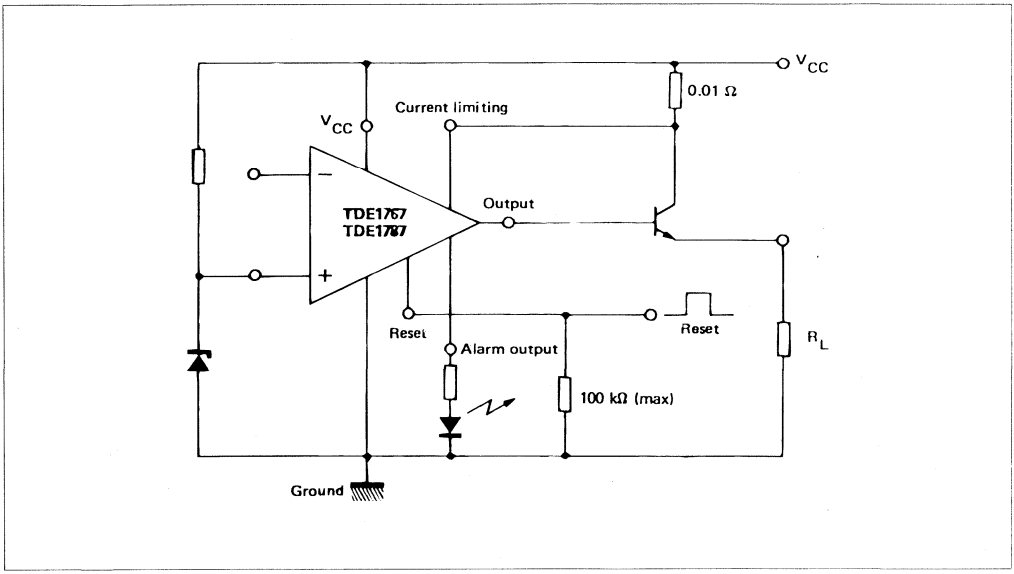


Figure 21 : Increasing Output Current Up to 10 A.

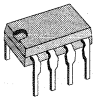


SGS-THOMSON MICROELECTRONICS

TDE1798

0.5A INTELLIGENT POWER SWITCH

- HIGH OUTPUT CURRENT 500mA
- SHORT-CIRCUIT PROTECTION UP TO V_{CC} = +35V
- INTERNAL THERMAL PROTECTION WITH EXTERNAL RESET AND SYNCRONIZATION CAPABILITY
- OPEN GROUND PROTECTION
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND FOR FAST INDUCTIVE LOAD DEMAGNETIZATION
- DIFFERENTIAL INPUTS FOR ANY LOGIC SYSTEM COMPATIBILITY
- INPUT VOLTAGE CAN BE HIGHER THAN V_{CC}
- LARGE SUPPLY VOLTAGE RANGE FROM 6V TO 35V
- SINK AND SOURCE ALARM OUTPUTS
- NO NEED FOR EXTERNAL CLAMPING DIODE FOR DEMAGNETIZATION ENERGY UP TO 150mJ
- SEVERAL DEVICES CAN BE CONNECTED IN PARALLEL

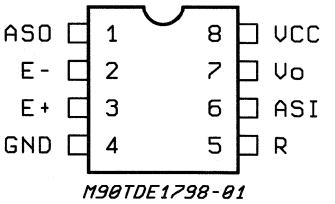


Minidip
ORDERING NUMBER: TDE1798DP

DESCRIPTION

The TDE1798 is an interface circuit delivering high currents and capable of driving any type of loads.
The output is protected from short-circuits with the positive supply or ground. In addition thermal shut down is provided to keep the IC from overheating. If internal dissipation becomes too high, the driver will shut down to prevent excessive heating. The output stays null after the overload is off, if the reset input is low. If high, the output will alternatively switch on and off until the overload is removed.
Higher current can be obtained by paralleling the outputs of several devices. In this case, the devices can be reactivated simultaneously after an overload if their reset input are connected in parallel.
The device operates over a wide range of supply voltages from standard ±15 operational amplifier supplies to the single ±6V or +35V used for industrial electronic systems. Input voltage can be higher than the V_{CC}. The output is low in open ground conditions.

PIN CONNECTION (Top view)

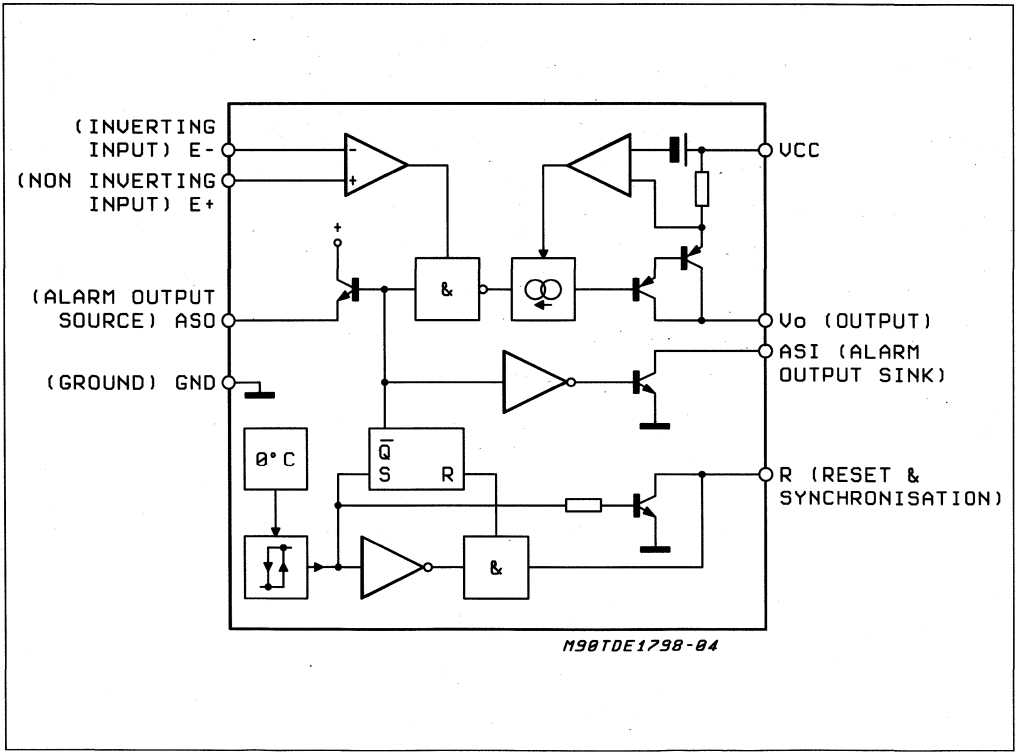


M90TDE1798-01

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	Supply Voltage	50	V
V_{ID}	Input Differential Voltage	50	V
V_I	Input Voltage	-30 to +50	V
$V_{I(reset)}$	Reset Input Voltage	VCC -50 to V_{CC}	V
I_O	Output Current	internally limited	A
P_{tot}	Power Dissipation	Internally Limited	mW
	Reset Input Sink Current (in thermal shut-down)	15	mA
W_D	Repetitive Maximum Demagnetization Energy - 10^6 Operations	150	mJ
T_{op}	Operating Ambient Temperature Range	-25 to -85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
$I_{A(sink)}$	Alarm Output Sink Current	25	mA
$I_{A(source)}$	Alarm Output Source Current	12	mA

BLOCK DIAGRAM



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case (1)	max.	30	°C/W
$R_{th\ j\text{-}ambient}$	Thermal Resistance Junction-ambient (1)	max.	90	°C/W

1) Devices bounded on a 40cm^2 glass-epoxy printed circuit 0.15cm thick with 4cm^2 of copper

ELECTRICAL CHARACTERISTICS (note 2)

TDE -25°C ≤ T_j ≤ +85°C, 6V ≤ V_{CC} ≤ +35V, I_o ≤ 500mA (unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage	(note 3)	–	2	50	mV
I_{CC}	Power Supply Current	Output High (Tamb = +25°C, I_o = 500mA) Output Low	– –	6.5 2	8 4	mA mA
I_{IB}	Input Bias Current		–	15	40	µA
V_{ICR}	Common-mode Input Voltage Range	(note 4)	1	–	45	V
V_I	Input Voltage Range	V_{ref} > +1V, (note 4 and 5)	-25	–	45	V
I_{SC}	Short-circuit Output Current	V_{CC} = 30V, t = 10ms	0.7	0.9	1.3	A
V_{CC} - V_O	Output Saturation Voltage	I_O = 500mA ($\|V^+ I - V^- I\|$ > 50mV)	–	1	1.25	V
I_{OL}	Output Low Leakage Current	T_j = +85°C (V_{CC} = 30V, V_O = 0V)	–	10	100	µA
$I_{(pin\ 1)\ source}$ $I_{(pin\ 6)\ sink}$	Available Alarm Output Current	Source ($V_{(pin\ 1)}$ = V_{CC} - 2.5V) Sink (in thermal shut-down) $V_{(pin\ 6)}$ = 2V	4 6	8 15	– –	mA mA
I_{RH} I_{RL}	Reset Input Current		– -1	15 0	40 +1	µA µA
V_{th}	Reset Threshold		0.8	1.4	2	V
I_{reset}	Reset Output Sink Current	(in thermal shut-down) for V_{reset} ≤ +0.8V	2	–	–	mA
$I_{OL(open\ GND)}$	Output Leakage Current	(open ground)	–	10	100	µA
V_{BRVEO}	Output Transistor Avalanche Volt.	V_{CC} - V_O	65	–	110	V

Notes:

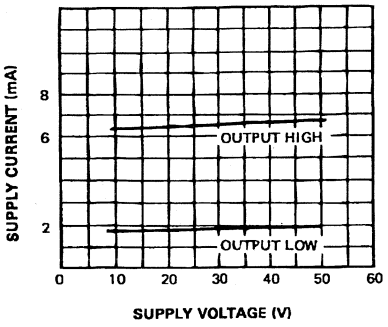
2) For operating at high temperature, the TDE1798 must be derated based on a 150°C maximum junction temperature and the junction-ambient thermal resistance.

3) The offset voltage given is the maximum value of input differential voltage required to drive the output voltage within 2V of the ground or the supply voltage;

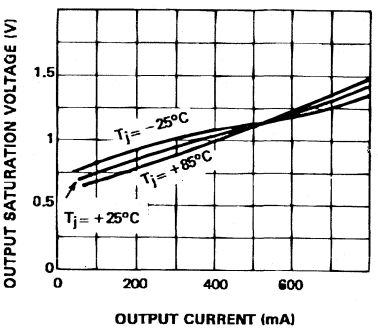
4) Input voltage range is independent of the supply voltage;

5) The reference input can be the inverting or the non-inverting one.

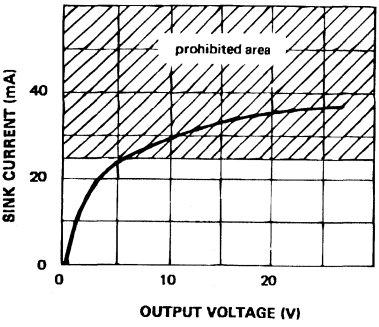
POWER SUPPLY CURRENT.



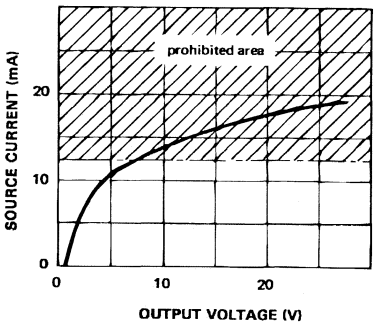
OUTPUT SATURATION VOLTAGE.



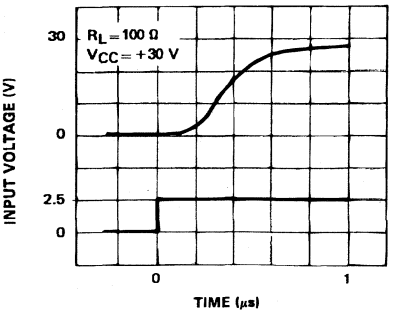
ALARM OUTPUT CURRENT SINK
(after thermal shut down).

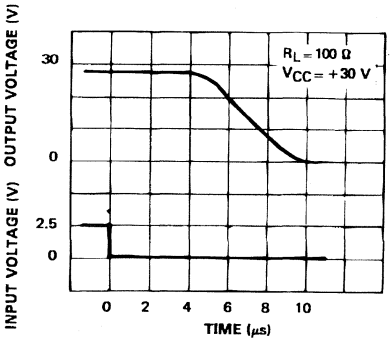


ALARM OUTPUT CURRENT SOURCE
(normal operation).

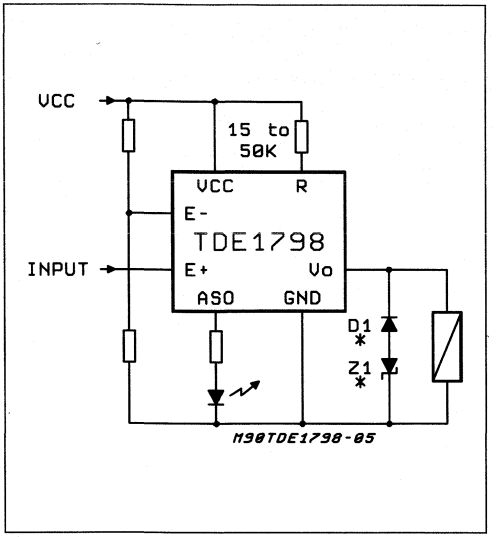


RESPONSE TIME.

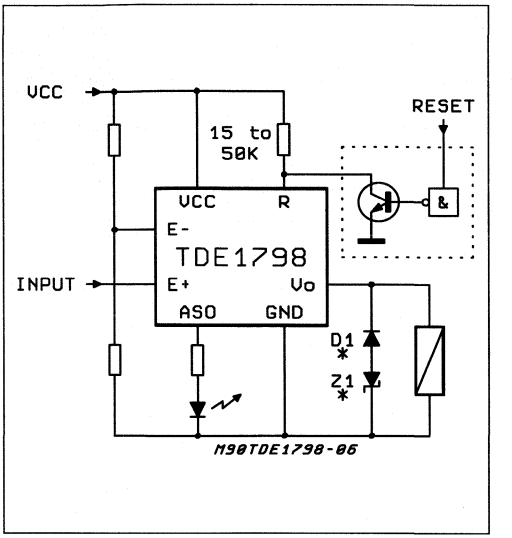




TYPICAL APPLICATION AUTOMATIC RESET

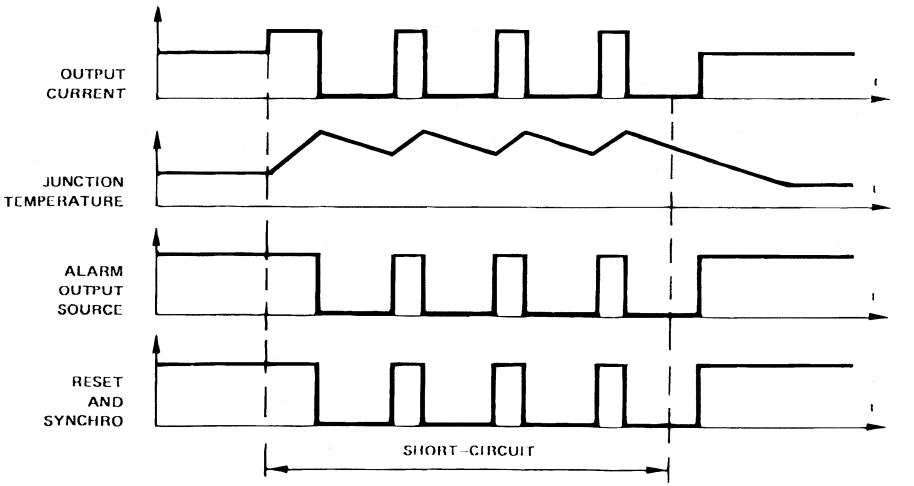


TYPICAL APPLICATION CONTROLLED RESET

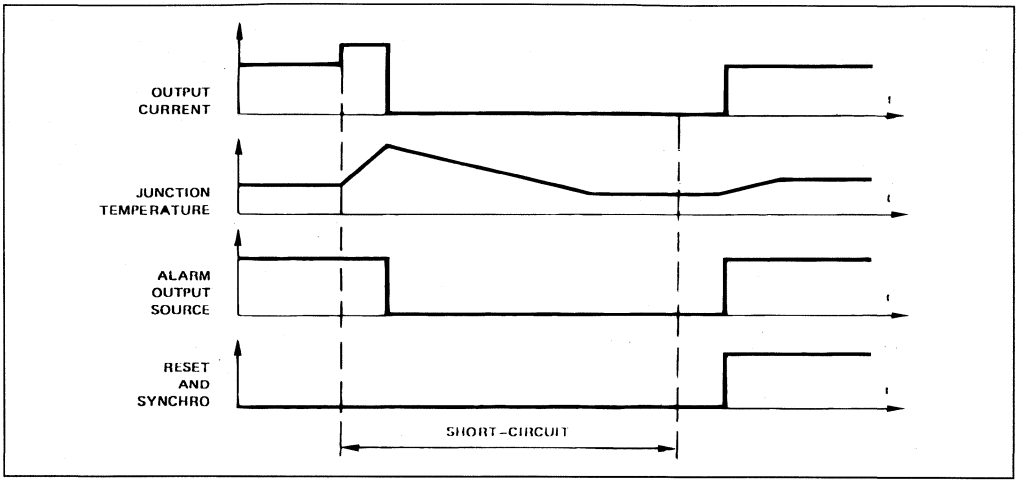


(*) D1 and Z1 needed if the demagnetization energy is higher than 150mJ

SHORT CIRCUIT CONDITIONS WITH AUTOMATIC RESET



SHORT CIRCUIT CONDITIONS WITH CONTROLLED RESET



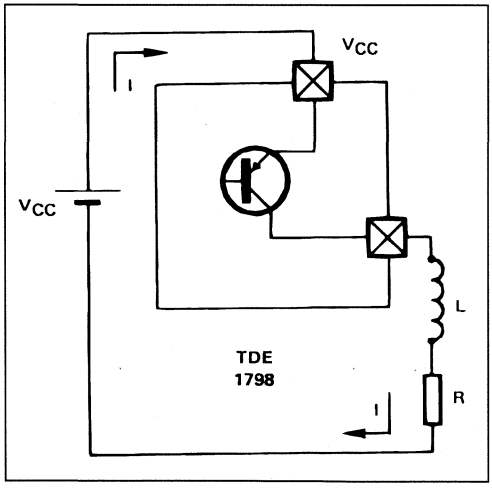
DEMAGNETIZATION OF INDUCTIVE LOADS WITHOUT EXTERNAL CLAMPING DEVICES.

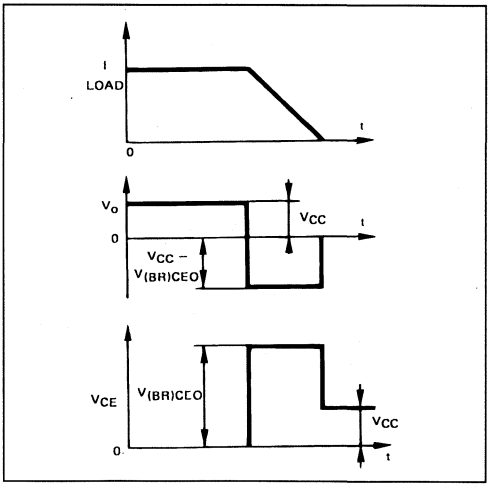
With no external clamping device, the energy of demagnetization is dissipated in the TDE1798 output stage, and the clamping voltage is the collector -emitter breakdown voltage $V_{(BR)CEO}$.

This method provides a very fast demagnetization of inductive loads and can be used up to 150 mJ.

The amount of energy W dissipated in the output stage during a demagnetization is :

$$W = V_{(BR)} \frac{L}{R} \left[I_o - \frac{V_{(BR)} - V_{CC}}{R} \text{Log} \left(1 + \frac{V_{CC}}{V_{(BR)} - V_{CC}} \right) \right]$$

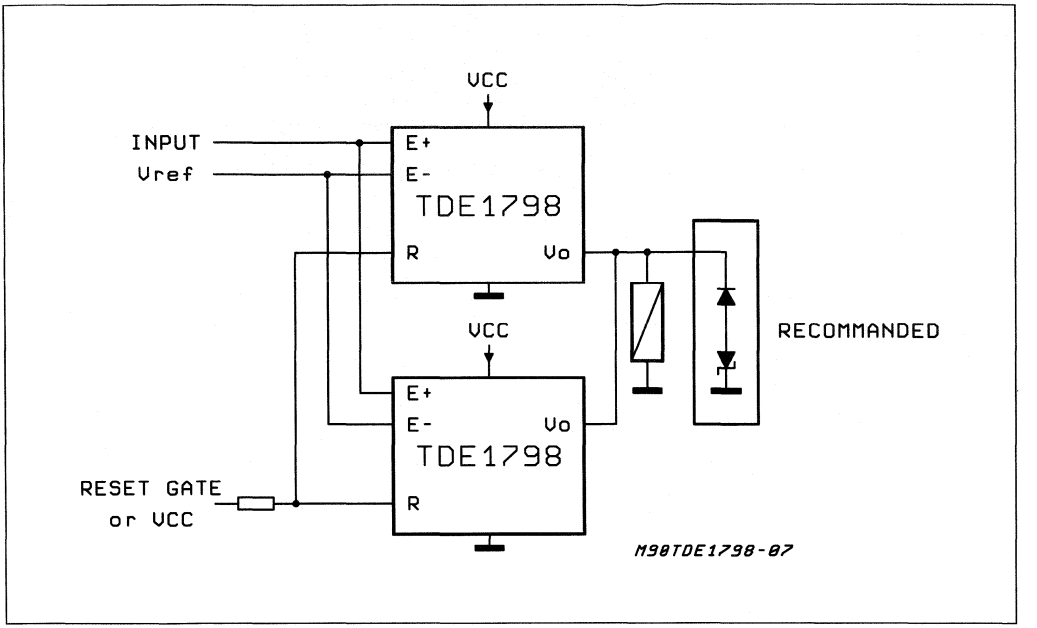




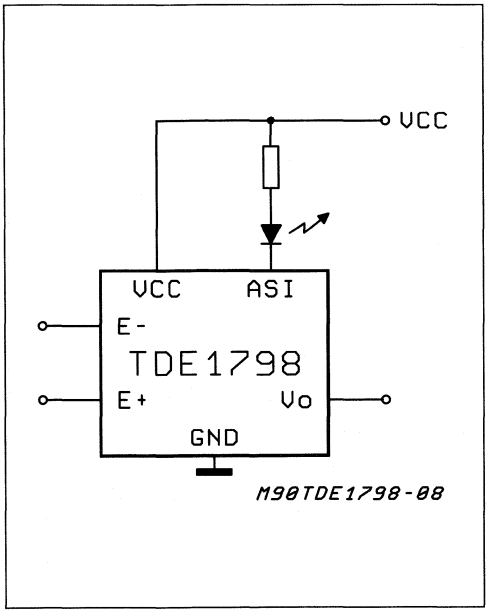
Remark 1 : This energy is dissipated inside the case, then must be included in the whole power dissipation.

Remark 2 : The use of external clamping device is recommended in case of parallel driving of loads. The dispersion of the collector-emitter breakdown voltage V(BR) would induce the circuit with the lowest V(BR) to dissipate the whole demagnetization energy (which is roughly proportionnal to I_O^2).

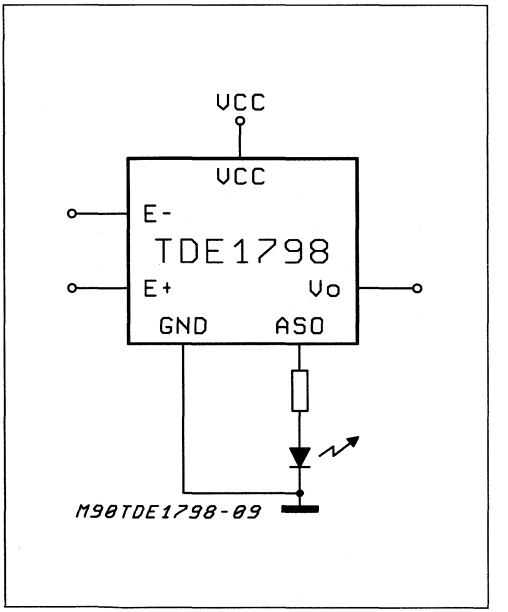
A 1 AMP. DRIVER (reset may be either automatic or controlled)



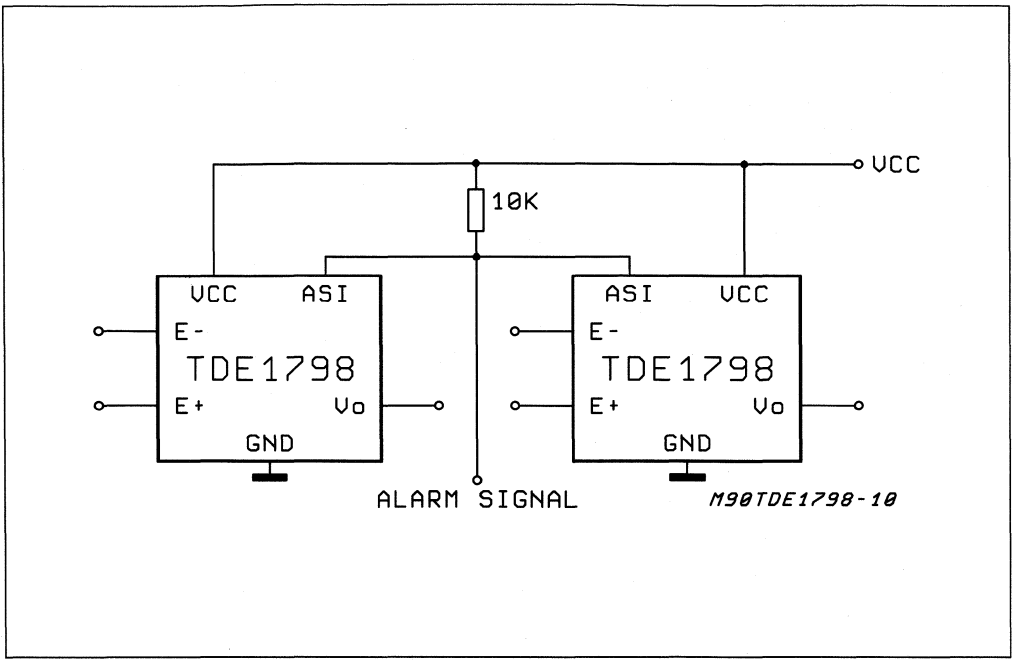
ALARM OUTPUT SINK



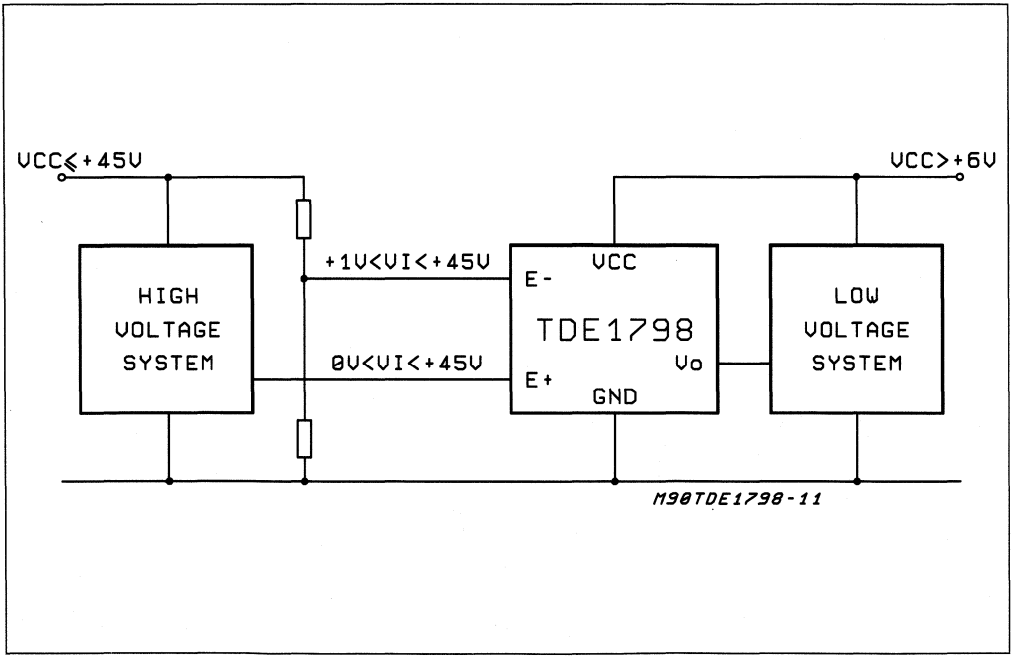
ALARM OUTPUT SOURCE



PARALLEL ALARM OUTPUTS



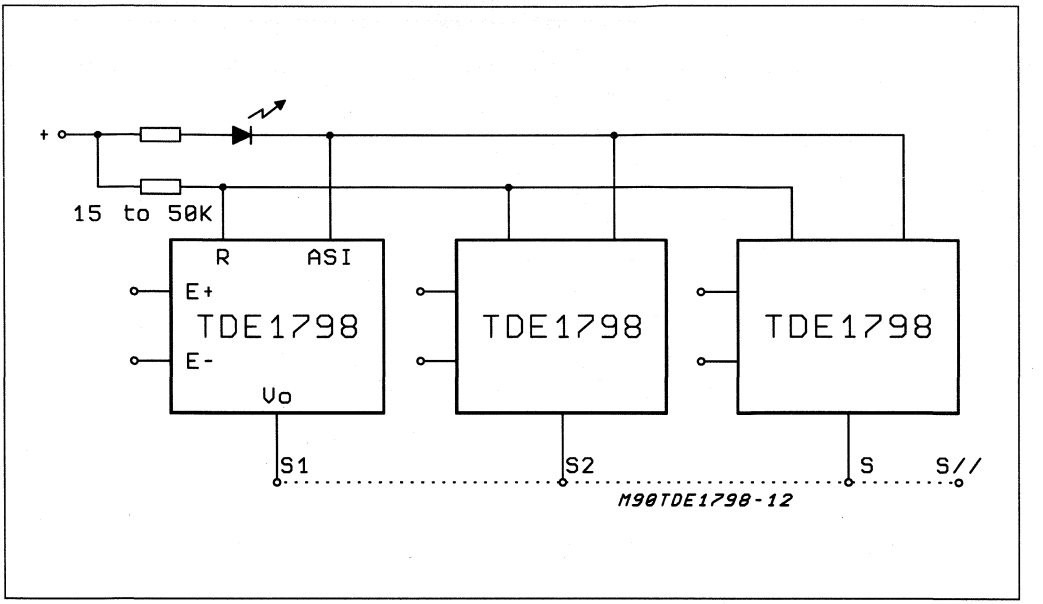
INTERFACE BETWEEN HIGH VOLTAGE AND LOW VOLTAGE SYSTEM



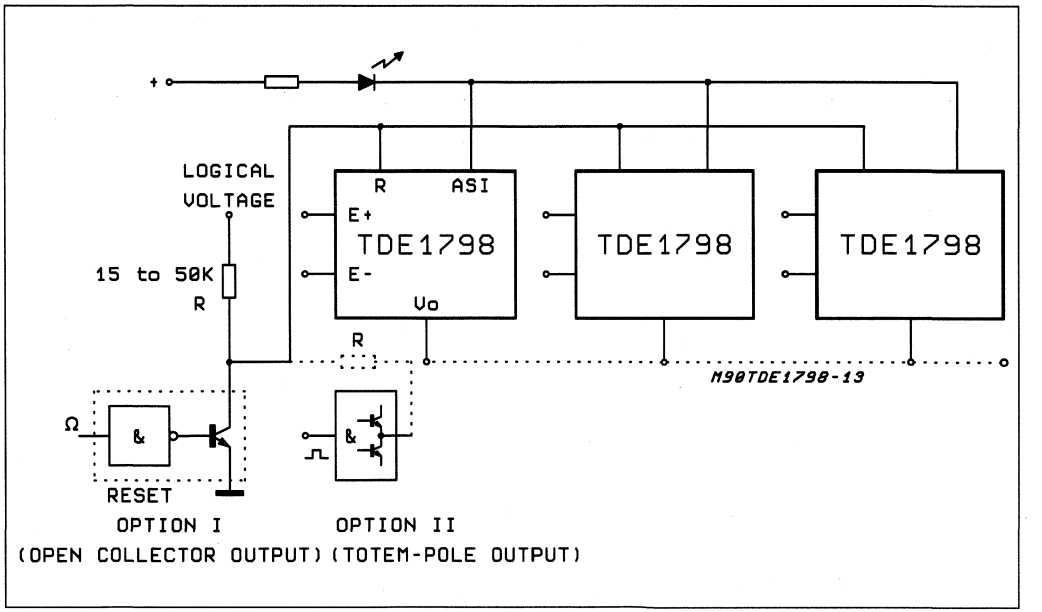
RESET AND SYNCHRONIZATION

Recommended diagram when the outputs are in parallel. After thermal disjunction a restart is possible when all the circuits are returned in operating conditions.

SYNCRONOUS AUTOMATIC RESET (parallel or independent outputs)



SYNCHRONOUS CONTROLLED RESET (parallel or idependent outputs)

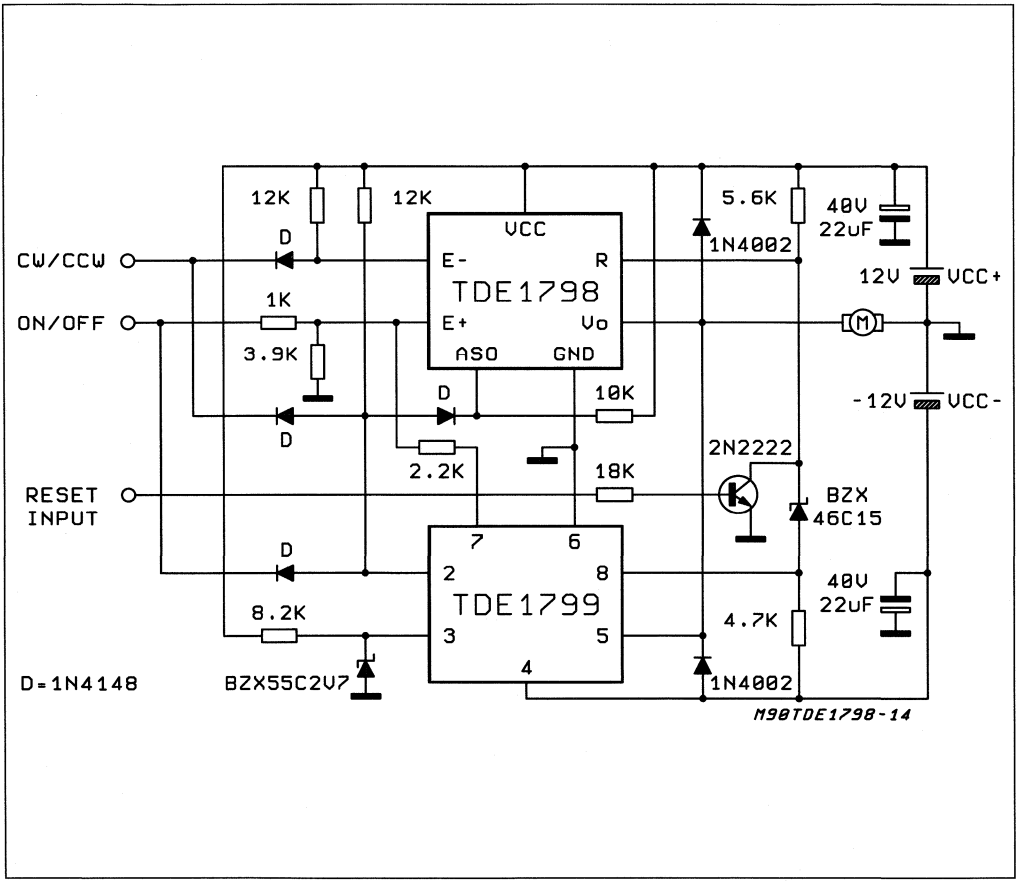


TWO QUADRANTS D.C. MOTOR DRIVE

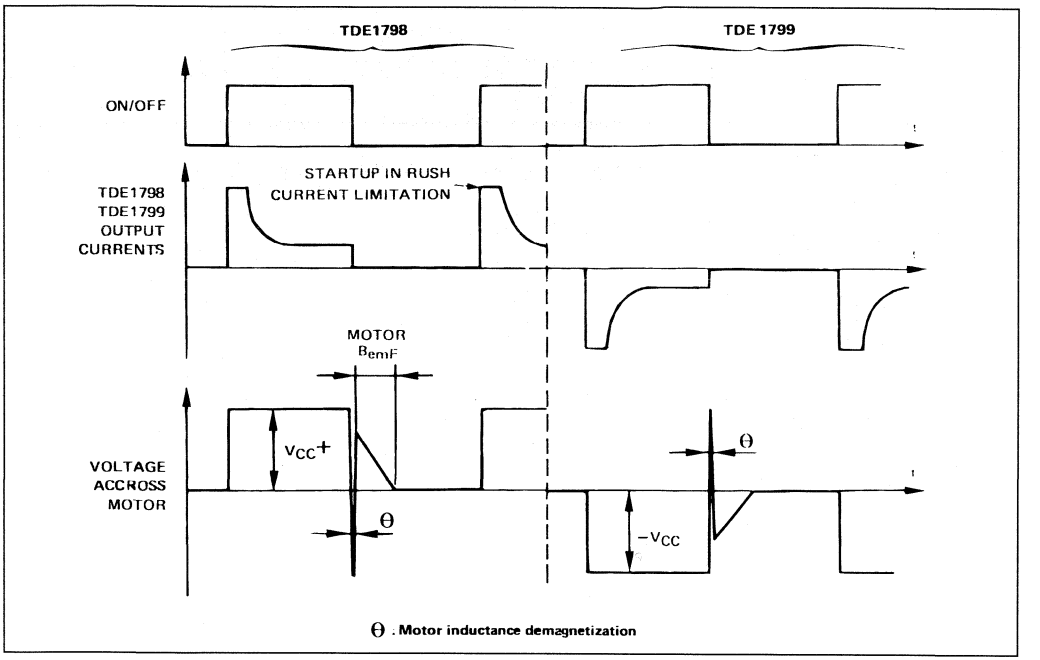
MAIN FEATURES

- V_{CC} - $V_{CC} \leq 50V$
- Maximum output current 0.5A
- Full protection against overloads and short-circuits
- No need of deadtime during rotation reversing
- TTL compatible inputs
- TDE1799 and TDE1798 input signals have the same reference
- No automatic restart after disjunction

CW/CCW	ON PFF	1798	1799
0	0	OFF	OFF
0	1	ON	OFF
1	1	OFF	ON
1	0	OFF	OFF

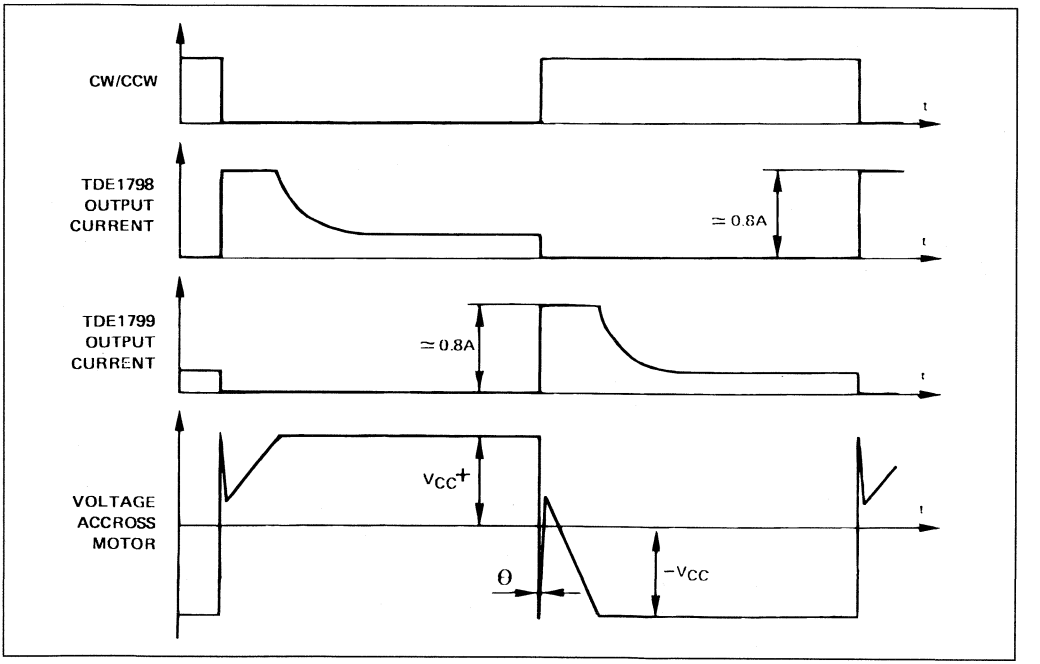


ON/OFF CYCLES

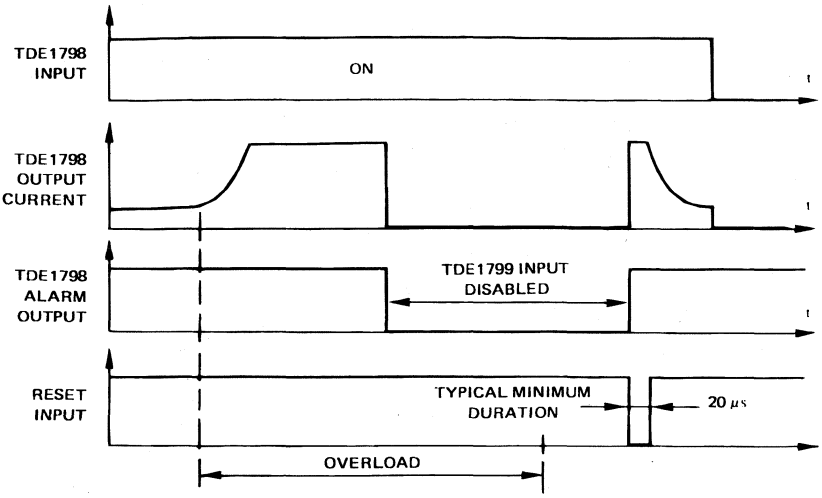


θ . Motor inductance demagnetization

ROTATION REVERSING



OVERLOAD CONDITIONS



* For instance overload during TDE1798 operation

SGS-THOMSON MICROELECTRONICS

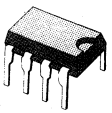
TDE3237

INTELLIGENT POWER SWITCH

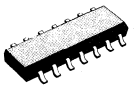
ADVANCE DATA

- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 8 V TO 30 V

MINIDIP/2



SO14J



ORDER CODES : TDE3237DP (MINIDIP)
TDE3237FP (SO14J)

DESCRIPTION

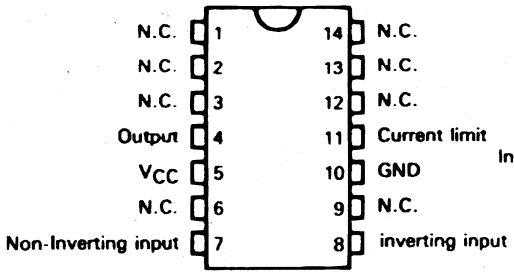
The TDE3237 is a monolithic amplifier designed for high current and high voltage applications, specially to drive lamps, relays and control of stepper motors.

This device is essentially blow-out proof. Current limiting is available to limit the peak output current to a safe value, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from over heating. If external dissipation becomes too great, the driver will shut down to prevent excessive heating.

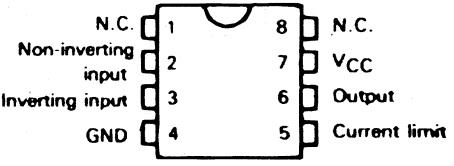
The output is also protected against short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 V used for industrial electronic systems.

PIN CONNECTIONS (top views)



SO14J



MINIDIP

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

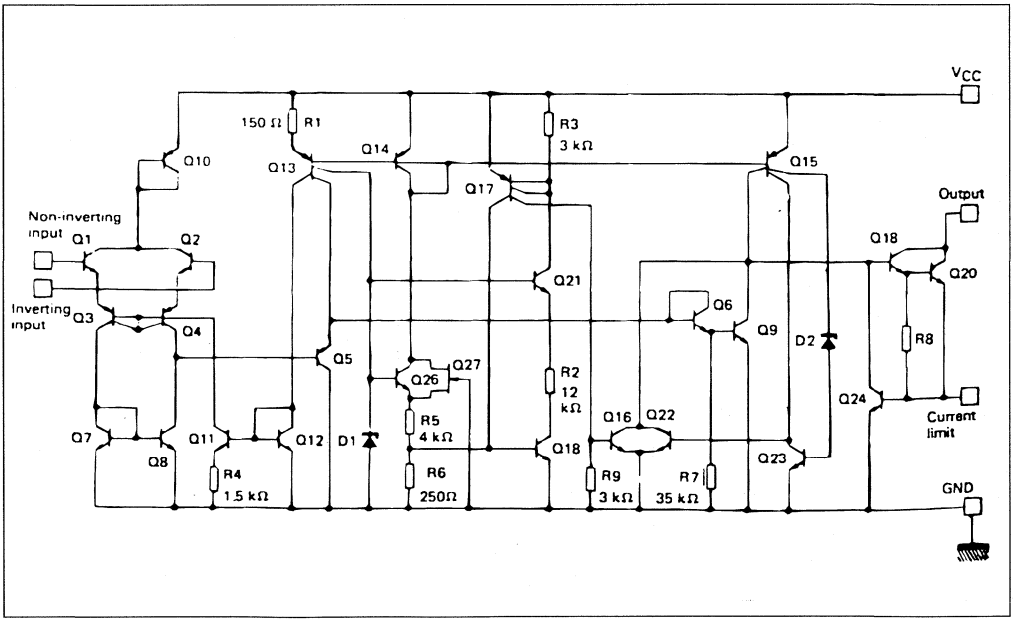
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_I	Input Voltage	36	V
V_{ID}	Differential Input Voltage	36	V
I_O	Output Current	500	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Free–air Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction–case Thermal Resistance (note 1)	Minidip	50	°C/W
$R_{th(j-a)}$	Maximum Junction–ambient Thermal Resistance (note 1)	Minidip	120	°C/W
–	Junction–ceramic Substrate (case glued to substrate)	SO14	90	°C/W
–	Junction–ceramic Substrate (case glued to substrate, substrate temperature maintened constant)	SO14	65	°C/W

Note : 1. Devices bonded on 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of copper.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

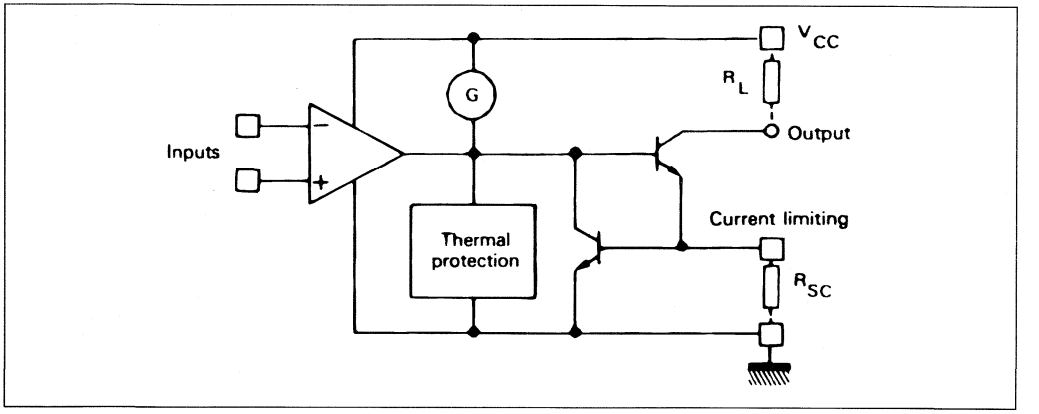
- 25 °C < T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ 30 V, I_O ≤ 150 mA, T_j ≤150 °C (note 2) (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (note 3)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	µA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0)	–	3	5	mA
V_{CM}	Common–mode Input Voltage Range	2	–	V_{CC} –2	V
I_{SC}	Short–circuit Current Limit (R_{SC} = 3.3 Ω, T_{case} = + 25 °C)	–	230	–	mA
V_{CC}–V_O	Output Saturation Voltage (output low) ($V_I^+ - V_I^-$ > 50 mV, I_O = 150 mA, R_{SC} = 0)	–	1	1.5	V
I_{OL}	Output Leakage Current (output high) (V_O = V_{CC} = + 24 V, T_{amb} = + 25 °C)	–	–	100	µA

Notes : 2. For operating at high temperatures, the TDE3237 must be derated on a 150 °C maximum junction temperature and a junction-ambient thermal resistance as showed in the thermal characteristics data base.

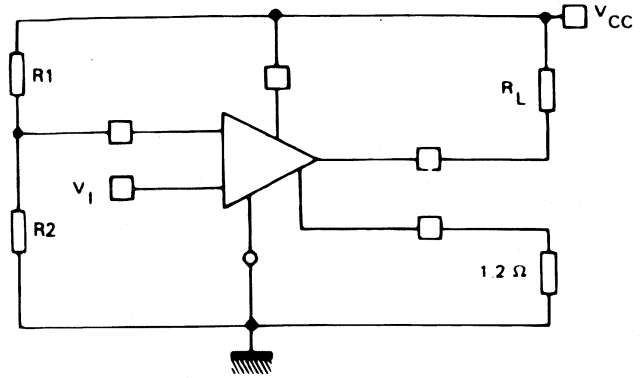
3. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.

SIMPLIFIED SCHEMATIC

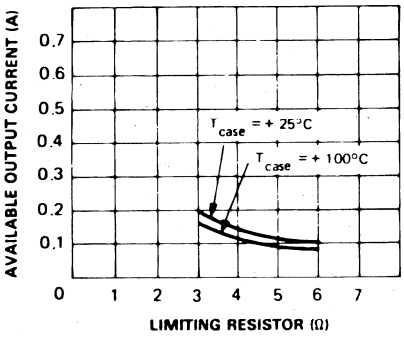


TYPICAL APPLICATION

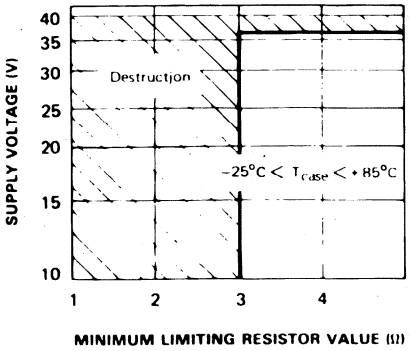
BASIC CIRCUIT



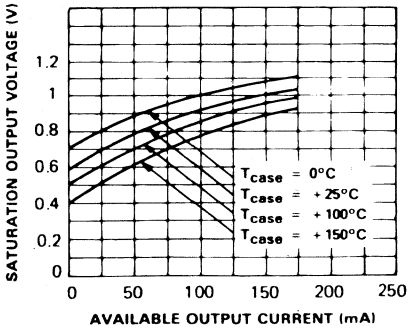
AVAILABLE OUTPUT CURRENT VERSUS LIMITING RESISTOR



SUPPLY VOLTAGE VS MINIMUM LIMITING RESISTOR VALUE



SATURATION OUTPUT VOLTAGE VERSUS CASE TEMPERATURE AND AVAILABLE OUTPUT CURRENT



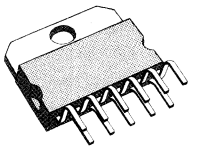
SGS-THOMSON MICROELECTRONICS

TDF1778

DUAL 2-A SOURCE DRIVER

- OUTPUT CURRENT UP TO 2.5 A
- WIDE RANGE OF SUPPLY VOLTAGES : + 8 to + 32 V
- CAN WITHSTAND OVERVOLTAGES OF AS HIGH AS 60 V BETWEEN V_{CC} AND GROUND
- INTERNAL ZENER DIODE PROVIDES FAST SWITCHING OF INDUCTIVE LOADS
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND

MULTIWATT-11



ORDER CODE : TDF1778SP

DESCRIPTION

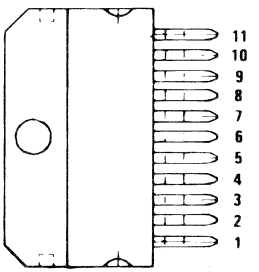
The TDF1778 is a dual source driver delivering high output currents and capable to drive any type of loads (Electrovalves, contactors, lamps).

This device is essentially blow-out proof, each output is protected against short-circuits. If internal dissipation becomes too high, drivers will shut down to prevent excessive heating. An "ALARM" output is provided to indicate the action of the thermal protection. To reactivate the power outputs, the reset input must be forced to low state.

"SENSE" information of both power outputs are ORed together and then processed internally.

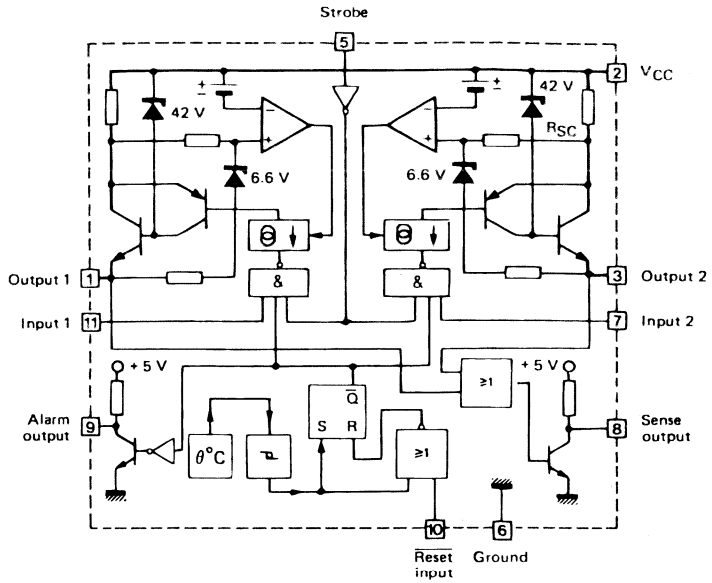
A "STROBE" input is also provided to offer the possibility of disabling the power outputs.

PIN CONNECTION



1 - Output 1
2 - VCC
3 - Output 2
4 - N.C.
5 - Strobe
6 - Ground
7 - Input 2
8 - Sense output
9 - Alarm output
10 - $\overline{\text{Reset}}$ input
11 - Input 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	35 V (60V/10 ms)	V
V_I, V_{reset}	Input Voltage (pins 7, 10 and 11)	− 30 to + 50	V
V_{strobe}	Strobe Input Voltage	− 0.5 to V_{CC}	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient Temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

THERMAL DATA

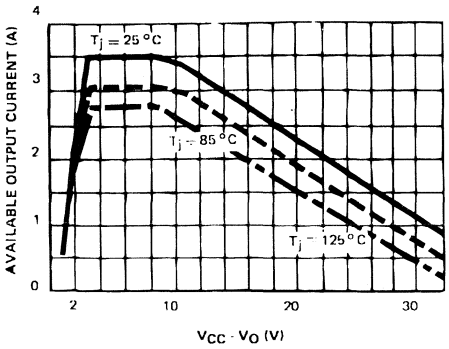
$R_{th(j-c)}$	Maximum Junction—case Thermal Resistance	3	°C/W
$R_{th(j-a)}$	Maximum Junction—ambient Thermal Resistance	40	°C/W

ELECTRICAL CHARACTERISTICS

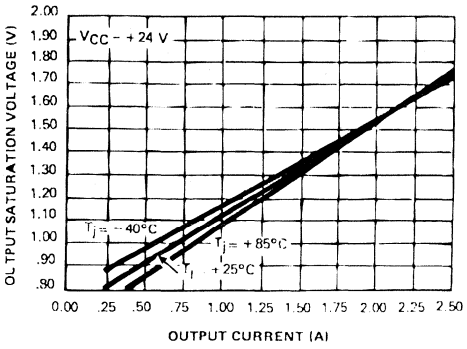
V_{CC} = + 24 V, − 40 °C < T_j < + 85 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	8	–	32	V
I_{CC}	Power Supply Current (pin 6), $I_{O1} = I_{O2}$ = 2 A	–	–	20	mA
V_{IL} V_{IH}	Logic Input Voltage (pins 7, 10, 11)	– 2	– –	0.8 –	V
V_I	Logic Input Threshold (pin 5)	–	0.8	–	V
I_{IH}	High Level Input Current (pins 7, 10, 11) V_I = + 2 V	–	20	50	µA
I_{IL}	Low Level Input Current (pins 7, 10, 11) V_I = + 0.8 V	− 5	0	+ 5	µA
V_{OH}	High Level Logic Output Voltage (pins 8, 9) I(8) = I(9) = − 30 µA	2.4	4	–	V
V_{OL}	Low Level Logic Output Voltage (pins 8, 9) I(8) = I(9) = 2 mA		–	0.4	V
$V_{CC} - V_{O1}$ $V_{CC} - V_{O2}$	Output Saturation Voltage (V(7) high, V(11) high, I_O = 2 A)	– –	1.5	1.8	V
I_{OL}	Low Level Input Current (pins 1, 3) V(7) Low, V(11) Low, V_O = 0 V	–	400	1000	µA
$V_{CC} - V_{O1}$ $V_{CC} - V_{O2}$	Switch–off Output Voltage (inductive load)	40 –	44 –	48	V
I_{O1}, I_{O2}	Available Output Current (pins 1, 3), V(7) High, V(11) High, $V_{CC} - V_O$ = 32 V, T_j = 25 °C	100	–	–	mA
I_{Oalarm}	Available "Alarm" Output Current, V(9) = + 4 V	4	8	–	mA
I_{Osense}	Available "Sense" Output Current, V(8) = + 4 V	4	8	–	mA
$I_{IHsense}$	Output Sensing High Level Input Current (pins 1, 3) V_I = + 2 V	–	1	2	mA
$V_{IHsense}$	High Level "Sense" Input Voltage (pins 1, 3)	0.8	1.9	2.5	V

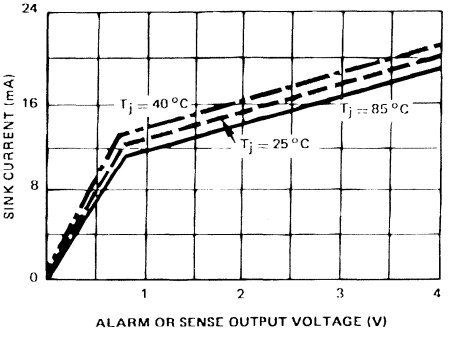
AVAILABLE OUTPUT CURRENT



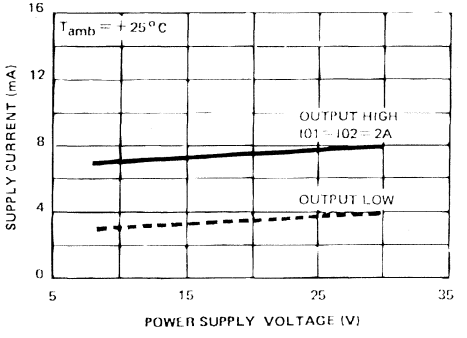
OUTPUT SATURATION VOLTAGE



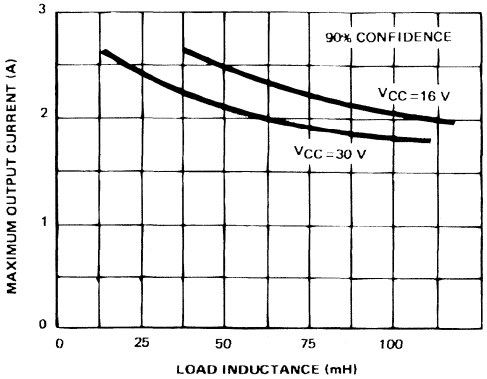
AVAILABLE ALARM OR SENSE OUTPUT CURRENTS



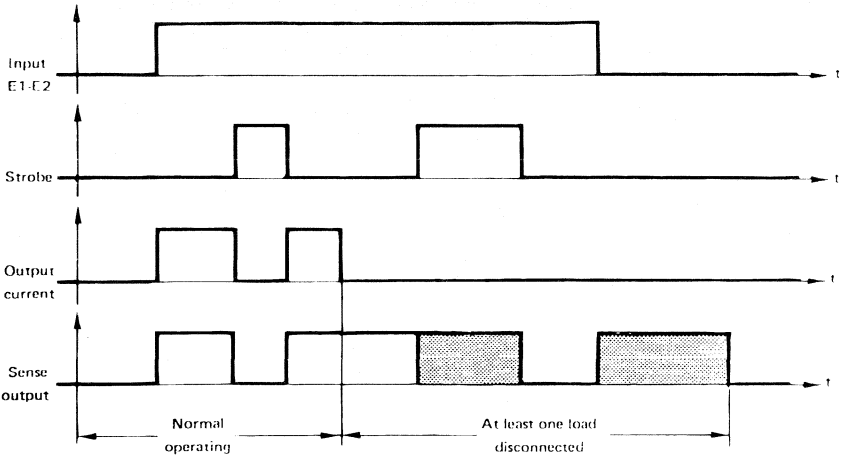
POWER SUPPLY CURRENT



MAXIMUM OUTPUT CURRENT VS LOAD INDUCTANCE



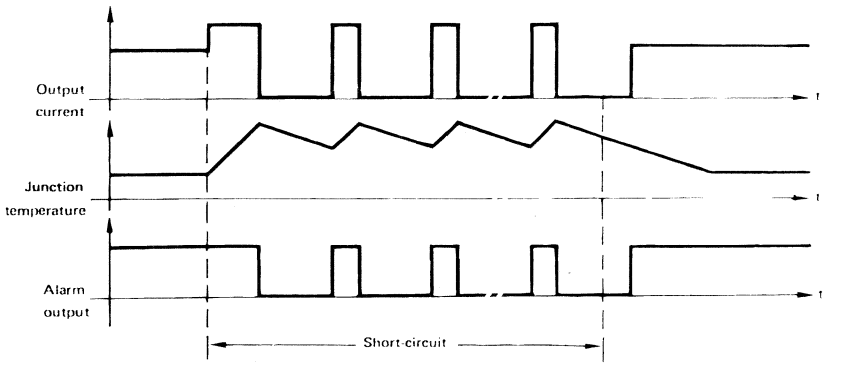
OPEN LOAD DETECTION



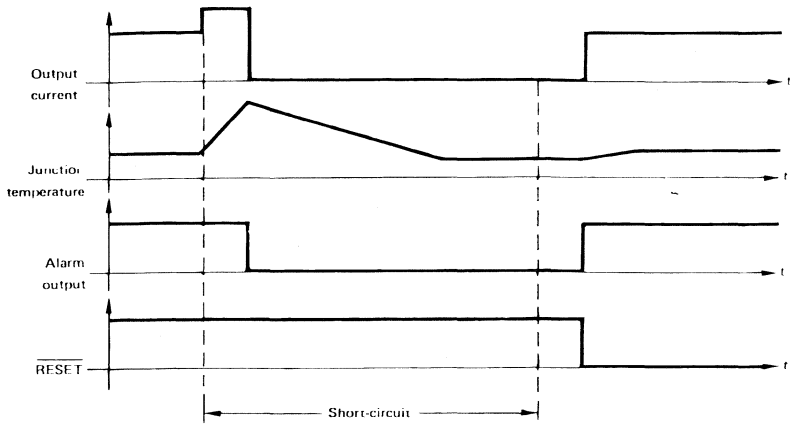
Open load detection is possible during the hachured aeras

Open load detection is possible during the hachured aeras.

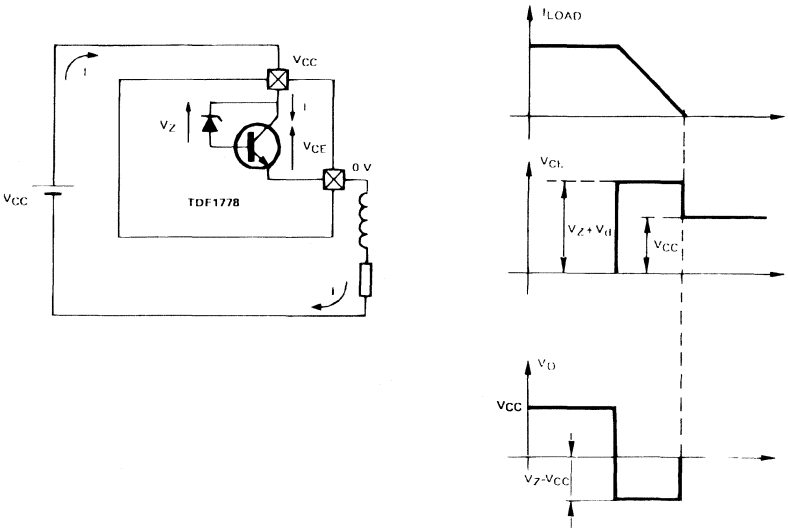
SHORT CIRCUIT CONDITIONS WAVEFORMS WITH AUTOMATIC RESET/$\overline{\text{RESET}}$ = 0



SHORT CIRCUIT WAVEFORMS WITH CONTROLLED RESET/$\overline{\text{RESET}}$ = 1

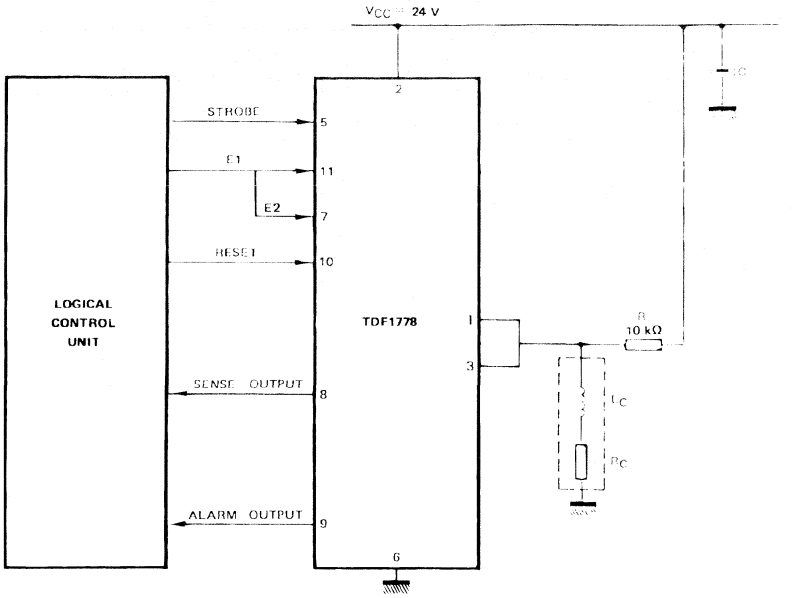


DEMAGNETIZATION UNDER INDUCTIVE LOAD



TYPICAL APPLICATION

TYPICAL APPLICATION WITH TDF1778 TWO INDUCTIVE LOADS 2 A - 24 V



Load : L_C = 80mH , R_C = 6 Ω
Rmax = V_{CC}/2 mA

Load : L_C = 80 mH, R_C = 12 Ω
R_{max} = V_{CC}/1 mA

MAIN FEATURES

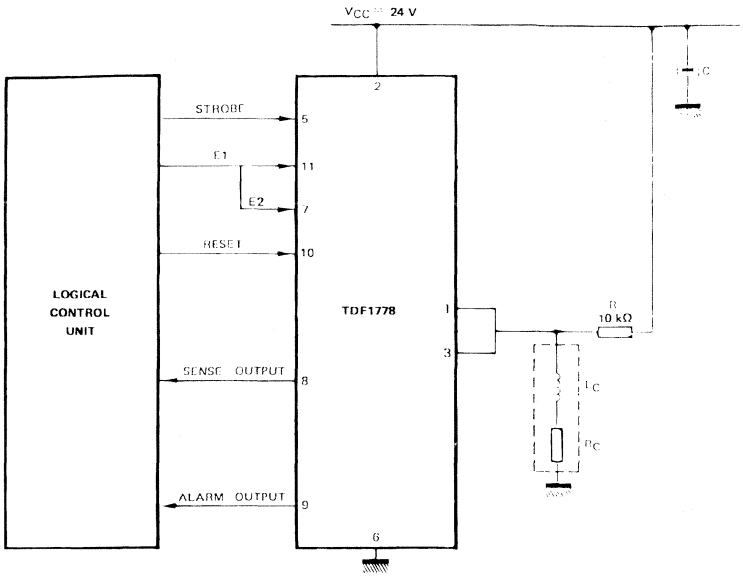
This application protected against short circuits.

The load disconnection is detected when inputs E1 and E2 are low and the sense output is high.

When thermal protection is activated the pin 9 is low.

Inputs and outputs are TTL comptable.

TDF1778 HIGH CURRENT APPLICATION WITH INDUCTIVE LOAD 24 V - 4 A



Load : L_C = 80 mH, T_C = 6 Ω
R_{max} = V_{CC}/2 mA

MAIN FEATURES

This application has the same features as the dual 2 A -12 V application.

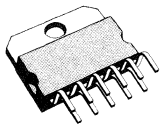
SGS-THOMSON MICROELECTRONICS

TDF1779A

DUAL 2-A SOURCE DRIVER

- OUTPUT CURRENT UP TO 2.5 A
- WIDE RANGE OF SUPPLY VOLTAGE : + 8 V TO + 26 V
- CAN WITHSTAND OVERVOLTAGES OF AS HIGH AS 60 V BETWEEN V_{CC} AND GROUND
- OUTPUT VOLTAGE CAN SWING TO LOWER THAN GROUND
- "SENSE" AND "ALARM" OUTPUTS ARE OPEN COLLECTOR OUTPUTS

MULTIWATT-11



ORDER CODE : TDE 1779ASP

DESCRIPTION

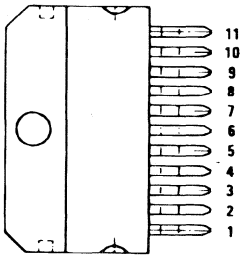
The TDF1779A is a dual source driver delivering hihg output currents and the capability to drive highly inductive loads (Electrovalves, contractors, relays...).

This device is essentially blow-out proof, each output is protected against short-circuits. If internal dissipation becomes too high, drivers will shut down to prevent excessive heating. An "ALARM" output is provided to indicate the action of the thermal protection. To reactivate the power outputs, the reset input must be forced to low state.

"SENSE" information of both power outputs are ORed together and then processed internally.

A "STROBE" input is also provided to offer the possibility of disabling the power outputs.

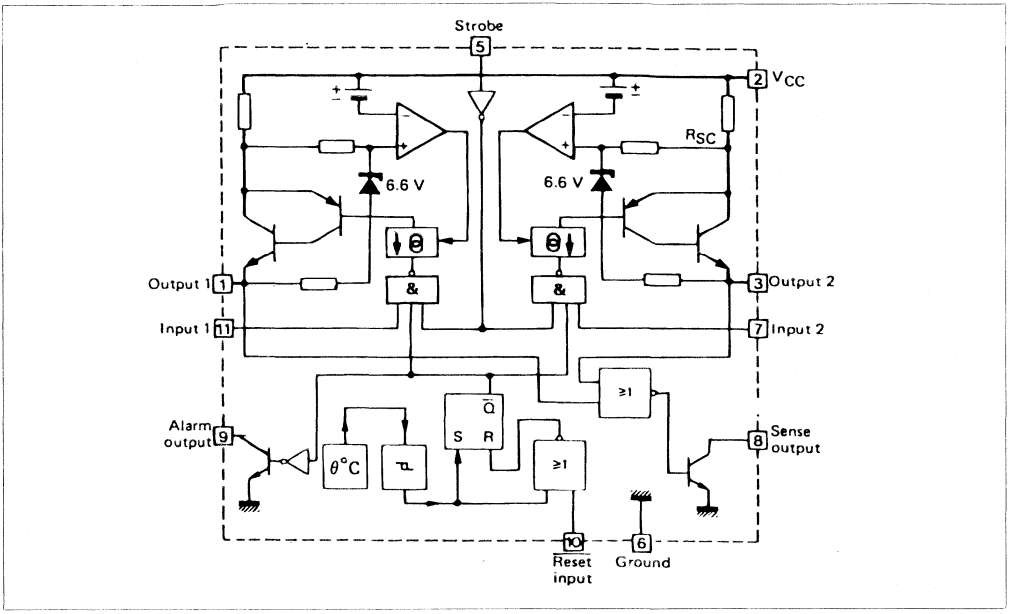
PIN CONNECTIONS



Tab is connected to pin 6

1 - Output 1
2 - V_{CC}
3 - Output 2
4 - N.C.
5 - Strobe
6 - Ground
7 - Input 2
8 - Sense output
9 - Alarm output
10 - Reset input
11 - Input 1

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	35 V (60 V/10 ms)	V
V_i, V_{reset}	Input Voltage (Pins 7, 10 and 11)	− 30 to + 50	V
V_{strobe}	Strobe Input Voltage	− 0.5 to V_{CC}	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

THERMAL CHARACTERISTICS

$R_{th\ (j-c)}$	Maximum Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j-a)}$	Maximum Junction-ambient Thermal Resistance	40	°C/W

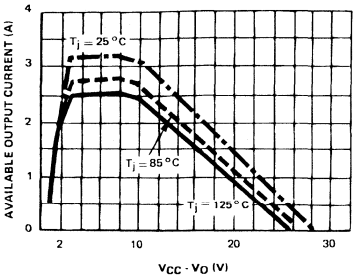
ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 24 V, − 40 °C < T_j < + 85 °C (unless otherwise specified)

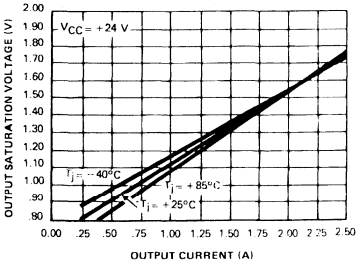
Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	8	-	26	V
I_{CC}	Power Supply Current (pin 6), IO1 =IO2, = 2A	-	-	20	mA
V_{IL} V_{IH}	Logic Input Voltage (pin 7,10,11)	- 2	- -	0.8 -	V
V_I	Logic Input Threshold (pin 5)	-	0.8	-	V
I_{IH}	High Level Input Current (pins 7,10,11) VI = + 2 V	-	20	50	µA
I_{IL}	Low Level Input Current (pins 7,10,11) VI = + 0.8 V	− 5	0	+ 5	µA
-	Off State Output Voltage (pins 8,9) I(8) = I(9) = 2 mA	-	-	0.4	V
V_{CC} − V01 V_{CC} − V02	Output Saturation Voltage (V(7) high, V(11) High, IO = 2A)	-	1.5	1.8	V
I_{OL}	Low Level Output Current pins 1,3) V(7) Low, V(11) Low, VO = 0 V	-	400	1000	µA
V_{CC} − V01 V_{CC} − V02	Switch-off Output Voltage (inductive load) Note 1	-	-	45	V
$I_{O}1$, I_{O2}	Available Ouptut Current (pins 1,3), V(7) high, V(11p) high, V_{CC} − V_O = 26 V, T_j = 25 °C	10	-	-	mA
$I_{O\ Alarme}$	Available "Alarme" Output Current, V(9) = + 4 V	4	8	-	mA
$I_{O\ Sense}$	Available "Sense Ouptut Current, V(8) = + 4 V	4	8	-	mA
$I_{IH\ Sense}$	Output Sensing high Level Input Current (pins 1,3) V_I = +2 V	-	1	2	mA

Note : 1. An external discharge circuit is required for inductive loads.

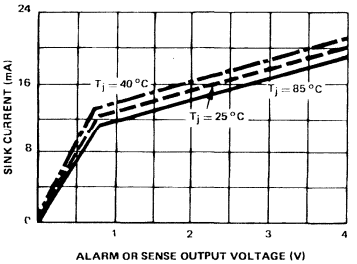
AVAILABLE OUTPUT CURRENT



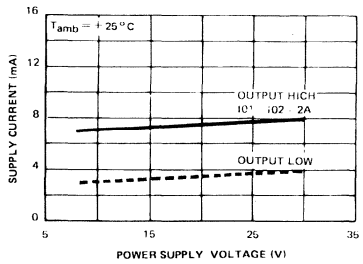
OUTPUT SATURATION VOLTAGE



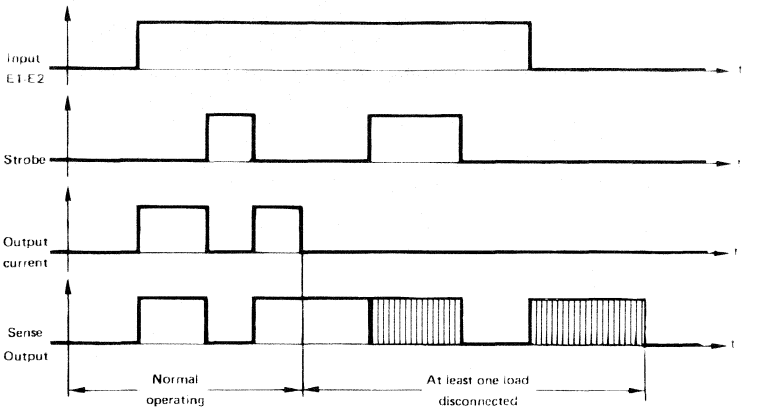
AVAILABLE ALARM OR SENSE OUTPUT CURRENTS



POWER SUPPLY CURRENT

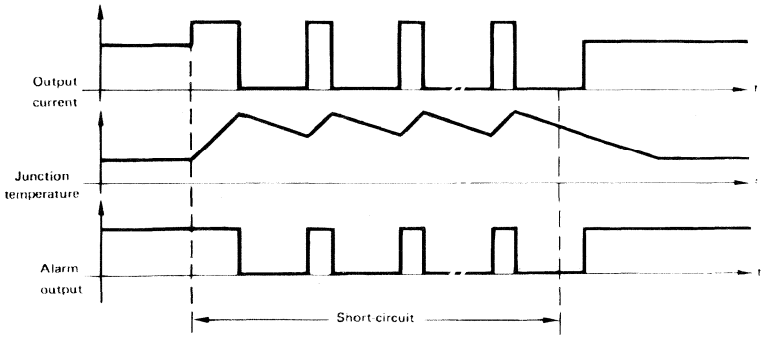


OPEN LOAD DETECTION

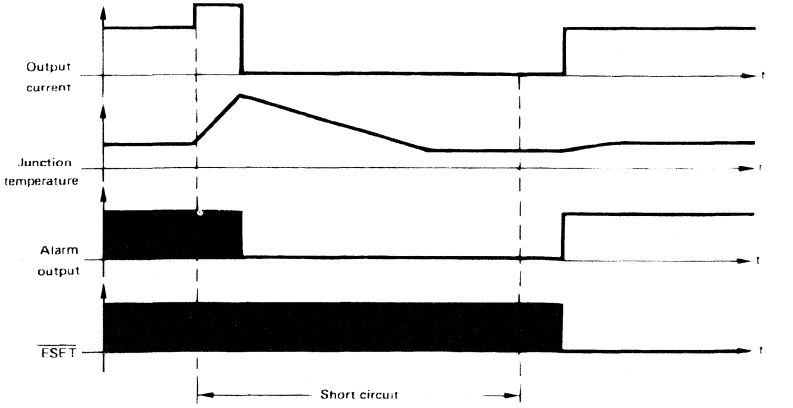


Open load detection is possible during the hachured aeras

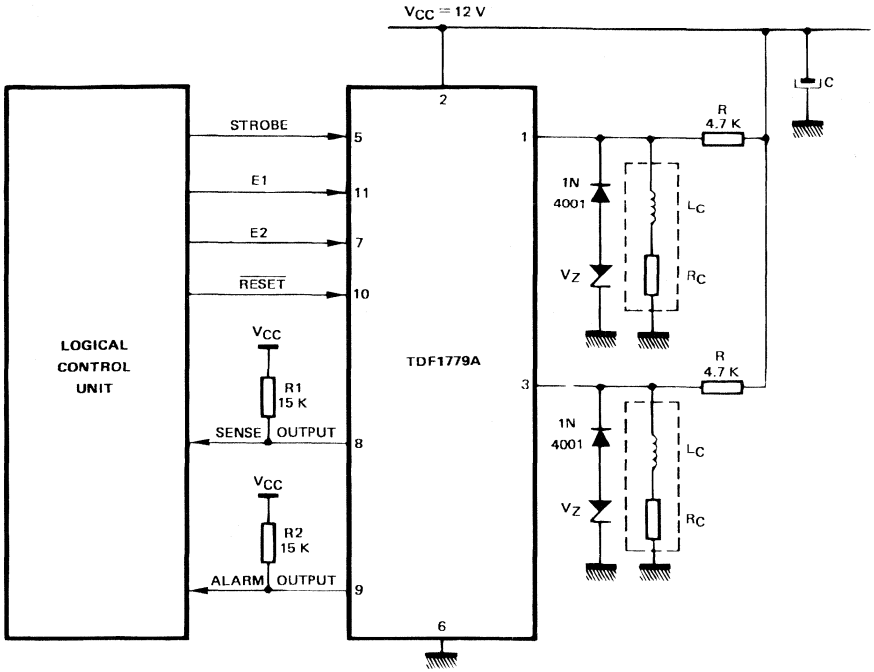
SHORT CIRCUIT CONDITIONS WAVEFORMS WITH AUTOMATIC RESET $\overline{RESET} = 0$



SHORT CIRCUIT CONDITIONS WAVEFORMS WITH CONTROLLED RESET $\overline{RESET} = 1$



TYPICAL APPLICATION WITH TDF1779A TWO LOADS 12 V - 2 A



Load : $R_C = 6\ \Omega$
The external Zener diode must dissipate the power stored in the inductance L_C.
$R_1 min = V_{CC}/4$ mA, $R_2 min = V_{CC}/4$ mA, $R max = V_{CC}/1$ mA.

MAIN FEATURES

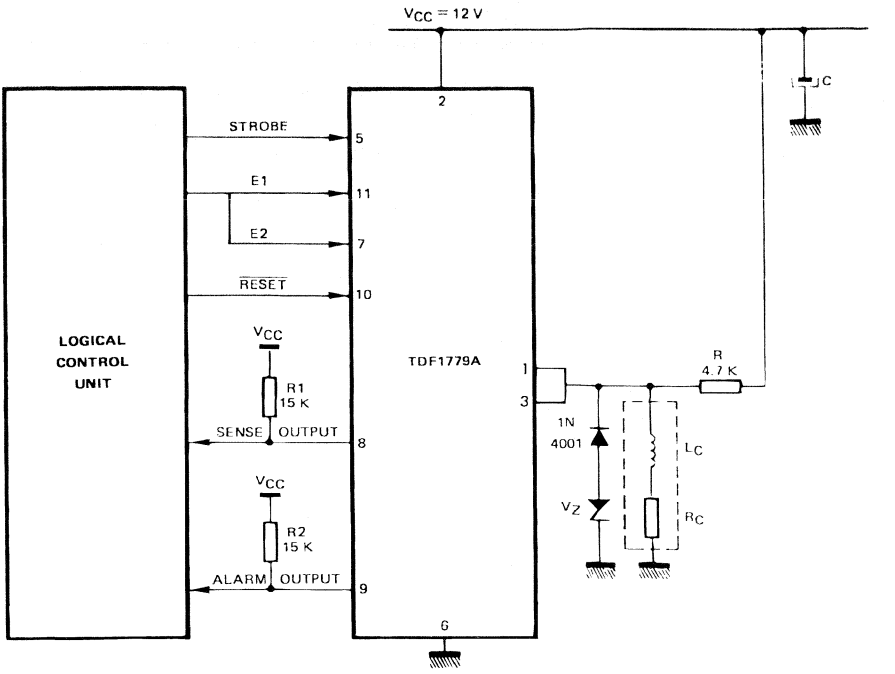
This application is protected against for short circuit and overload.

The load disconnection is detected when inputs E_1 and E_2 are low and the sense output is high.

When thermal protection is actived the pin 9 is low. Inputs are TTL compatible.

Sense output, Alarm output are open collector.

TDF1779A HIGHT CURRENT APPLICATION WITH LOAD 12 V - 4 A



Load : $R_C = 3\ \Omega$
The external Zener diode must dissipate the power stored in the inductance Lc.
$R_1min = V_{CC}/4$ mA, $R_2min = V_{CC}/4$ mA, $Rmax = V_{CC}/2$ mA.

MAIN FEATURES

This application has the same features as the dual 2 A - 12 V application.

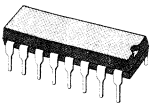
SGS-THOMSON MICROELECTRONICS

TEA3717

STEPPER MOTOR DRIVER

- HALF-STEP AND FULL-STEP MODE
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL 5 TO 1000 mA
- WIDE VOLTAGE RANGE 10 TO 45 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY

POWERDIP 12 + 2 + 2

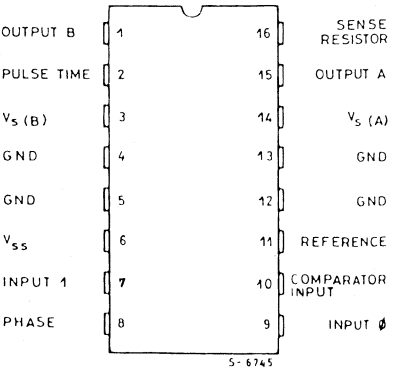


ORDER CODE : TEA3717DP

DESCRIPTION

The TEA3717 is a bipolar monolithic integrated circuit intended to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3717 and a few external components form a complete control and drive unit for LS-TTL or microprocessor-controlled stepper motor systems.

CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

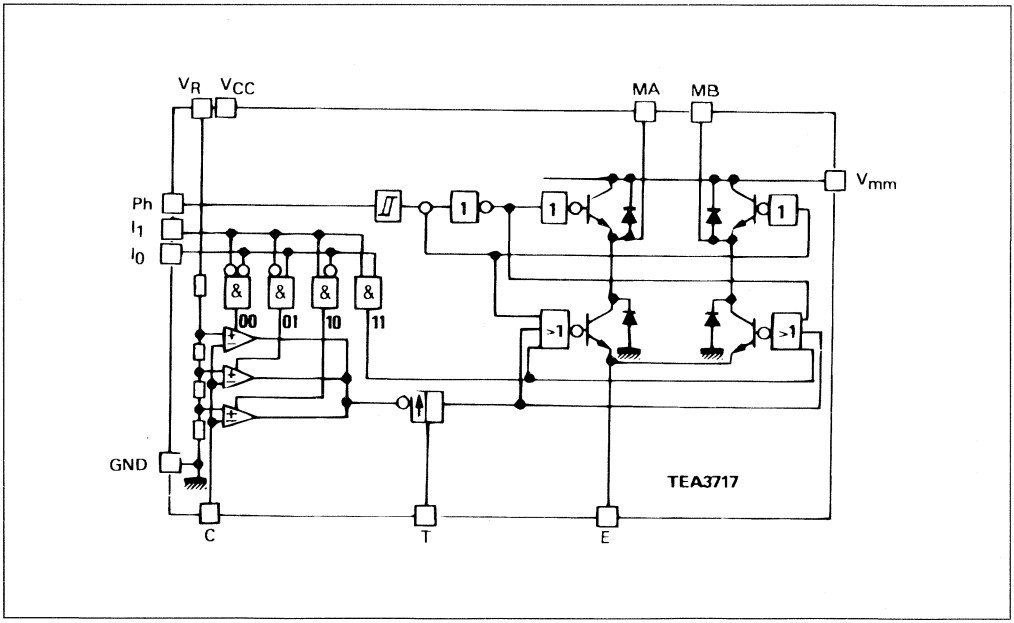
Symbol	Parameter	Value	Unit
V_{mm}	Power Supply Voltage (pins 14, 3)	45	V
V_{CC}	Logic Supply Voltage (pin 6)	7	V
	Input Voltage		V
V_{in}	Logic Inputs	− 0.5 to 6	
V_{in}	Analog Inputs	V_{CC}	
V_V	Reference Input	15	
	Input Current		mA
I_{in}	Logic Inputs	− 10	
I_{in}	Analog Inputs	− 10	
I_O	Output Current	± 1	A
T_j	Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C
T_{oper}	Operating Ambiant Temperature Range	0 to + 70	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Maximum Junction-pins Thermal Resistance	11	°C/W
$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	45*	°C/W

* Soldered on a 35 mm thick 20 cm^3 PC board copper area

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{mm}	Supply Voltage	10	–	40	V
I_o	Output Current	0.020	–	0.8	A
T_{amb}	Ambient Temperature	0	–	70	°C
t_r	Rise Time, Logic Inputs	–	–	2	µs
t_f	Fall Time, Logic Inputs	–	–	2	µs

ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V, ± 5 %, V_{mm} = + 10 V to + 40 V, T_{amb} = 0 °C to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	–	–	25	mA
V_{IH}	High Level Input Voltage - Logic Inputs	2.0	–	–	V
V_{IL}	Low Level Input Voltage - Logic Inputs	–	–	0.8	V
I_{IH}	High Level Input Current - Logic Input (V_I = + 2.4 V)	–	–	20	µA
I_{IL}	Low Level Input Current - Logic Inputs (V_I = + 0.4 V)	– 0.4	–	–	mA
V_{CH} V_{CM} V_{CL}	Comparator Threshold Voltage (V_R = + 5.0 V), I_0 = 0, I_1 = 0 I_0 = 1, I_1 = 0 I_0 = 0, I_1 = 1	390 230 65	420 250 90	440 270 90	mV
I_{CO}	Comparator Input Current	– 20	–	20	µA
I_{off}	Output Leakage Current (I_0 = 1, I_1 = 1) T_{amb} = + 25 °C T_{amb} = + 70 °C, V_S = 40 V, V_{SS} = 5 V	 – –	 – 100	 100 200	µA
V_{sat}	Total Saturation Voltage Drop (I_o = 500 mA)	–	–	4.0	V
P_{tot}	Total Power Dissipation I_o = 500 mA, f_s = 30 kHz I_o = 800 mA, f_s = 30 kHz	 – –	 1.8 3.7	 2.3 –	W
t_{off}	Cut off Time (see figure 1 and 2, V_{mm} = + 10 V, t_{on} ≥ 5 µs)	25	30	35	µs
t_d	Turn off Delay (see figure 1 and 2, T_{amb} = + 25 °C, dVC/dt ≥ 50 mV/µs)	–	1.6		µs

Figure 1 (see note).

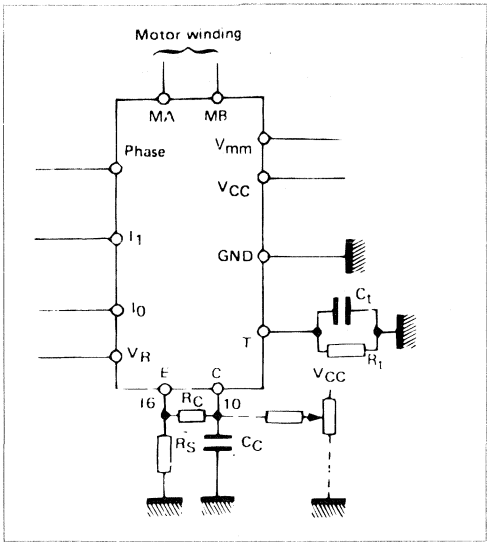
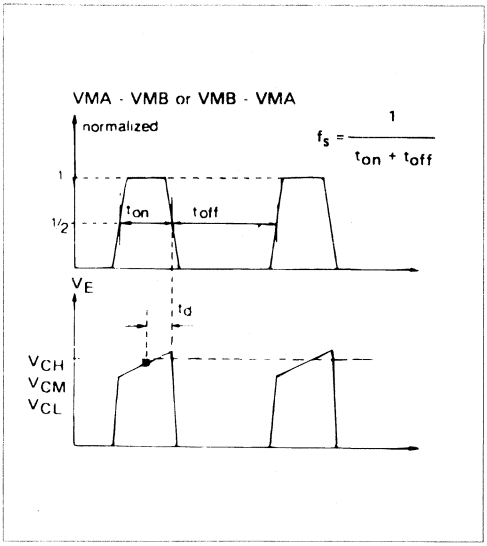


Figure 2.



FUNCTIONAL DESCRIPTION

The circuit is intented to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs I_0 and I_1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

I_0	I_1	Current Level
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	Maximum Current

PHASE – This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the PHASE-input causes the motor current flow from M_A through the winding to M_B.

Note : R_S = 1 Ω, inductance free
R_C = 1 kΩ
C_C = 820 pF, ceramic
R_t = 56 kΩ
C_t = 820 pF, ceramic

I_0 and I_1 – The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor R_S.

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1. The motor current flows through the sensing resistor R_S. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off}.

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output.

The monostable output is high during the pulse time, t_{off}, which is determined by the timing components R_t and C_t.

$$t_{off} = 0.69 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.

If a new trigger signal should occur during t_{off}, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power-supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that it is not permitted to short circuit the outputs.

V_{CC}, V_{mm}, V_R

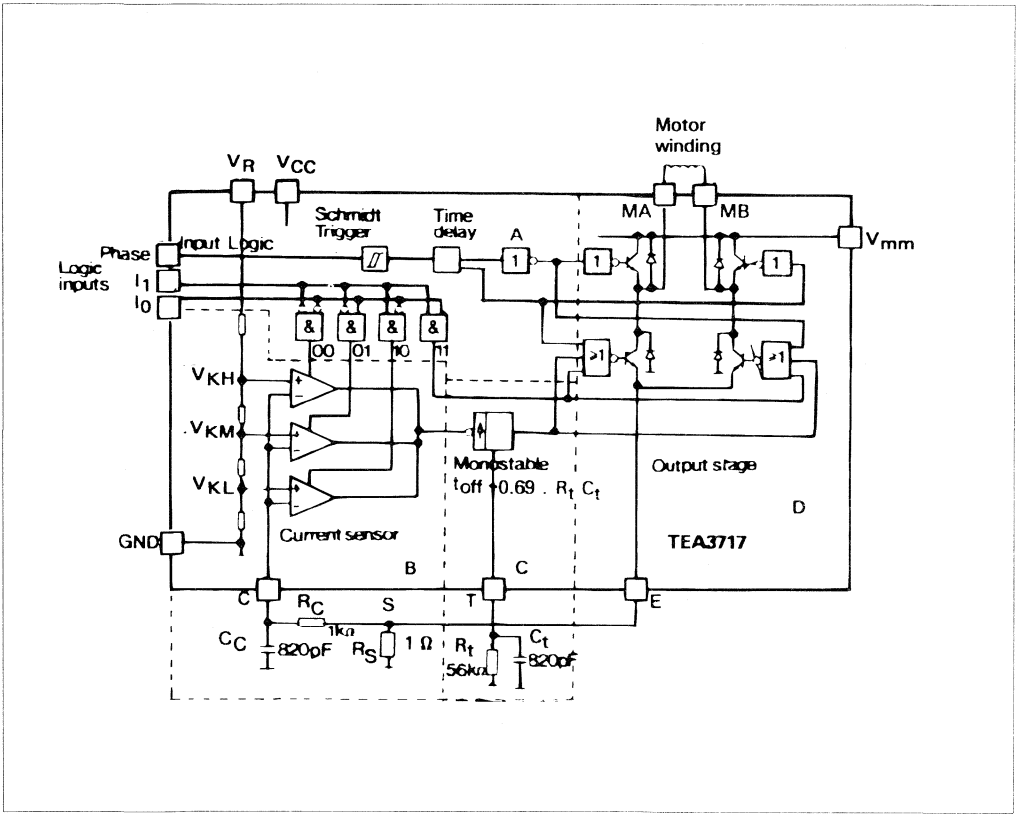
The circuit will stand any order of turn-on or turn-off of the supply voltages V_{SS} and V_S. Normal dV/dt values are then assumed.

Preferably, V_R should be tracking V_{CC} during power-on and power-off.

ANALOG CONTROL

The current levels can be varied continuously either if V_R is varied or with a circuit varying the voltage fed into the comparator terminal (see fig.1).

Figure 3.



Functional blocks

A. TTL compatible input logic
B. Current sensor
C. Single-pulse generator (monostable)
D. Output stage with protection diodes.

Figure 4 : Typical Sink Saturation Voltage vs Output Current.

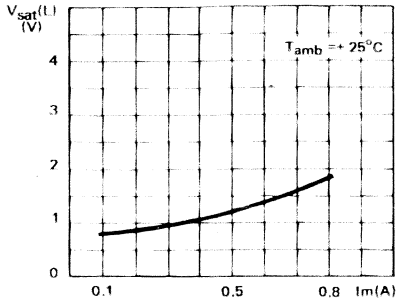


Figure 5 : Typical Source Saturation Voltage vs Output Current.

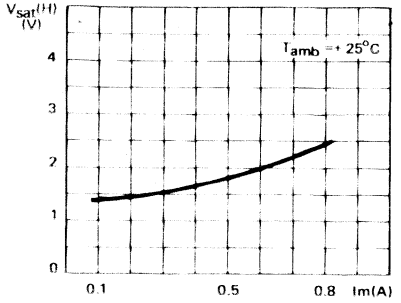
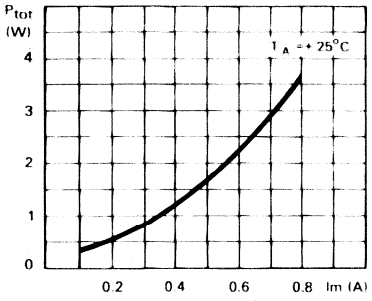


Figure 6 : Typical Power Losses vs Output Current.



TYPICAL APPLICATION

Figure 7 : Serial Printer Carriage Drive.

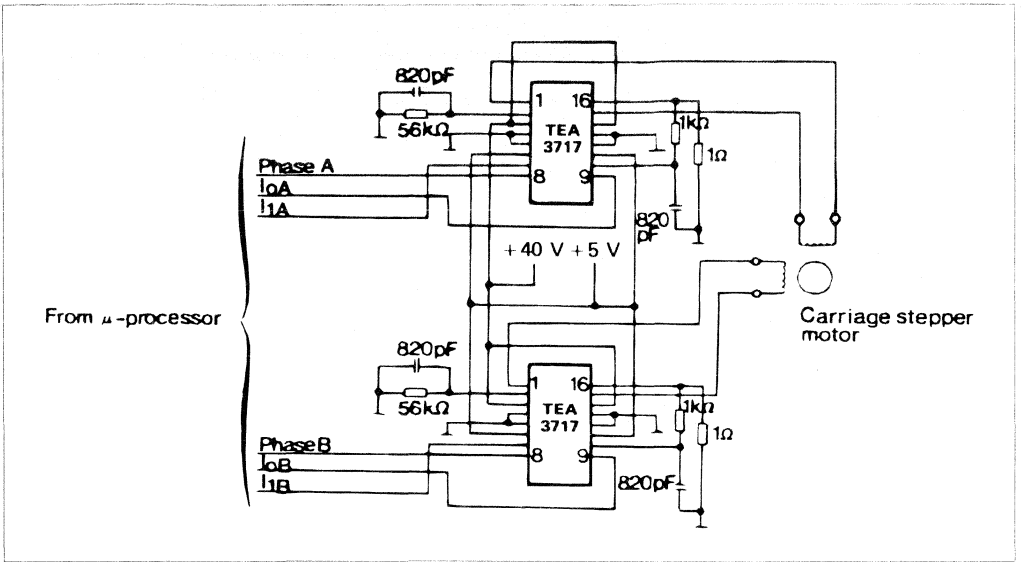
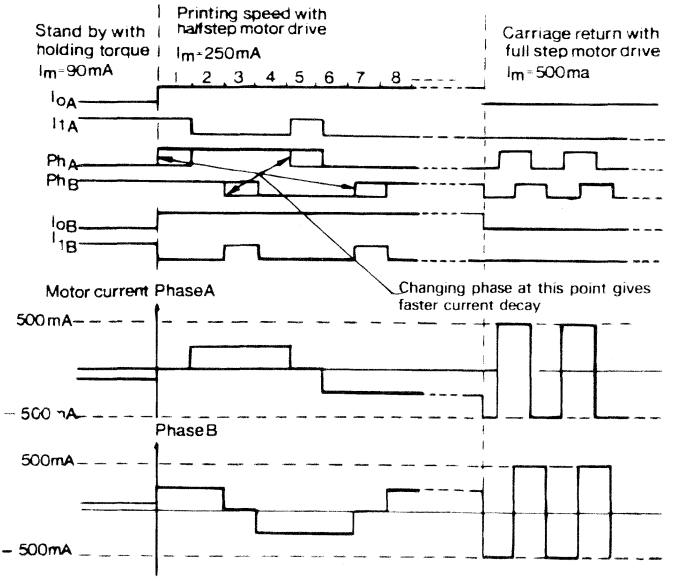


Figure 8 : Principal Operating Sequence.



SGS-THOMSON MICROELECTRONICS

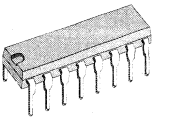
TEA3718
TEA3718S

STEPPER MOTOR DRIVER

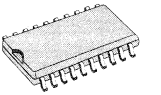
ADVANCE DATA

- HALF-STEP AND FULL-STEP MODE
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL 5 TO 1500 mA
- WIDE VOLTAGE RANGE 10 TO 50 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY
- THERMAL OVERLOAD PROTECTION
- ALARM OUTPUT OR PRE-ALARM OUTPUT (see internal table)

Powerdip
12 + 2 + 2



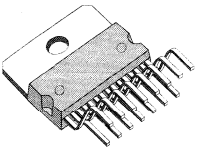
SO-20L



ORDERING NUMBERS :
TEA3718SDP
TEA3718DP

ORDERING NUMBER :
TEA3718SFP

MULTIWATT-15



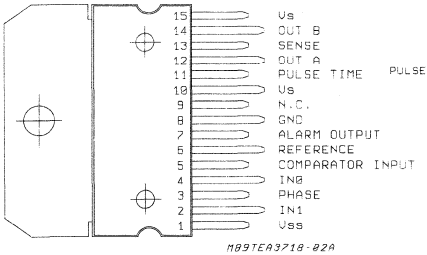
ORDERING NUMBER : TEA3718SP

DESCRIPTION

The TEA3718 and TEA3718S are bipolar monolithic integrated circuits intended to control and drive the current in one winding of a bipolar stepper motor. The circuits consist of an LS-TTL compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3718 or TEA3718S and a few external components form a complete control and drive unit for LS-TTL or microprocessor-controlled stepper motor systems.

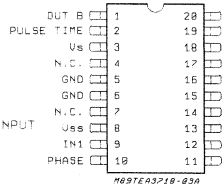
PIN CONNECTIONS (top views)

TEA3718SP
(Multiwatt-15)

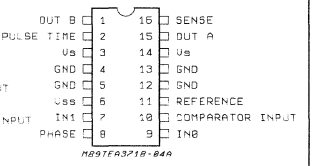


Note: HEATSINK SURFACE CONNECTED TO PIN 8

TEA3718SFP
(SO-20L)

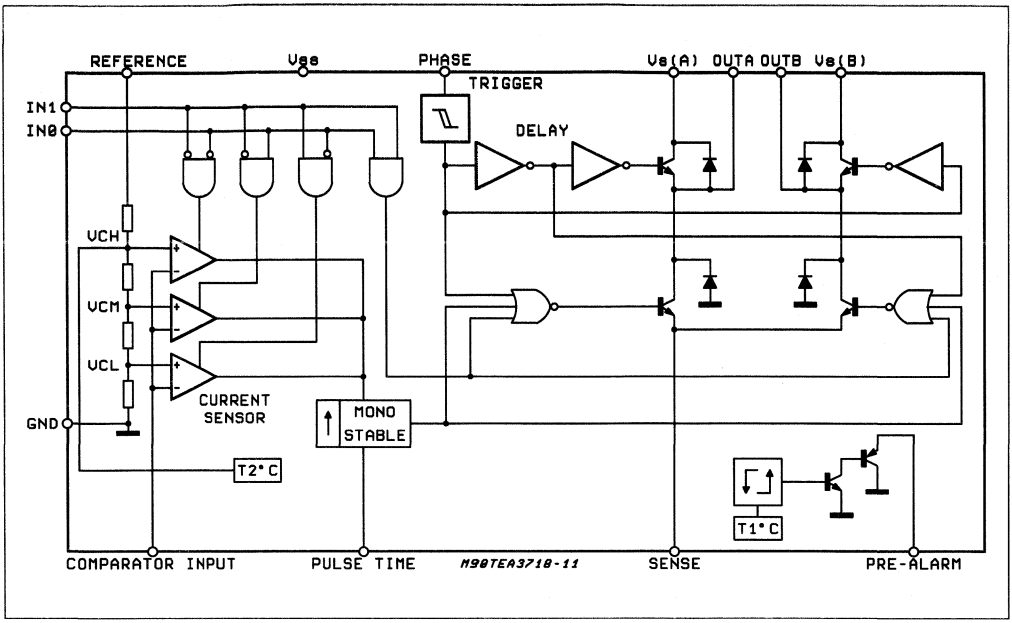


TEA3718DP
TEA3718SDP
(Powerdip 12+2+2)

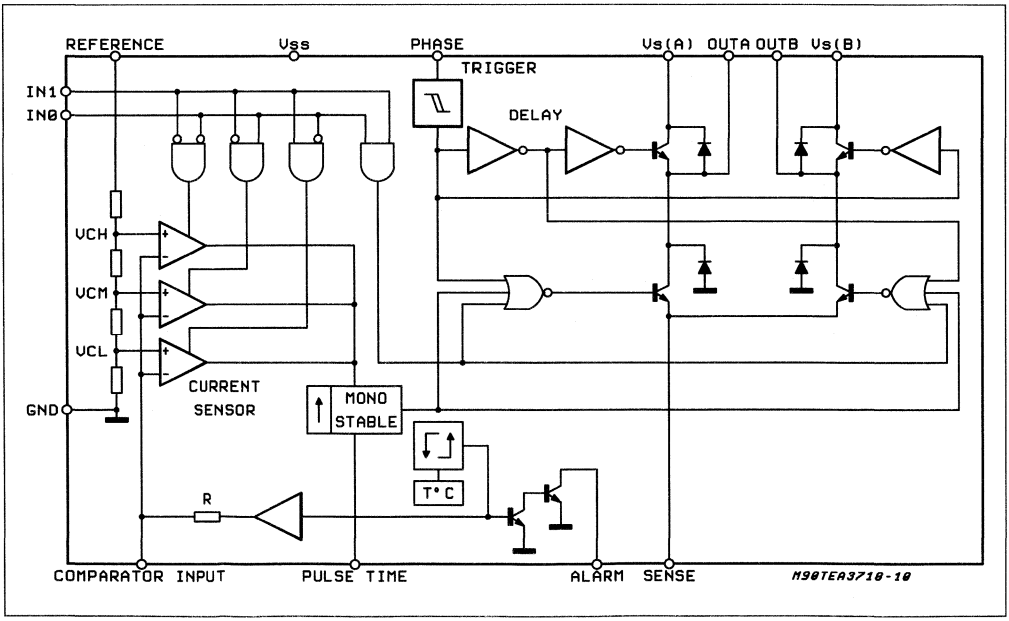


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM TEA3718S



BLOCK DIAGRAM TEA3718



PIN FUNCTIONS

Name	Function
OUT B	Output Connection (with pin OUTA). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators (t_{off} = 0.69 R_TC_T).
V_S(B)	Supply Voltage Input for Half Output Stage
GND	Ground Connection. In SO-20L and Powerdip these pins also conduct heat from die to printed circuit copper.
V_{SS}	Supply Voltage Input for Logic Circuitry
IN1	This pin and pin IN0 are logic inputs which select the outputs of three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUT A (source) to OUT B (sink). A Schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
IN0	See INPUT 1
COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter R_CC_C. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_TC_T, T_{off} = 0.69 R_TC_T.
REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators. Reference voltage with the value of R_S and the two inputs IN0 and IN1 determines the output current.
V_S(A)	Supply voltage input for half output stage
OUT A	See pin OUT B
SENSE RESISTOR	Connection to lower emitters of output stage for insertion of current sense resistor
ALARM	When T_j reaches T1°C the alarm output becomes low (TEA3718SP)
PRE-ALARM	When T_j reaches T2°C the prealarm output becomes low (T2<T1) (TEA3718SFP)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Value	Unit
V_{SS}	Supply Voltage	7	V
V_S		50	V
V_I	Input Voltage:		
	Logic Inputs	6	V
	Analog Inputs	V_{SS}	V
	Reference Input	15	V
i_i	Input Current		
	Logic Inputs	-10	mA
	Analog Inputs	-10	mA
I_O	Output Current	±1.5	A
T_J	Junction Temperature	+150	°C
T_{op}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Parameter	SO-20L	Powerdip	Multiwatt	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	16	11	3	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	60 *	45 *	40	°C/W

* Soldered on a 35 µm thick 4 cm^2 PC board copper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
v_{ss}	Supply Voltage	4.75	5	5.25	V
V_S	Supply Voltage	10	–	45	V
i_m	Output Current	0.020	–	1.2	A
T_{amb}	Ambient Temperature	0		70	°C
t_r	Rise Time Logic Inputs	–	–	2	µs
t_f	Fall Time Logic Inputs	–	–	2	µs

COMPARISON TABLE

Device	Current	Package	Alarm	Pre-Alarm
TEA3718SDP	1.5A	Powerdip 12+2+2		not connected
TEA3718SFP	1.5A	SO-20L		x
TEA3718SP	1.5A	Multiwatt-15	X	
TEA3718DP	1.5A	Powerdip 12+2+2	not connected	

MAXIMUM POWER DISSIPATION

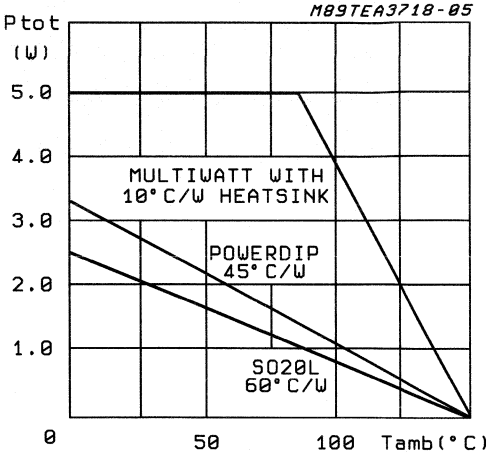


Figure 1.

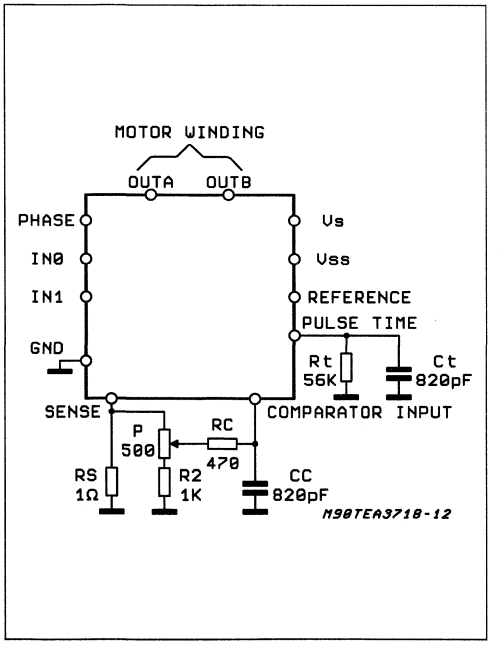
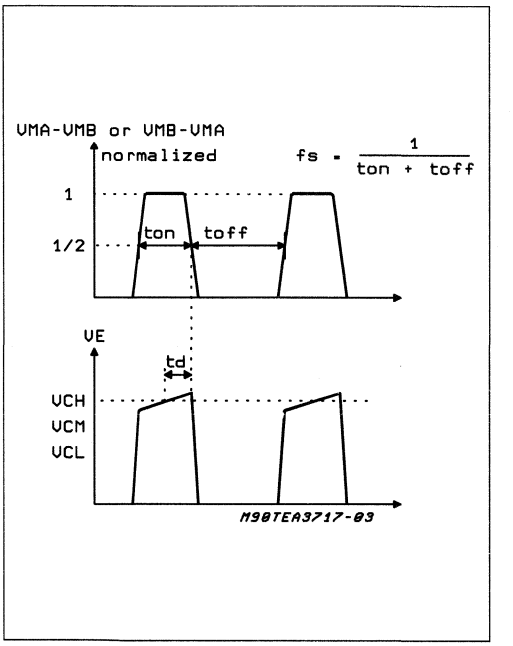


Figure 2.



R_S = 1 Ω INDUCTANCE FREE
R_C = 470 Ω
C_C = 820 pF CERAMIC
R_t = 56 kΩ
C_t = 820 pF CERAMIC
P = 500 Ω
R_2 = 1 K

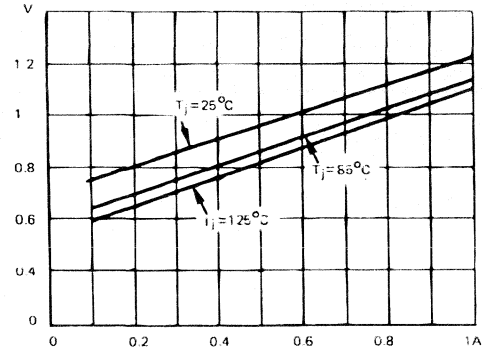
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, ± 5%, V_{mm} = 10V to 45V, T_{amb} = 0 to 70°C (T_{amb} = 25°C for TEA3718FP/SFP) unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{CC}	Supply Current		-	-	25	mA
V_{IH}	High Level Input Voltage - Logic Inputs		2	-	-	V
V_{IL}	Low Level Input Voltage - Logic Inputs		-	-	0.8	V
I_{IH}	High Level Input Current - Logic Inputs		-	-	20	µA
I_{IL}	Low Level Input Current - Logic Inputs (VI = 0.4V)		-0.4	-	-	mA
V_{CH}	Comparator Thershold Voltage (VR = 5V)	I_O = 0 I_1 = 0	390	420	440	mV
V_{CM}		I_O = 0 I_1 = 0	230	250	270	mV
V_{CL}		I_O = 0 I_1 = 1	65	80	90	mV
I_{CO}	Comparator Input Current		-20	-	20	µA
I_{off}	Output Leakage Current (I_O = 0, I_1 = 1 T_{amb} = 25°C		-	-	100	µA
V_{sat}	Total Saturation Voltage Drop (Im = 1A)	SO20/Powerdip	-	-	2.8	V
		Multiwatt	-	-	3.2	V
P_{tot}	Total Power Disssipation - I_m = 1A, f_s = 30KHz		-	3.1	3.6	W
t_{off}	Cut off Time (see figure 1 and 2, V_{mm} = 10V, V_{ton} > 5µs		25	30	35	ms
t_d	Turn off Delay (see fig. 1 and 2, T_{amb} = 25°C, dVC/dt>50mV/µs)		-	1.6	-	µs
V_{sat}	Alarm Output Saturation Voltage - I_O = 2mA (Multiwatt)		-	0.8	-	V
I_{ref}	Reference Input Current, V_R = 5V		-	0.4	1	mA
V_{sat}	Source Diode Transistor Pair Saturation Voltage	Powerdip I_m = 0.5A	-	1.05	1.2 (1.3)	V
		Powerdip I_m = 1A	-	1.35	1.5 (1.7)	V
		Multiwatt I_m = 0.5A	-	-	1.3	V
		Multiwatt I_m = 1A	-	-	1.7	V
V_f	Diode Forward Voltage	I_f = 0.5A	-	1.1	1.5 (1.6)	V
		I_f = 1A	-	1.25	1.7 (1.9)	V
I_{sub}	Substrate Leakage Current	I_f = 1A	-	-	5	mA
V_{sat}	Sink Diode Transistor Pair Saturation Voltage	Powerdip I_m = 0.5A	-	1	1.2 (1.3)	V
		Powerdip I_m = 1A	-	1.2	1.3 (1.5)	V
		Multiwatt I_m = 0.5A	-	-	1.3	V
		Multiwatt I_m = 1A	-	-	1.5	V
V_f	Diode Forward Voltage	I_f = 0.5A	-	1	1.4 (1.6)	V
		I_f = 1A	-	1.1	1.5 (1.9)	V

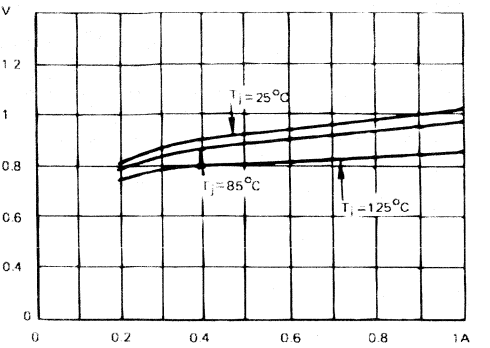
Notes:

(...) Only for TEA3718SFP mounted in SO-20L package.

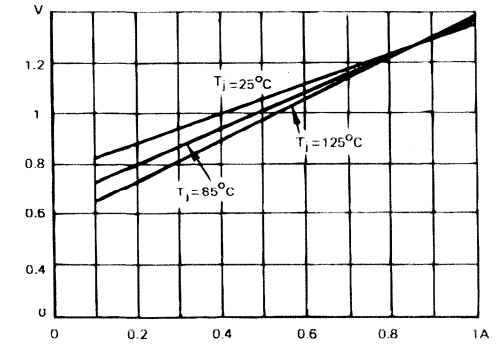
SINK DRIVER $V_{CE\ sat}$ VS I_{OUT} and T_j



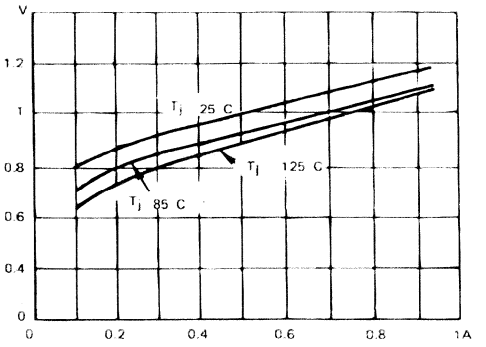
LOWER DIODE V_F VS I_{OUT} and T_J



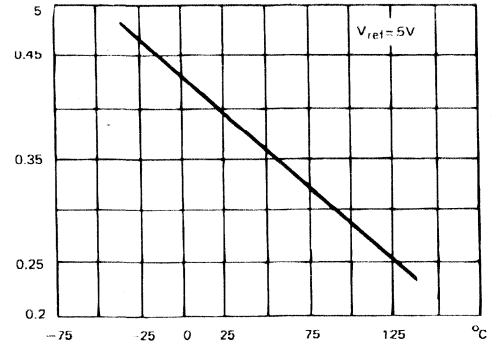
SOURCE DRIVER $V_{CE\ sat}$ VS I_{OUT} and T_j



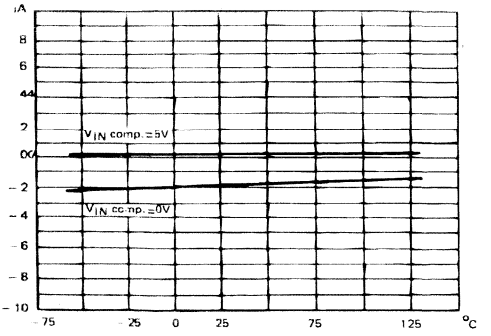
UPPER DIODE V_F VS I_{OUT} and T_j



I_{ref} VS JUNCTION TEMPERATURE



COMPARATOR INPUT CURRENT VS T_j and V_C



FUNCTIONAL BLOCKS

Figure A: ALARM OUTPUT (TEA3718SP - TEA3718DP)

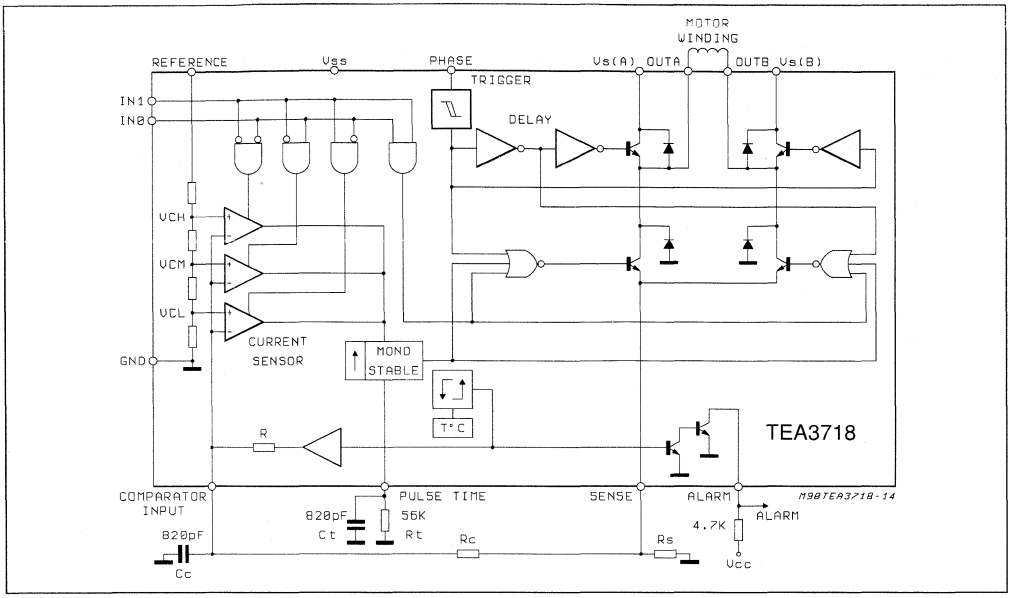
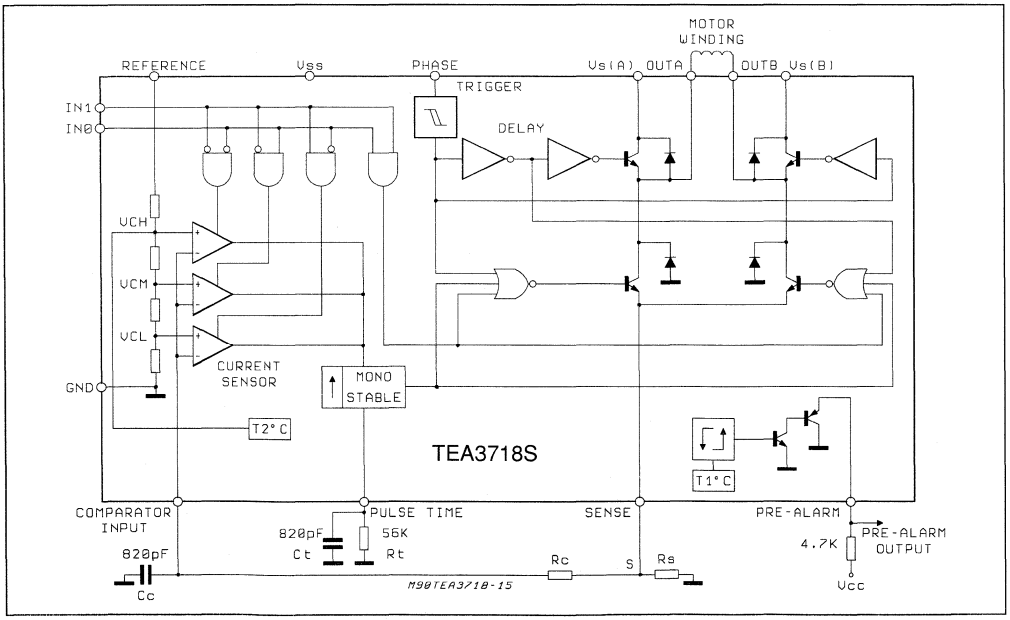


Figure B: PRE-ALARM OUTPUT (TEA3718SDP - TEA3718SFP)



ALARM OUTPUTS (TEA3718SP - TEA3718DP)
The alarm output becomes low when the junction temperature reaches T°C.
When an alarm condition occours, parts of the supply voltage (dividing bridge R - R_C) is fed to the comparator input pin (Fig. A)
Depending of the R_CC value the behaviour of the circuit is different on alarm condition:

1) $R_C > 80\Omega \Rightarrow$ the output stage is switched off

2) $R_C > 60\Omega \Rightarrow$ the current in the motor windings is reduced according to the approximate formula: (see also fig. E and F)

$$I_m = \frac{V_{TH}}{R_S} - \frac{V_{CC}}{R + R_C} \cdot \frac{R_C}{R_S}$$

with V_{TH} = Threshold of the comparator (V_{CH}, V_{CM}, V_{CL}) R = 700Ω (typical)

For several Multiwatt packages a common detection can be obtained as in Fig. D

PRE-ALARM OUTPUT
When the junction temperature reaches T1°C (typ. = 170°C) a prealarm signal is generated.

Soft thermal protection occours when function temperature reaches T2 (T2 > T1)

Figure C: Alarm Detection for Powerdip Package

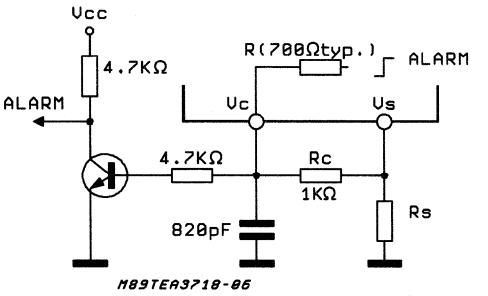


Figure D: CommonDetection for Several Multiwatt Package

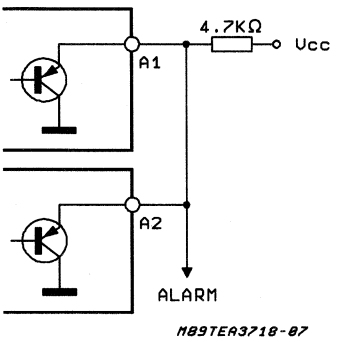


Figure E: (typical curve) Current Reduction in the Motor on Alarm Condition.

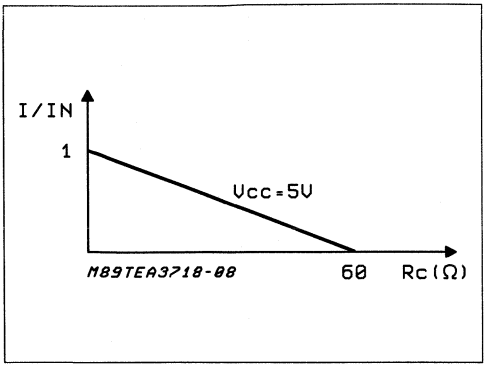
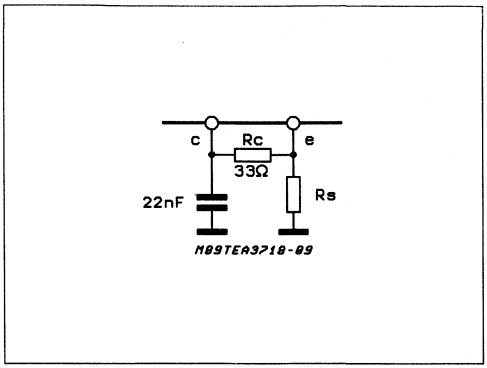
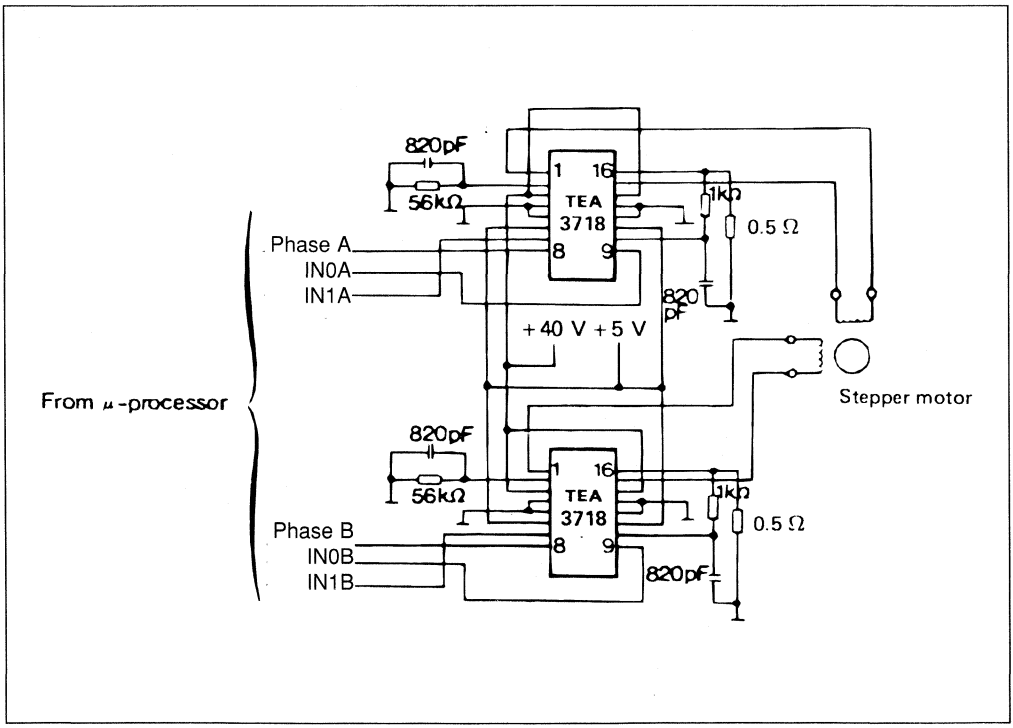


Figure F: (V_{ref} 5V) Block Diagram for Half Current on Alarm Condition.



Notes: 1. Resistance values given here are for the V_{ch} threshold. They should be adjusted using other comparators threshold or other V_{ref} value.

TYPICAL APPLICATION



FUNCTIONAL DESCRIPTION

The circuit is intended to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs IN0 and IN1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

IN0	IN1	Current Level
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	Maximum Current

PHASE - This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the PHASE input causes the motor current flow from Out A through the winding to Out B.

I_{H0} and I_{H1} - The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor R_S.

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals IN0 and IN1. The motor current flows through the sensing resistor R_S. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off}.

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off}, which is determined by the timing components R_t and C_t.

$$t_{off} = 0.69 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.

If a new trigger signal should occur during t_{off}, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that it is not permitted to short circuit the outputs.

V_{SS}, V_S, V_R

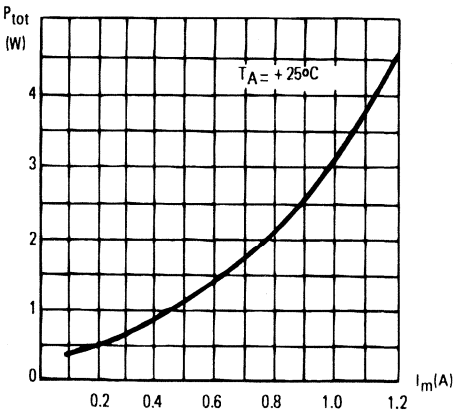
The circuit will stand any order of turn-on or turn-off the supply voltages V_{SS} and V_S. Normal dV/dt values are then assumed.

Preferably, V_R should be tracking V_{SS} during power-on and power-off if V_S is established.

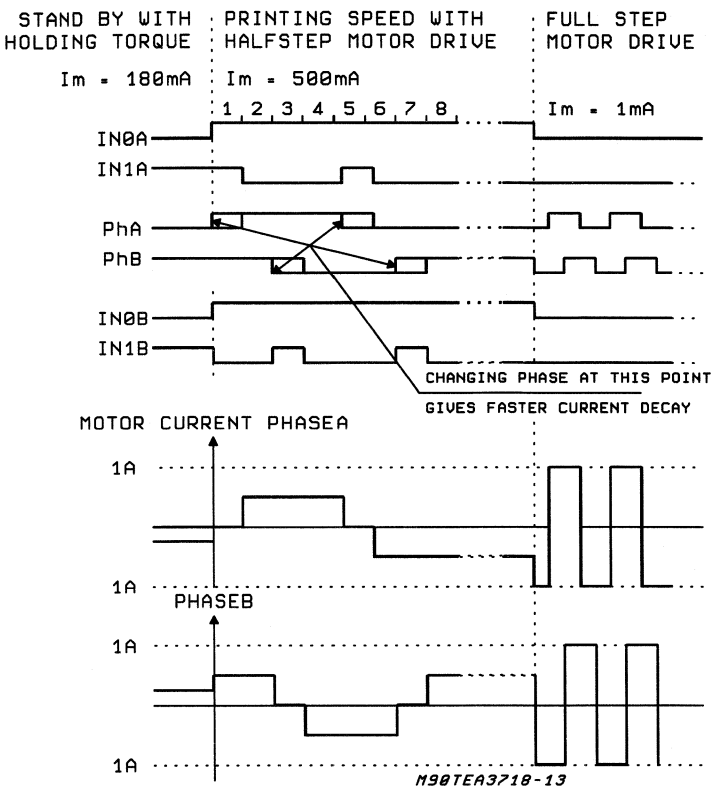
ANALOG CONTROL

The current levels can be varied continuously if V_R is varied with a circuit varying the voltage on the comparator terminal.

POWER LOSSES V_S OUTPUT CURRENT



PRINCIPAL OPERATING SEQUENCE



APPLICATION NOTES

MOTOR SELECTION

Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.

Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

UNUSED INPUTS

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

INTERFERENCE

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 15 nF ceramic capacitor, located near the package between power line V_S and ground.

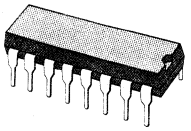
The ground lead between R_S, C_C and circuit GND should be kept as short as possible. This applies also to the lead between the sensing resistor R_S and point S, see FUNCTIONAL BLOCKS.

SGS-THOMSON MICROELECTRONICS

TEF3718
TEF3718S

STEPPER MOTOR DRIVER

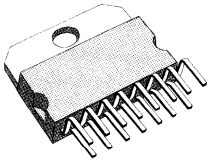
- HALF AND FULL-STEP MODES
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL : 5 TO 1500 mA
- WIDE VOLTAGE RANGE : 10 TO 50 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY
- THERMAL OVERLOAD PROTECTION
- ALARM OUTPUT (TEF3718SP) OR PREA-LARM OUTPUT (TEF3718SSP)



POWERDIP 12 + 2 + 2

ORDER CODE :

TEF3718DP TEF3718SDP



MULTIWATT 15

ORDER CODE :

TEF3718SP TEF3718SSP

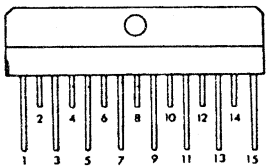
DESCRIPTION

The TEF3718 and TEF3718S are bipolar monolithic integrated circuits intended to control and drive the current in one widing of a bipolar stepper motor. The circuits consists of an LS-TLL - compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEF3718 or TEF3718S and a few external components form a complete control and drive unit for LS-TTL or microprocessor controlled stepper motor systems.

PIN CONNECTON

TEF3718

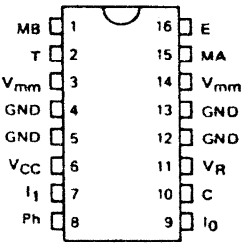
1 - V_{CC}
2 - I_1
3 - Ph
4 - I_O
5 - C
6 - V_{ref}
7 - ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB
15 - V_{mm}



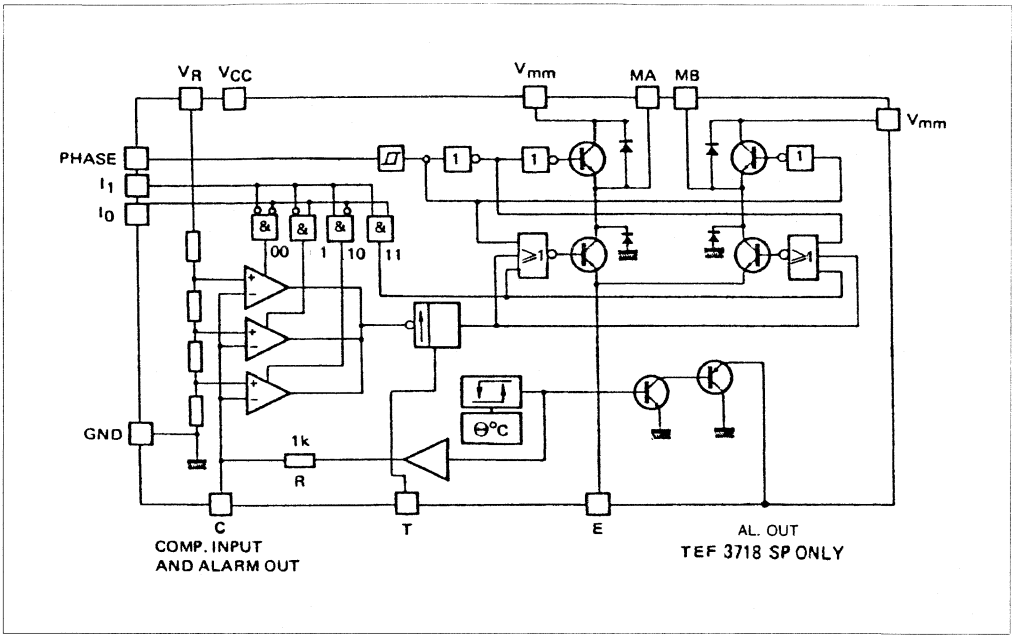
TEF3718S

1 - V_{CC}
2 - I_1
3 - Ph
4 - I_O
5 - C
6 - V_{ref}
7 - PRE-ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB
15 - V_{mm}

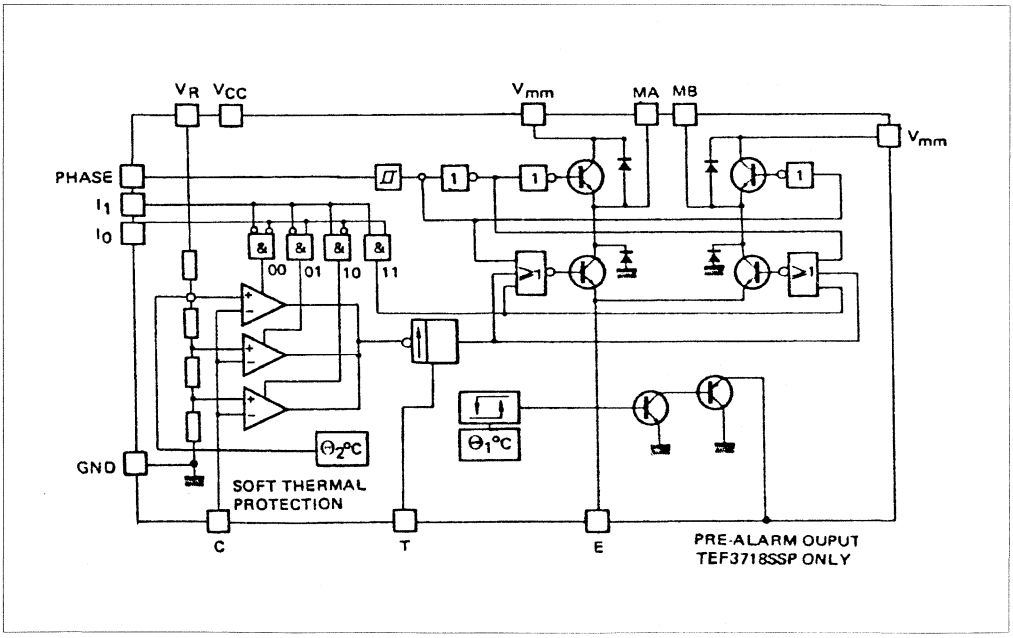
TEF3718
TEF3718S



BLOCK DIAGRAM (TEF3718)



BLOCK DIAGRAM (TEF3718S)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC} V_{MM}	Supply Voltage	7 50	V
V_i	Input Voltage : Logic Inputs Analog Inputs Reference Input	 6 V_{CC} 15	V
I_I	Input Current : Logic Inputs Analog Inputs	 10 10	mA
I_O	Output Current	± 1.5	A
T_j	Junction Temperature	+ 150	C
T_{oper}	Operating Ambient Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	POWERDIP MULTIW	11 3	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	POWERDIP MULTIW	45 (*) 40	°C/W

(*) Soldered on a 35 µm thick 20 cm^2 PC board cooper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC} V_{MM}	Supply Voltage	4.75 10	5 –	5.25 45	V
I_m	Output Current	0.020	–	1.2	A
T_{amb}	Ambient Temperature	– 40	–	85	°C
t_r	Rise Time Logic Inputs	–	–	2	µs
t_f	Fall Time Logic Inputs	–	–	2	µs

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V ± 5 %. V_{MM} = − 10 V to + 45 V. T_{amb} = − 40 C to + 85 °C (Unless otherwise specified)

Symbol	Characteristics			Min.	Typ.	Max.	Unit
I_{CC}	Supply Current					25	mA
V_{IH}	High Level Input Voltage Logic Input			2			V
V_{IL}	Low Level Input Voltage Input					0.7	V
I_{IH}	High Level Input Current Logic Input (V_I = 2.4 V)					20	µA
I_{IL}	Low Level Input Current Logic Input (V_I = 0.4 V)			0.4			µA
V_{CH} V_{CM} V_{CL}	Comparator Treshold Voltage (V_R = + 5 V)		I_O = 0 I_1 = 0 I_O = 1 I_1 = 0 I_O = 0 I_1 = 1	390 230 65	420 250 80	440 270 90	mV
I_{CO}	Comparator Input Current			- 20		20	µA
I_{off}	Output Leakage Current (I_O 1, I1 = 1)					100	µA
V_{sat}	Total Saturation Voltage Drop (I_m = 1 A,)		POWERDIP MULTIWATT			2.9 3.3	V
P_{tot}	Total Power Dissipation (I_m = 1 A, f_s = 30 kHz)				3.1	3.6	W
t_{off}	Cutt off Time (see figures 1 and 2 V_{mm} = + 10 V, $V_{ton} \leq$ 5 µs)			25	30	35	µs
t_d	Turn off Delay (see figures 1 and 2, T_{amb} =+ 25 °C dVC/dt ≤ 50 mV/µs)				1.6		µs
V_{sat}	Alarm Output Saturation Voltage I_O = 2 mA				0.8		V
I_{ref}	Reference Input Current, V_R = 5 V				0.4	1	mA
V_{sat}	Source Diode Transistor Pair	MULTIWATT	I_m = 0.5 A I_m = 1 A			1.35 1.75	mA
	Saturation Voltage	POWERDIP	I_m = 0.5 A I_m = 1 A			1.25 1.55	
V_f	Diode Forward Voltage		I_f = 0.5 A I_f = 1 A			1.5 1.7	
I_{sub}	Substrate Leakage Current		I_f = 1 A			10	
	Sink Diode Transistor Pair	MULTIWATT	I_m = 0.5 A I_m = 1 A			1.35 1.55	
V_{sat}	Saturation Voltage	POWERDIP	I_m = 0.5 A I_m = 1 A			1.25 1.35	
V_f	Diode Forward Voltage		I_f = 0.5 A I_f = 1 A			1.5 1.8	

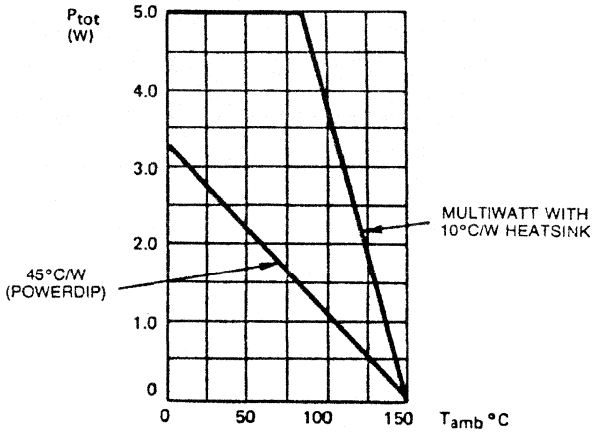
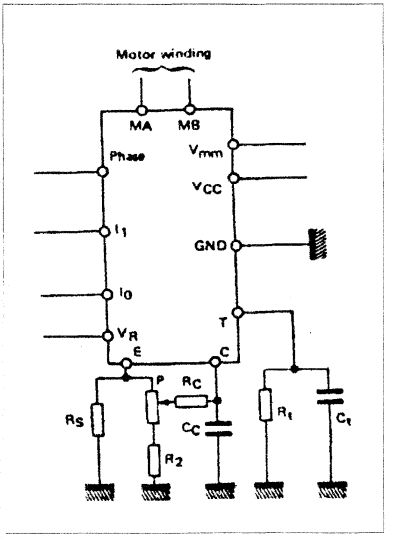
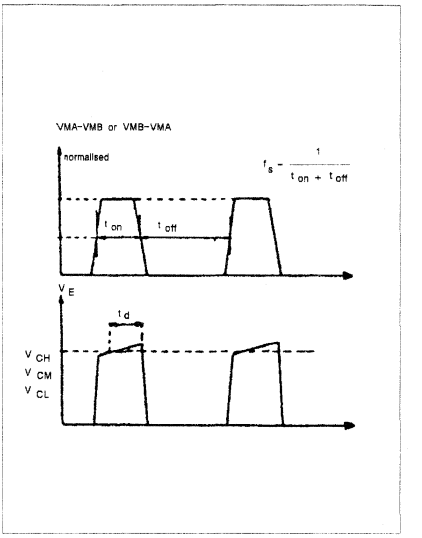


Figure 1.



R_S = 1 Ω inductance free
R_C = 470 Ω
C_C = 820 pF ceramic
R_t = 56 kΩ
C_t = 820 pF ceramic
P = 500 Ω
R_2 = 1 K

Figure 2.



SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE ... 3 V TO 18 V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

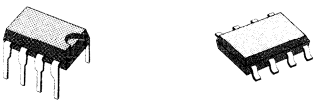
DESCRIPTION

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

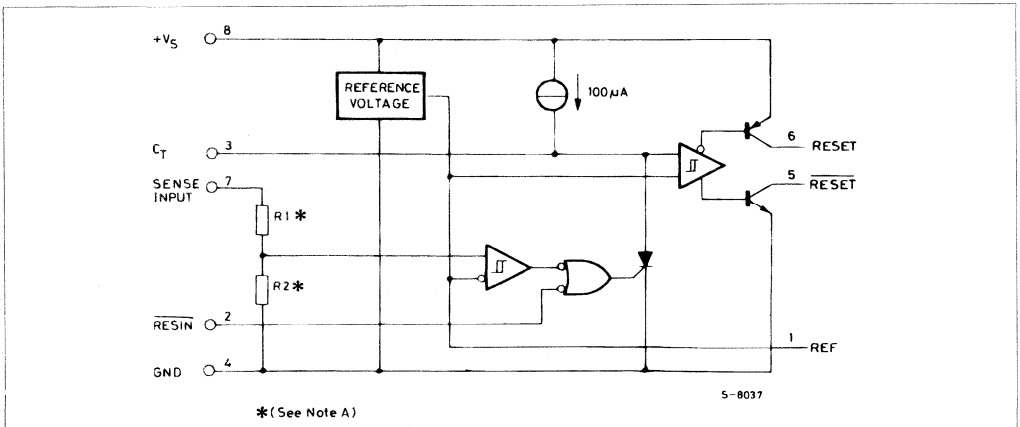
Where : C_T is in farads (F) and t_d in seconds (s). In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 µF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from – 25°C to 85°C ; the TL7700AC series is characterized from 0°C to 70°C.



Plastic Minidip SO-8 J

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open ; TL7705A R1 = 7.8 KΩ, R2 = 10 KΩ ; TL7709A R1 = 19.7 KΩ, R2 = 10 KΩ ; TL7712A R1 = 32.7 KΩ, R2 = 10 KΩ ; TL7715A R1 = 43.4 KΩ, R2 = 10 KΩ.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage, V_{CC} (see note 1)	20	V
V_i	Input Voltage Range at $\overline{RESIN}$	– 0.3 to 20	V
V_i	Input Voltage at SENSE : TL7702A (see note 2)	– 0.3 to 6	V
	TL7705A	– 0.3 to 10	V
	TL7709A	– 0.3 to 15	V
	TL7712A	– 0.3 to 20	V
	TL7715A	– 0.3 to 20	V
I_{OH}	High-level Output Current at RESET	– 30	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$	30	mA
T_{amb}	Operating Free-air Temperature Range : TL77XXAI	– 25 to 85	°C
	TL77XXAC	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

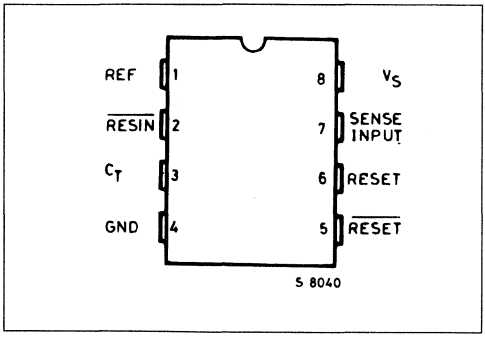
Notes : 1. All voltage values are with respect to the network ground terminal.
2. For the TL7700A, the voltage applied to the SENSE terminal must never exceed V_S.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_S	Supply Voltage		3.6	18	V
V_{IH}	High-level Input Voltage at RESIN		2		V
V_{IL}	Low-level Input Voltage at RESIN			0.6	V
V_i	Voltage at Sense Input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level Output Current at RESET			– 16	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$			16	mA
T_{amb}	Operating Free-air Temperature Range	TL77 - AI	– 25	85	°C
		TL77 - AC	0	70	

Note : 3. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_S – 1 V or 6 V, whichever is less.

CONNECTION DIAGRAM AND ORDER CODE



Temperature Range	Plastic Minidip	SO-8
Commercial 0 to 70 °C	TL77XXACP	TL77XXACD
Industrial – 25 to 85 °C	TL77XXAIP	TL77XXAID

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	120	°C/W

ELECTRICAL CHARACTERISTICS these specifications unless otherwise specified, apply for : T_{amb} = – 25 to 85 °C (TLXXAI) ; T_{amb} = 0 to 70 °C (TL77XXAC)

Symbol	Parameter		Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level Output Voltage at RESET		I_{OH} = – 16 mA	V_S–1.5			V
V_{OL}	Low-Level Output Voltage at $\overline{RESET}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference Voltage		T_{amb} = 25 °C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input Current at $\overline{RESIN}$ Input		V_i = 2.4 V to V_S			20	µA
			V_I = 0.4 V			– 100	
I_I	Input Current at SENSE Input	TL7702A	$V_{ref} < V_i < V_S$ –1.5 V		0.5	2	
I_{OH}	High-level Output Current at $\overline{RESET}$		V_O = 18 V			50	
I_{OL}	Low-level Output Current at RESET		V_O = 0 V			– 50	
I_S	Supply Current		All Inputs and out. open		1.8	3.3	mA

Notes : 1. All characteristics are measured with C = 0.1 µF from Pin 1 to GND, and with C = 0.1 µF from Pin 3 to GND.
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse Width at SENSE Input	$V_{ih} = V_{ityp} + 0.04 \times V_i$ $V_{iL} = V_{ityp} - 0.04 \times V_i$	0.9			µs
t_{pi}	Pulse Width at $\overline{\text{RESIN}}$ Input		0.4			µs
t_{po}	Pulse Width at Output	$C_f = 0.1\ \mu F$	0.65	1.3	2.6	ms
t_{pdHL}	Propagation Delay Time from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	$C_L = 100$ pF $V_S = 5$ V $R_L = 4.7\ K\Omega$			1	µs
$t_{r/f}$	Rise/Falltime at $\overline{\text{RESET}}$ and $\overline{\text{RESET}}$	$C_L = 10$ pF $V_S = 5$ V $R_L = 4.7\ K\Omega$			1	µs

Figure 1 : Multiple Power Supply System Reset Generation.

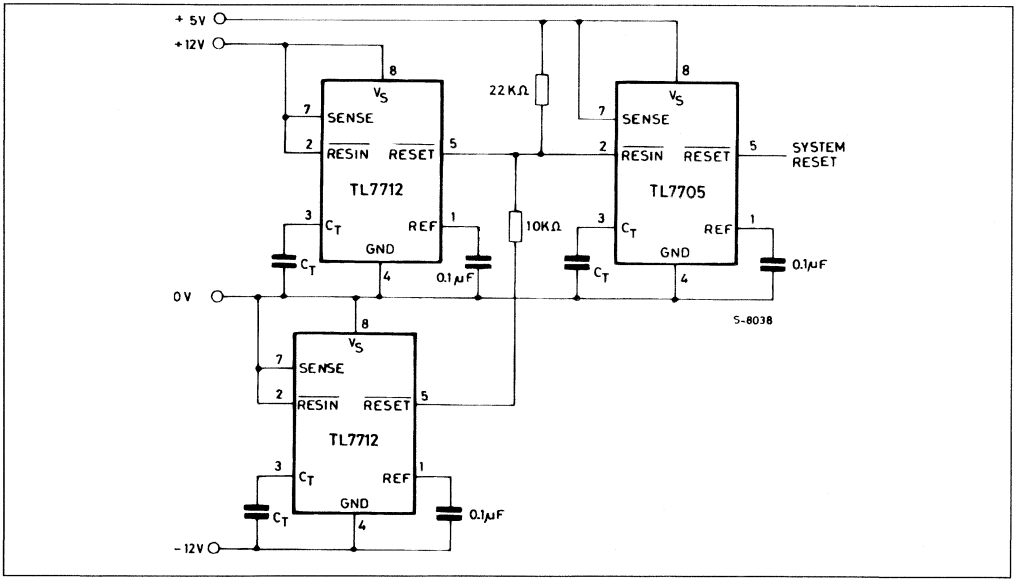
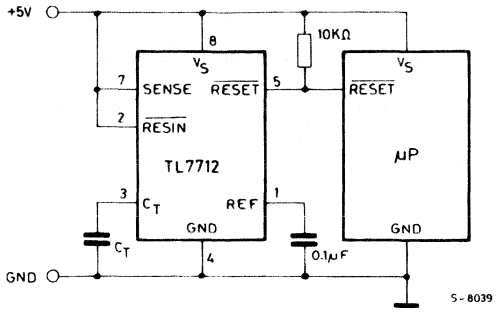


Figure 2 : Reset Controller for μP.



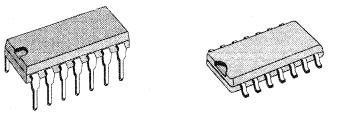
SGS-THOMSON MICROELECTRONICS

UAA4713

MOTION DETECTOR INTERFACE

ADVANCE DATA

- 50/ 60 Hz AC SUPPLY
- INPUT FOR PYROELECTRICAL SENSOR
- INPUT FOR PHOTORESISTIVE SENSOR
- SENSOR FILTER AMPLIFIER
- PROGRAMMABLE ON-TIMER
- TRIAC OUTPUT AND RELAY OUTPUT
- SHORT CIRCUIT PROTECTION
- LOW QUIESCENT CURRENT
- TWO-WIRE TECHNIQUE



DIP-14 **SO-14**

ORDERING NUMBERS:

UAA4713DP UAA4713FP

DESCRIPTION

The UAA4713 is a monolithic integrated circuit intended to control triac or relay switch for AC-mains timer applications.The device can be used in a wide range of industrial and consumer applications as light control, automatic door opening detector, fire alarm, fluid level control .

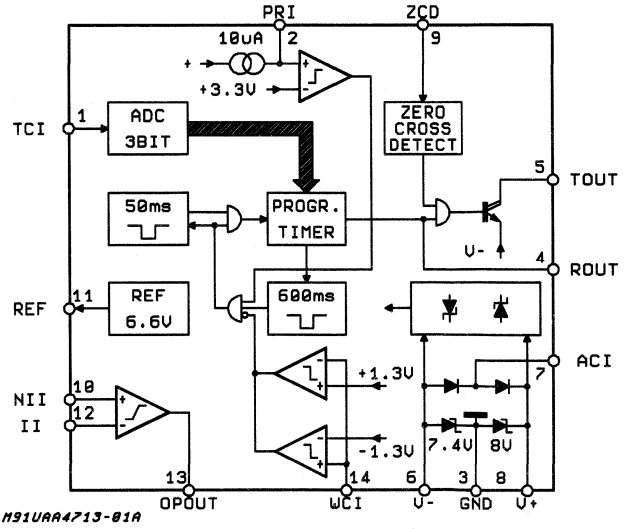
The circuit processes the output signal of an infrared pyroelectric detector which senses temperature changes caused by heat radiation of the human body.

If the sensor detects a temperature change, a programmable timer will start and switch a lamp or other loads to the mains.

A further input for a photo-resistive sensor allows to program circuit operation depending on the day-light intensity.

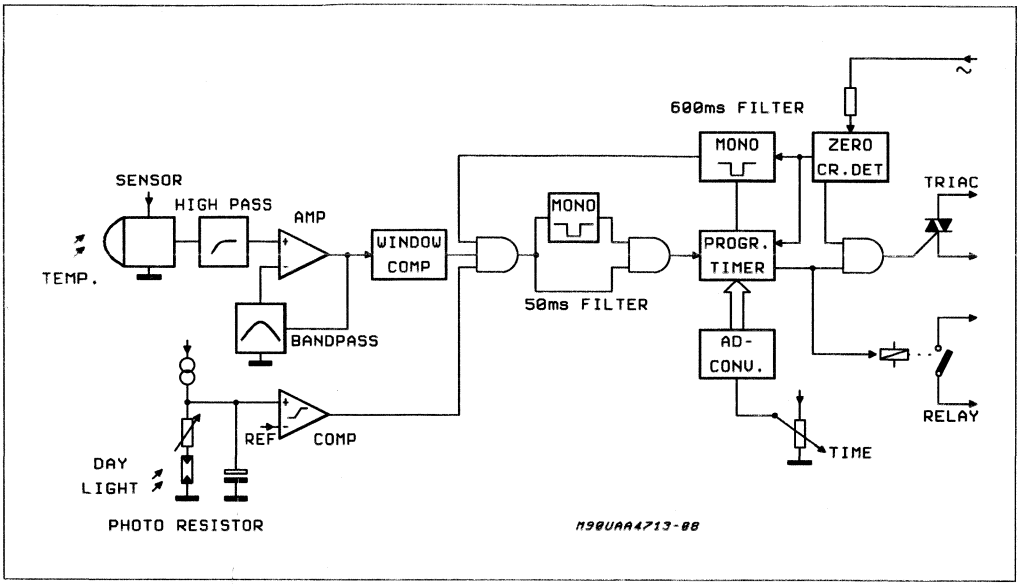
Internal circuits avoid false triggering of the external actuators. (see functional diagram).

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

FUNCTIONAL DIAGRAM



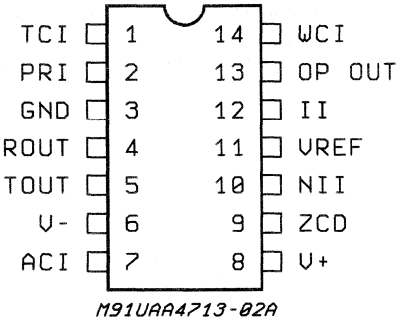
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
I7	AC Supply Current	60	mA
I7	Peak Current (T.P < 200µs)	200	mA
I7	Sourge Current (not repetitive 10ms)	500	mA
I9	ZCD Max. Input Current	5	mA
V6-3	Negative Clamp Voltage	-9	V
V8-3	Positive Clamp Voltage	9.5	V
V14-3	Comp. Input Voltage	±8	V
V10-12	Differential Input Voltage	±8	V
Top	Operating Temperature	-25 to 85	°C
T_{stg}, T_j	Junction and Storage Temperature	-40 to 150	°C
P_{tot}	Total Power Dissipation (T_j = 85°C)	650	mW

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	100	°C/W

PIN CONNECTION (Top view)



M91UAA4713-02A

PIN FUNCTIONS

Pin	Symbols	Functions
1	TCI	Time control Input
2	PRI	Photosensor comparator input
3	GND	Ground
4	R_{OUT}	Relay output
5	T_{OUT}	Triac output
6	V-	Negative clamp voltage
7	ACI	AC-input supply
8	V+	Positive clamp voltage
9	ZCD	Zero cross detector
10	NII	Non-invert input sensor amplifier
11	V_{REF}	Sensor reference voltage
12	II	Invert input sensor amplifier
13	OP OUT	Output sensor amplifier
14	WCI	Window comparator input

ELECTRICAL CHARACTERISTICS (I_S = ± 2mA to ±10mA;T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
I_S	Operative Supply Current		7	±0.7		± 15	mA
V-	Negative Clamping Voltage	$\pm I_S$ = 0.7mA	6	-7.8		-7	V
V+	Positive Clamping Voltage		8	7.6		8.4	V
V_{REF}	Sensor Reference Voltage	I_{REF} = 50µA I_{REF} = 200µA	11	6 5	6.6	7.2 7.2	V V
I_{ROUT}	Output Current Relay Driver	during on-time V_{ROUT} = 0V	4	80			µA
$V_{R\ HIGH}$	Relay Driver Source Saturation Voltage	$I_{R\ OUT}$ = 80µA	4			2	V
I_R	Relay Sink Output Current	$V_{R\ OUT}$ = 0.4V during on-time	4	1		8	mA
I_{TOUT}	Triac Firing Current		5	50	65		mA
V_{ZCD}	Zero Cross Detector Clamping Voltage		9	±7.4	±8	±8.6	V
I_{ZCD}	Zero Cross Detector Operating Current		9	1.6		10	µA
I_{PRI}	Photoresistor Source Current	V_{PRI} = 0V	2	6	10	14	µA
V_{PRth}	Photoresistor Threshold Voltage	I_S = 0.7mA	2	3	3.3	3.6	V
I_{TCI}	Timer Control Input Current	V_{TCI} 0 to V+	1	0		0.5	µA
t_{TIM}	On-Timer Counter Duration (depends on the mains frequency and on externally adjustable Timer Control Input Voltage) ± 1/2 cicle precision	V_{TCI}	14/4	**50**		**60**	Hz
		11/12 V+		0		0	s
		9/12 V+		4.48		3.73	s
		7/12 V+		40		33.3	s
		5/12 V+		81		67.5	s
		3/12 V+		163		135.8	s
		1/12 V+		327		272.5	s
		0V (GND)	Continue				
t_D	Delay Time Between Window Comparator Input and Timer Start	50Hz	14/4	40	50	60	ms
		60Hz		33.3	41.6	50	ms
t_{DR}	Delay Time Between Timer Stop to Retrigger	50Hz	14/4		500		ms
		60Hz			600		ms
I_{TOL}	Triac Output Leakage Current	V_{TO} = 0V	5			10	µA
$V_{th\ WCI}$	Window Comparator T4	Pin 2 open	14/4	±1.20	±1.3	±1.40	V
I_{WCI}	Window Comparator Input Current	V_{WCI} = -2V to + 2V	14			± 1	mA
OP. AMP.							
R_I	Input Resistance		10/12		1		MΩ
I_{IO}	Input Offset Current		10/12			25	nA
I_{IB}	Input Bias Current		10/12			1	µA
V_{IO}	Input Offset Voltage		10/12	- 10		+10	mV
V_{CM}	Common Mode Volt. Renge		10/12	- 4.5		5	V
V_O	Output Voltage Swing		13	±4		±5	V
I_O	Output Current		13		1.5		mA
I_{SC}	Output Short Circuit Current		13			3	mA
G_V	Large Signal Open Loop Voltage Gain	R_L = 10K		80	100		V

Figure 1: Open Loop Frequency Response

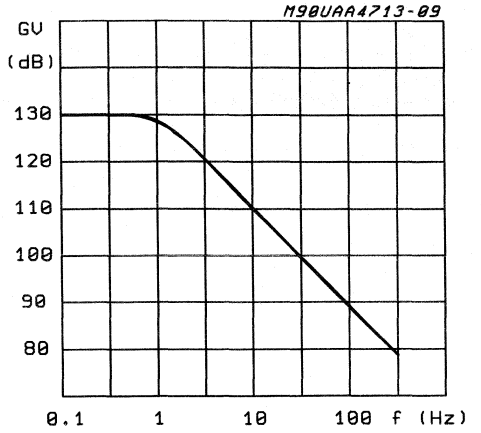


Figure 2: V_{REF} versus I_{REF}

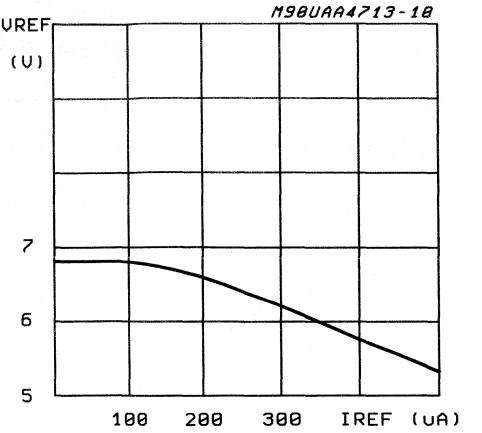
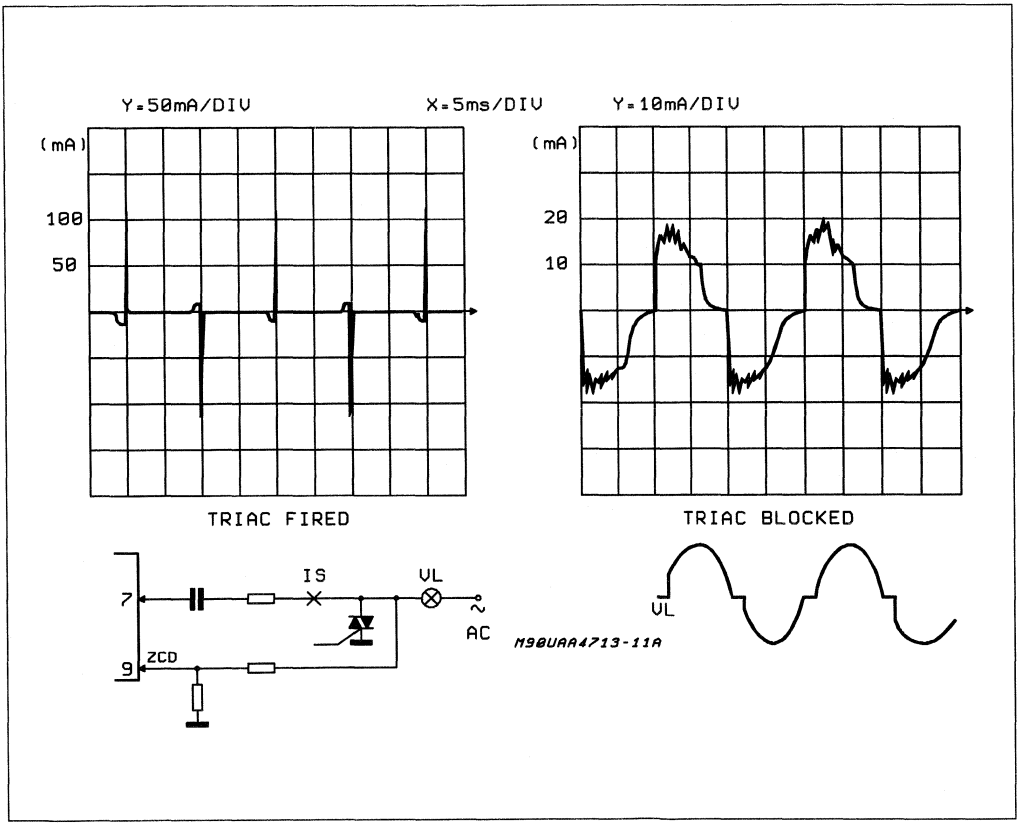


Figure 3: Supply Current



SYSTEM DESCRIPTION (see Functional Diagram)

If a heat source moves in front of the IR-detector, the sensor delivers a quasi sinusoidal AC-signal in the µV to mV range. The operational amplifier amplifies the sensor signal by 72dB.

To reject an unwanted signal, a band pass filter is needed. If the AC-level at pin 14 exceeds the window comparator thresholds, the programmable timer will start. To suppress short sensor signals, a 50ms time filter is implemented between the window comparator output and the programmable timer. This function improves the noise immunity.

After the reset of the timer a second timer will provide a 600ms dead time to prevent retriggering of the timer. This function avoids restarting of the timer, when the turned off lamp temperature. decreases
The lamp switched by the triac can be located close to the sensor.

To avoid circuit operation during day-time, a photo resistor (LDR) senses the light intensity and switches off the circuit. The capacitor at pin 2 prevents circuit start-up during short shadow phases, when a person passes by the sensor.

From the analog input pin 1 via the AD-converter the on-time duration can be programmed in 7 steps (see t_{TIM} table in the electical characteristics). The timer is clocked by the mains frequency.

Two outputs for various applications are available.
Pin 5 is the trigger output for triac gate.
Pin 4 output can be used to switch a relay or other loads.
The zero crossing detector provides the firing pulse for the triac at the right time, shortly after the zero crossing of the AC-signal.

The RC-network at pin 7 supplies current to the circuit via a double wave rectification which is provided by a split power supply. Due to the capacitive energy transfer into pin 7, the circuit will also be supplied with current if the triac is fired. A short wire for circuit supply is not needed.

The circuit works similar to a simple two-terminal switch and can be installed in parallel with ordinary mechanical pulse switches (fig. 4).
After a short supply connection via an external pulse switch, the circuit timer will also start without a sensor signal.
Therefore the circuit can also be used as an ordinary light timer without the IR-moving sensor feature.

Figure 4

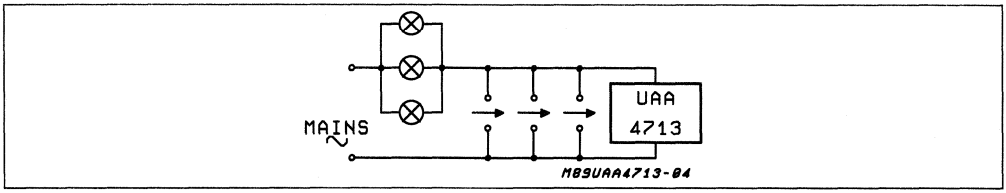


Figure 5: Different Possible Filter Solutions

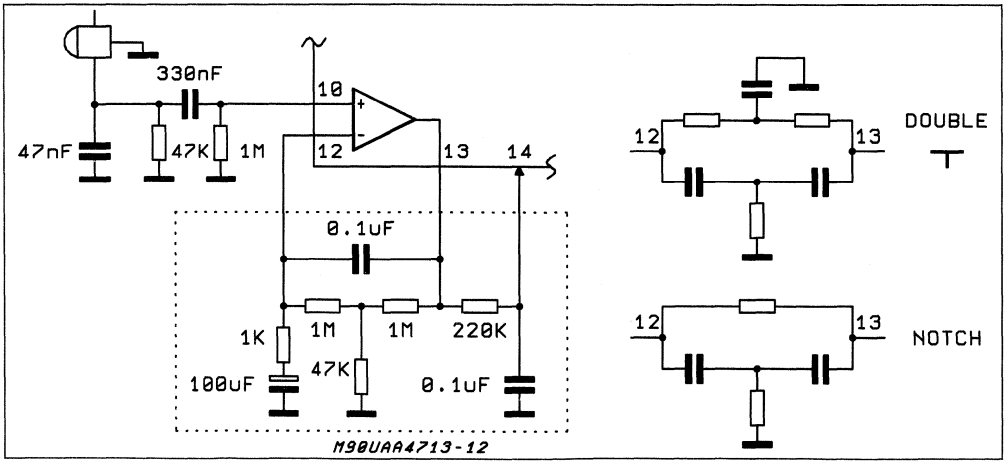


Figure 6: Triac Application

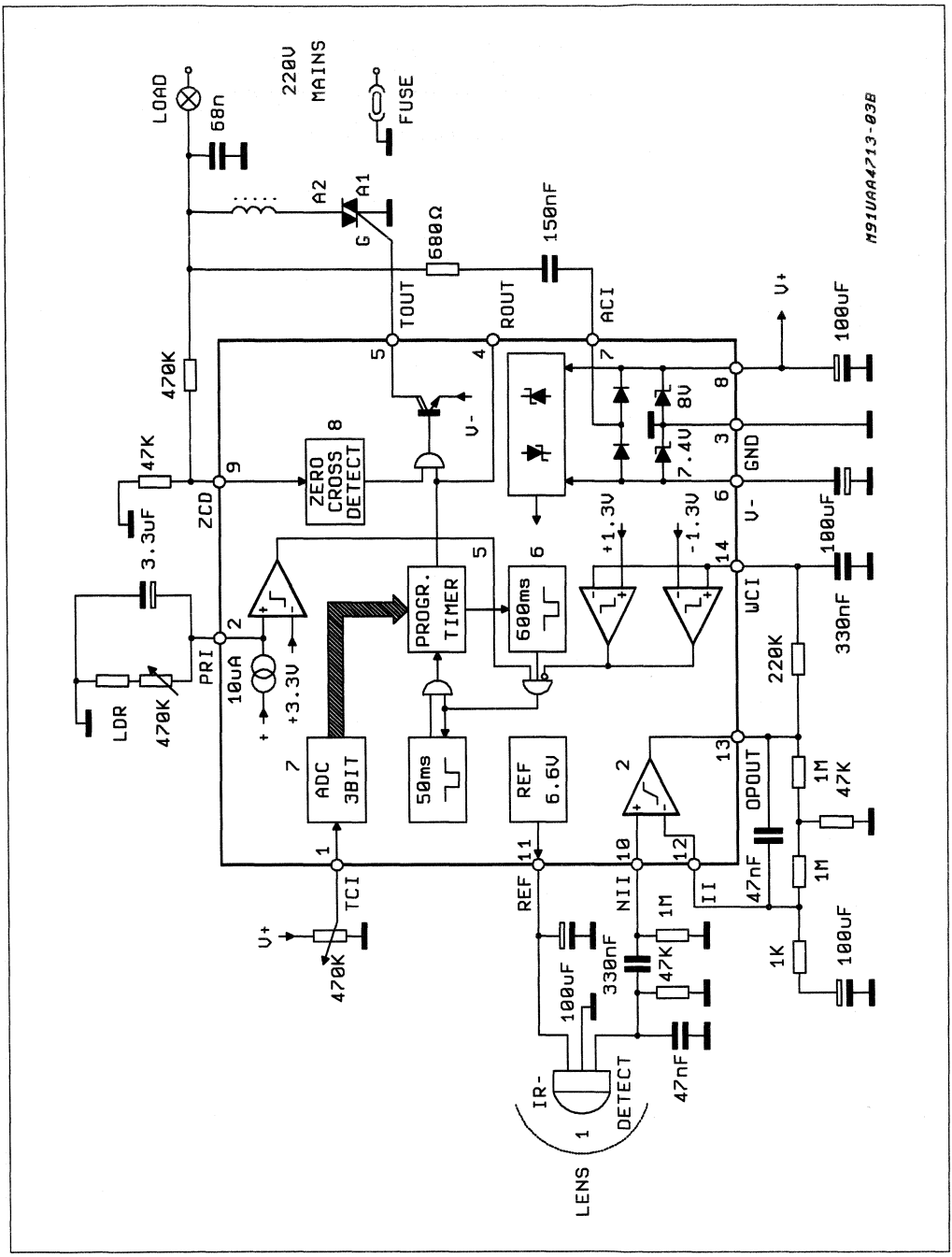
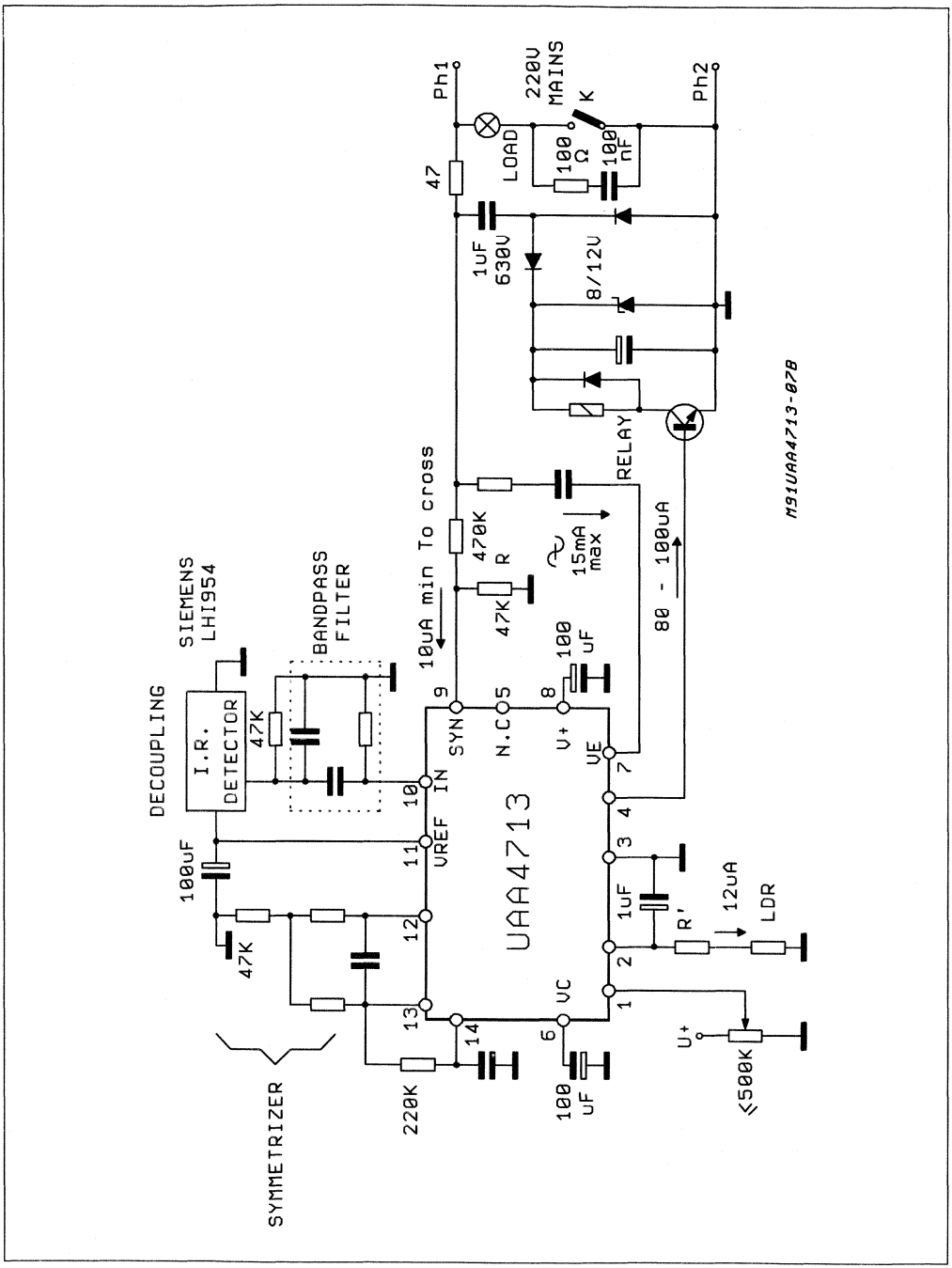


Figure 7: Relay Application



APPLICATION INFORMATION

1. HOW TO CHOOSE THE TRIAC ASSOCIATED TO THE MOTION DETECTOR UAA4713

Analysis of the Triac Associated to the Motion Detector UAA4713

Associated with the UAA4713, the Triac is defined by the driver output stage (Triac output pin 5) and the characteristics of the load.

The Triac is consequently defined by:

1) The gate sensitivity
2) The surge current capability
3) The RMS Triac current
4) The blocking voltage capability

1) The gate sensitivity

The "Triggering gate current" is the parameter to be taken into consideration. The I_{GT} is given at 25°C. as a maximum value required to trigger the Triac.

ex. BTA06-600CW = $I_{GT\ max}$ (mA) = 35mA

The UAA4713 Triac output provides a current of 65mA typical.

$$I_{Tout} = 65mA(Typ) = I_G$$

In order to control the Triac properly IG should be greater than 1.5 x I_{GT} or

$$I_{Tout} > 1.5\ I_{GT}$$

For this reason it is suggested to use a snubberless Triac of the CW series (I_{GT} < 35mA).

2) The surge current capability

In the Triac databook the surge current capability of the Triac is given by the non repetitive surge peak current:

I_{TSM}

ex. BTA06-600CW

I_{TSM} at $T_{J\ initial}$ = 25°C

t = 8.3mA: 63A
t = 10ms: 60A

The choice of the Triac is defined by the following application parameters:

a)The starting performance, and the ratio of the nominal resistance to the cold resistance, KR

$$I_{max} > KR \times I_{nominal} \times \sqrt{2}$$

b)The thermal fast fuse behaviour during short-circuit condition.

$$(I^2t)\ (Triac) > (I^2t)\ (fuse)$$

To select the I_{Tsm} (given as a minimum value) the following table is suggested.

Mains: V_{AC} (V)	240V	110V
Power (W)	$I_{Tsm\ (min)}$	$I_{Tsm\ (min)}$
600	50	80
1000	80	120
>1000	>100	>150

3) RMS Triac Current

The RMS Triac current I_{TRMS} is defined by the light power P:

$$I_{TRMS} > 1.25 \times P \times V_{AC}$$

It depends also on the heat sink which has to limit the junction temperature in the worse case conditions ($T_{amb\ max}$ and I_{TRMS}).
With the snubberless triac I_{TRMS} ranges from 6A to 25A.

4) Blocking Voltage Capability

The maximum blocking voltage VD_{RM} is defined by the mains:

Country	Mains Voltage (V) V_{AC}	V_{DRM} (V)
EUROPE	240	600
USA	110	400

5) Conclusion:

Selector guide with the above parameters the optimal device selection for a given power to be controlled is given in the following table:

LIGHT POWER (W)	MAINS VOLTAGE V_{AC} (V)	
	240	110
600	BTA 06 600 CW	BTA 08 400 CW
1,000	BTA 08 600 CW	BTA 12 400 CW
> 1,000	BTA X 600 CW X = 10 X = 12 X = 16	BTA X 400 CW X = 12 X = 16 (A)

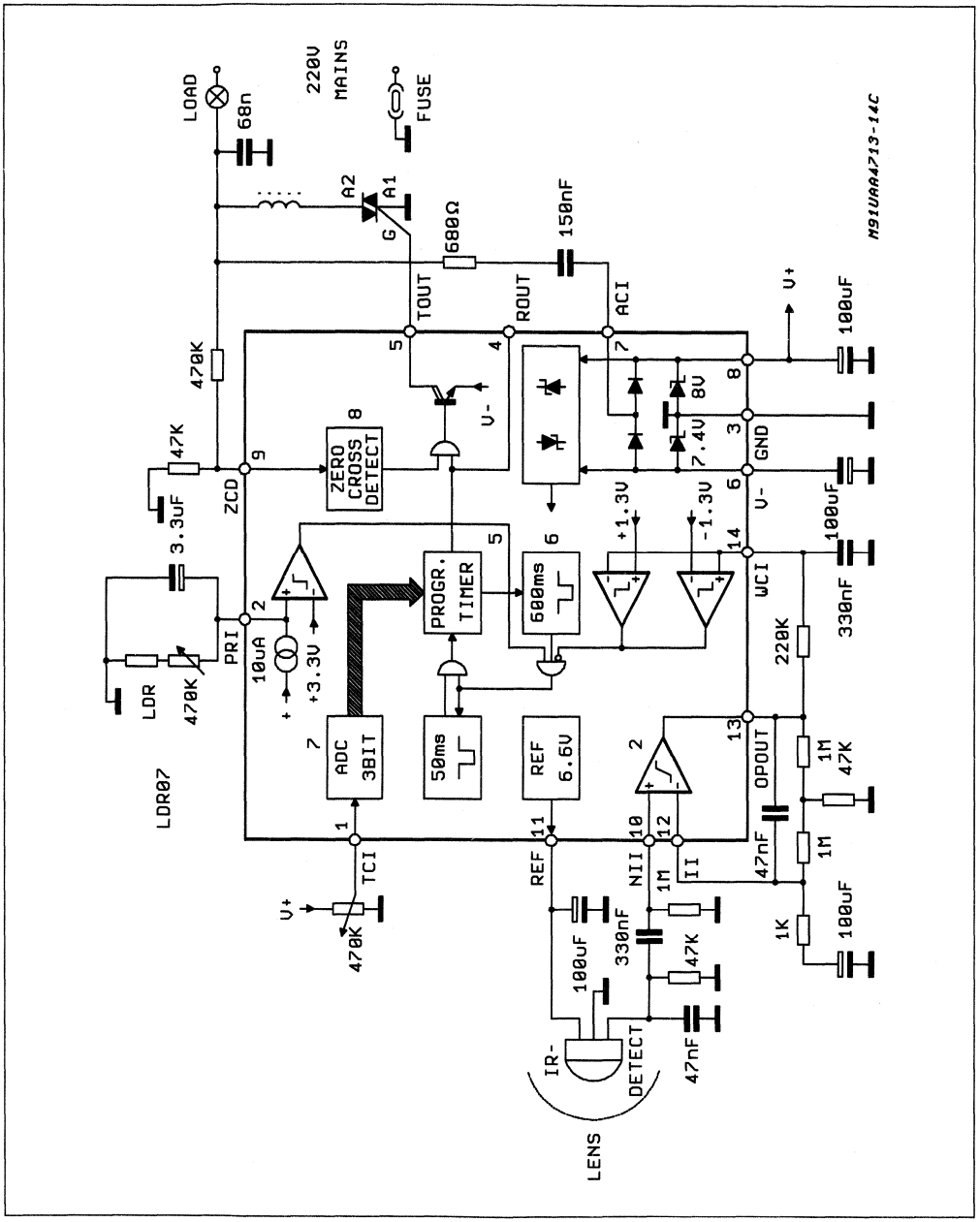
Ref: High Performance Triacs that need no snubber (DSTRIACBK/1088)

APPLICATION INFORMATION (continued)

2. MOTION DETECTOR DEMO BOARD

This document allows the user to construct rapidly a Demo and Test Board for the UAA4713

Figure 8: Demo Board Diagram



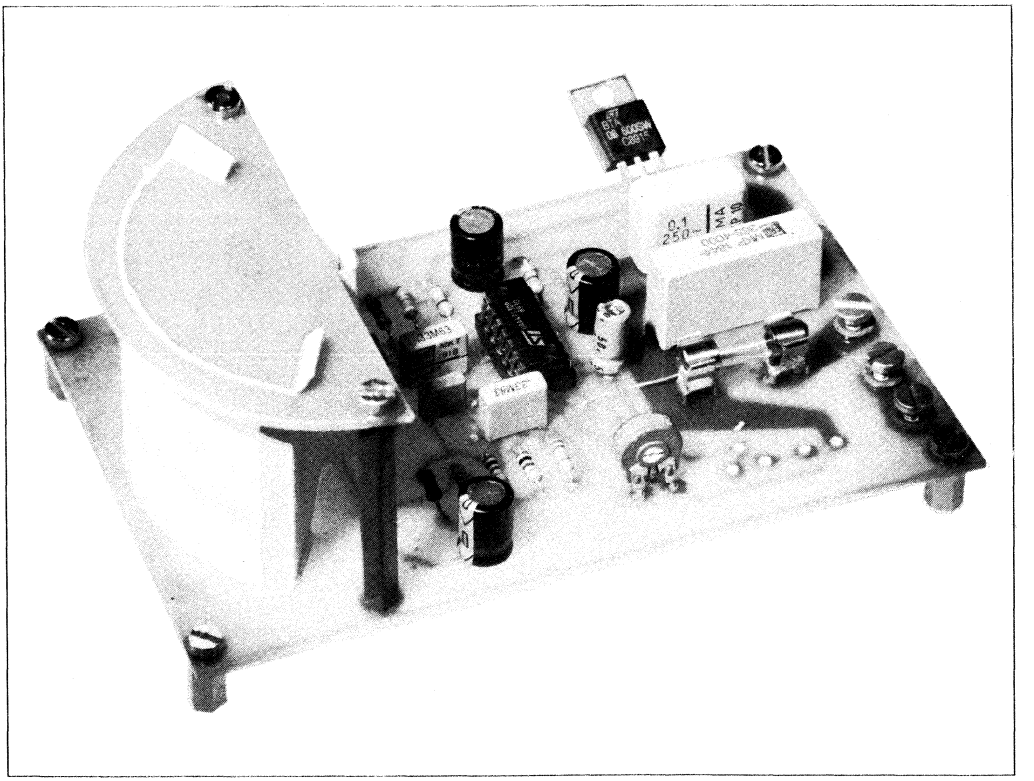
APPLICATION INFORMATION (continued)

Demo Board - Part List

QTY	DEVICE	DESCRIPTION	SUPPLIER
1	UAA4713DP OR UAA4713FP	INTEGRATED CIRCUIT	SGS-THOMSON
1	BTA06-600 (240V mains) BTA08-400 (110V mains)	TRIAC TRIAC	SGS-THOMSON SGS-THOMSON
1	KRX10FL or IRA - EI00S series	SENSOR WITH FRESNEL LENS Pyroelectic Infrared Sensor	PHILIPS COMPONENTS MURATA
1	LDR07	PHOTORESISTOR	PHILIPS COMPONENTS

CAPACITORS		RESISTORS (0.25W)	
QUANTITY	VALUE	QUANTITY	VALUE
4	100µF/35V	3	1MΩ
2	330nF	3	47kΩ
2	47nF	1	680Ω
1	4.7nF	1	1KΩ
1	68nF 400V	1	470KΩ
1	150nF 250V	1	220KΩ
1	3.3µF 35V	2 POTENTIOMETERS	500KΩ

Figure 9: Demo Board Photo IRA - E100S



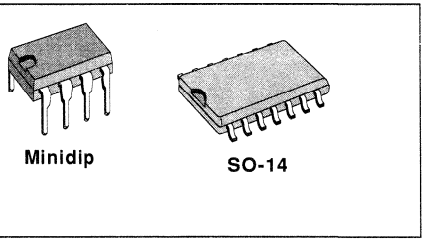
CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_O ERROR AMP

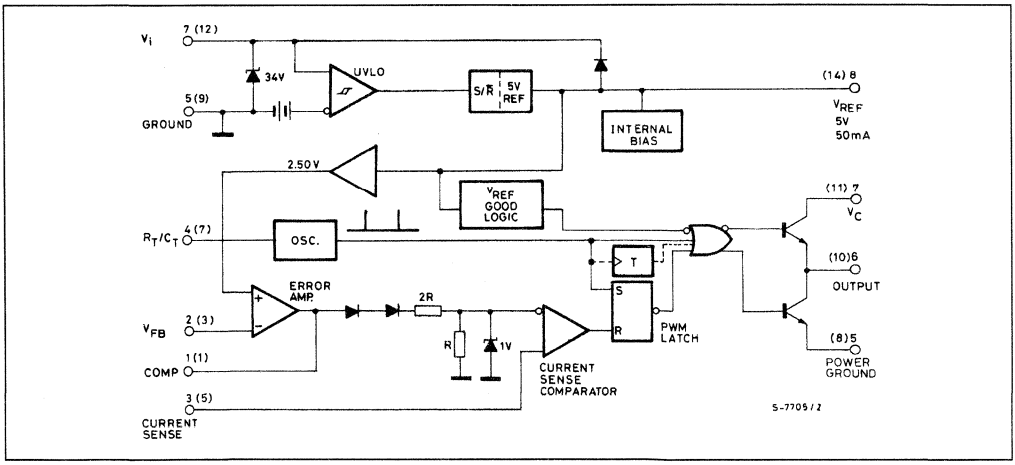
DESCRIPTION

The UC3842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842 and UC3844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications The corresponding thresholds for the UC3843 and UC3845 are 8.5 V and 7.9 V. The UC3842 and UC3843 can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844 and UC3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



BLOCK DIAGRAM (toggle flip flop used only in U3844 and UC3845)



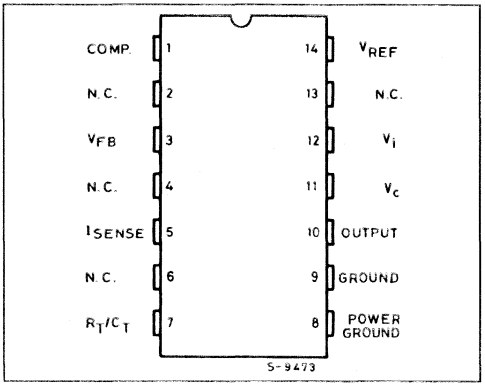
ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (I_i < 30 mA)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	− 0.3 to 6.3	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 50$ ° C (minidip, DIP-14)	1	W
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ ° C (SO-14)	725	mW
T_{stg}	Storage Temperature Range	− 65 to 150	°C
T_L	Lead Temperature (soldering 10 s)	300	°C

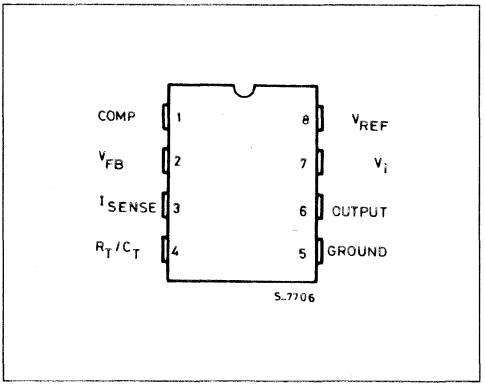
* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTION (top view)

SO14



Minidip



ORDERING NUMBERS

Type	Minidip	SO14
UC2842	UC2842N	UC2842D
UC3843	UC2843N	UC2843D
UC2844	UC2844N	UC2844D
UC2845	UC2845N	UC2845D
UC3842	UC3842N	UC3842D
UC3843	UC3843N	UC3843D
UC3844	UC3844N	UC3844D
UC3845	UC3845N	UC3845D

THERMAL DATA

Symbol	Description		Minidip	SO14	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient.	max.	100	165	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-25 \leq T_{amb} \leq 85°C$ for UC2824X; $0 \leq 70°C$ for UC384X; $V_i = 15V$ (note 5); $R_T = 10K$; $C_T = 3.3nF$)

Symbol	Parameter	Test Conditions	UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	$T_j = 25$ °C $I_o = 1$ mA	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	$12\ V \leq V_i \leq 25\ V$		6	20		6	20	mV
ΔV_{REF}	Load Regulation	$1 \leq I_o \leq 20$ mA		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
	Total Output Variation	Line, Load, Temperature (Note 2)	4.9		5.1	4.82		5.18	V
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 10 KHz T_j = 25 °C (Note 2)		50			50		μV
	Long Term Stability	T_{amb} = 125 °C, 1000 Hrs (Note 2)		5	25		5	25	mV
I_{sc}	Output Short Circuit		−30	−100	−180	− 30	−100	−180	mA
OSCILLATOR SECTION									
f_s	Initial Accuracy	T_j = 25 °C (Note 6)	47	52	57	47	52	57	KHz
	Voltage Stability	$12 \leq V_i \leq 25\ V$		0.2	1		0.2	1	%
	Temperature Stability	$T_{MIN} \leq T_{amb} \leq T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	V_{PIN4} Peak to Peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input Voltage	V_{PIN1} = 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input Bias Current			− 0.3	− 1		− 0.3	− 2	μA
	A_{VOL}	$2 \leq V_o \leq 4\ V$	65	90		65	90		dB
B	Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
SVR	Supply Voltage Rejection	$12 \leq V_i \leq 25\ V$	60	70		60	70		dB
I_o	Output Sink Current	V_{PIN2} = 2.7 V V_{PIN1} = 1.1 V	2	6		2	6		mA
I_o	Output Source Current	V_{PIN2} = 2.3 V V_{PIN1} = 5 V	− 0.5	− 0.8		− 0.5	− 0.8		mA
	V_{OUT} High	V_{PIN2} = 2.3 V ; R_L = 15 KΩ to Ground	5	6		5	6		V
	V_{OUT} Low	V_{PIN2} = 2.7 V ; R_L=15 KΩ to Pin 8		0.7	1.1		0.7	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT SENSE SECTION									
G_v	Gain	(Notes 3 & 4)	2.85	3	3.15	2.8	3	3.2	V/V
V_3	Maximum Input Signal	V_{PIN1} = 5 V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	12 ≤ V_i ≤ 25 V (Note 3)		70			70		dB
I_b	Input Bias Current			– 2	– 10		– 2	– 10	µA
	Delay to Output			150	300		150	300	ns
OUTPUT SECTION									
I_{OL}	Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200 mA		1.5	2.2		1.5	2.2	
I_{OH}	Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		12	13.5		
t_r	Rise Time	T_j = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
t_f	Fall Time	T_j = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
		X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
	Min. Operating Voltage After Turn-on	X842/4	9	10	11	8.5	10	11.5	V
		X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION									
	Maximum Duty Cycle	X842/3	93	97	100	93	97	100	%
		X844/5	46	48	50	47	48	50	
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current			0.5	1		0.5	1	mA
I_i	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0 V		11	20		11	20	mA
V_{iz}	Zener Voltage	I_i = 25 mA		34			34		V

Notes : 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{PIN2} = 0.
4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8 V$$

5. Adjust V_i above the start threshold before setting at 15 V.
6. Output frequency equals oscillator frequency for the UC3842 and UC3843.
Output frequency is one half oscillator frequency for the UC3844 and UC3845.

Figure 1 : Error Amp Configuration.

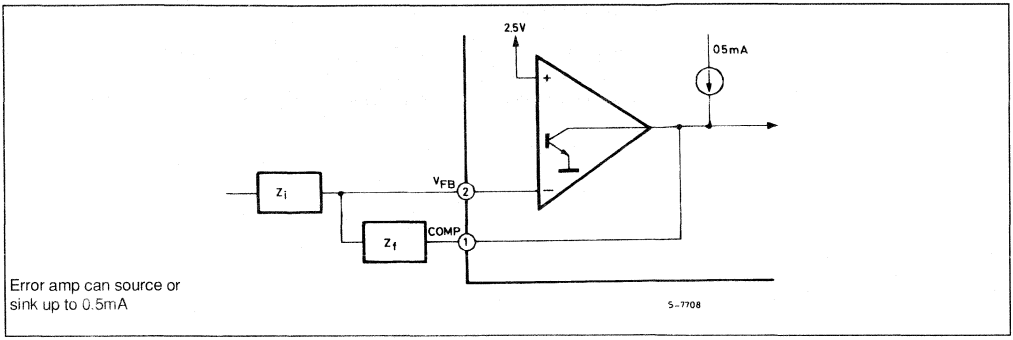
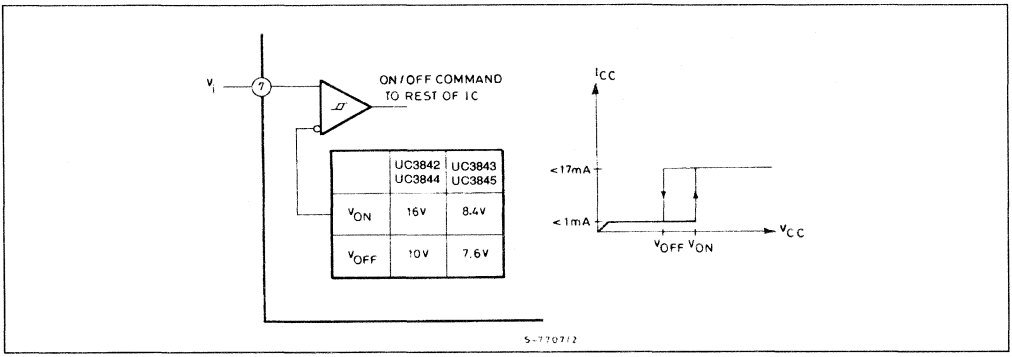
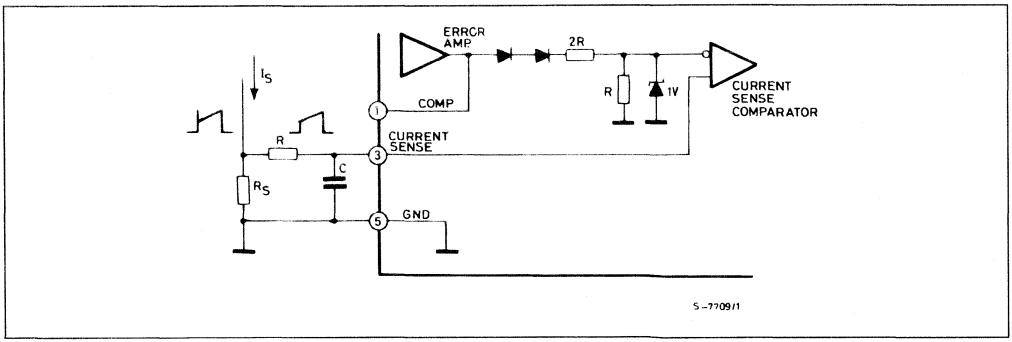


Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit .



Peak current (i_S) is determined by the formula

$$I_{S\ max} \approx \frac{1.0\ V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 4.

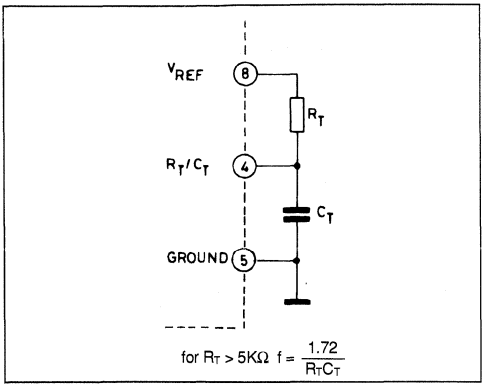


Figure 5 : Deadtime vs. C_T (R_T > 5KΩ).

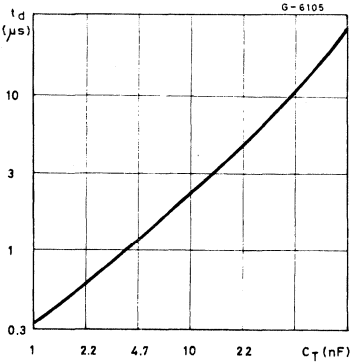


Figure 6 : Timing Resistance vs. Frequency.

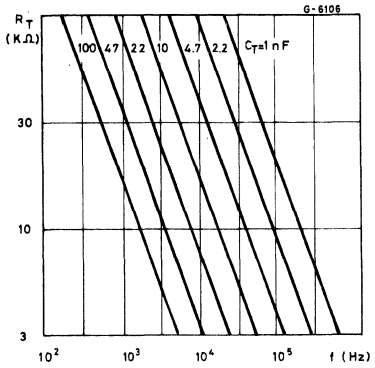


Figure 7 : Output Saturation Characteristics.

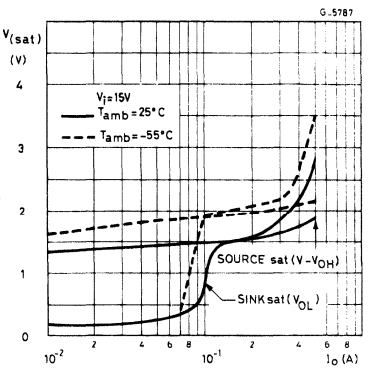


Figure 8 : Error Amplifier Open-loop Frequency Response.

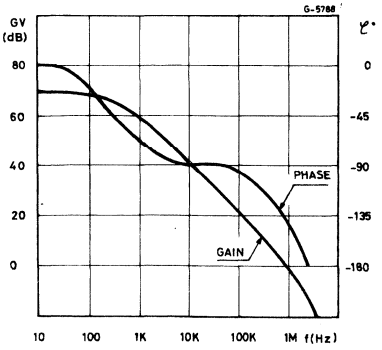
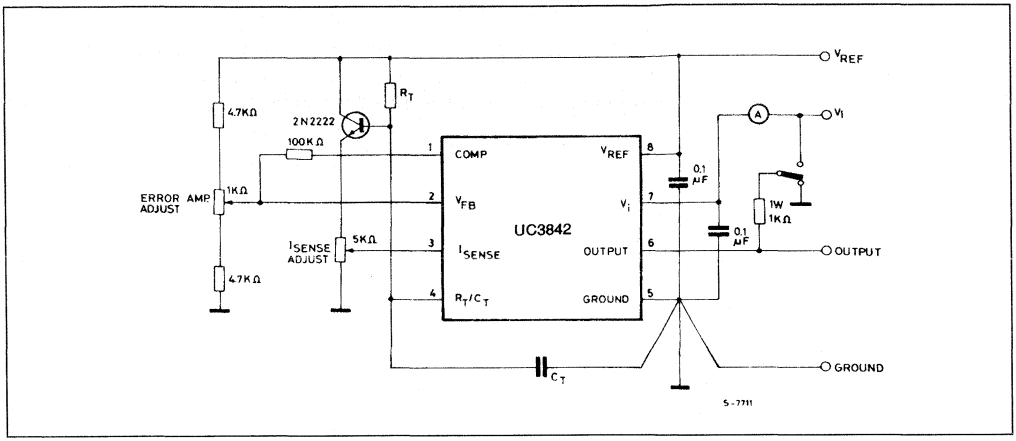
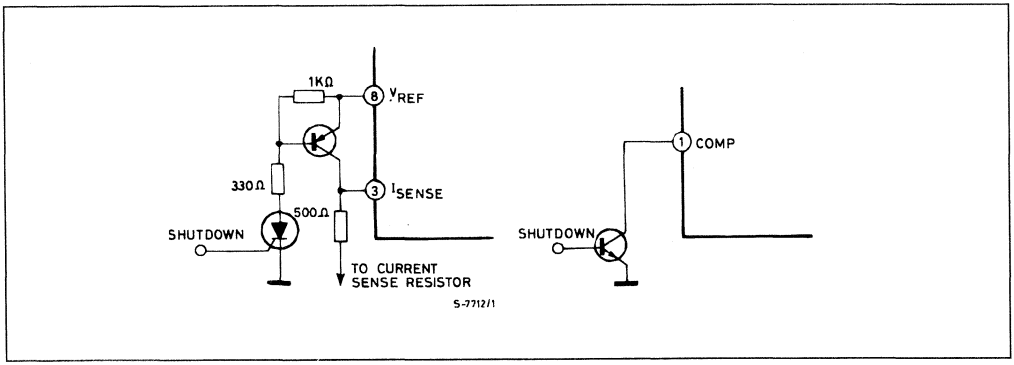


Figure 9 : Open Loop Test Circuit.



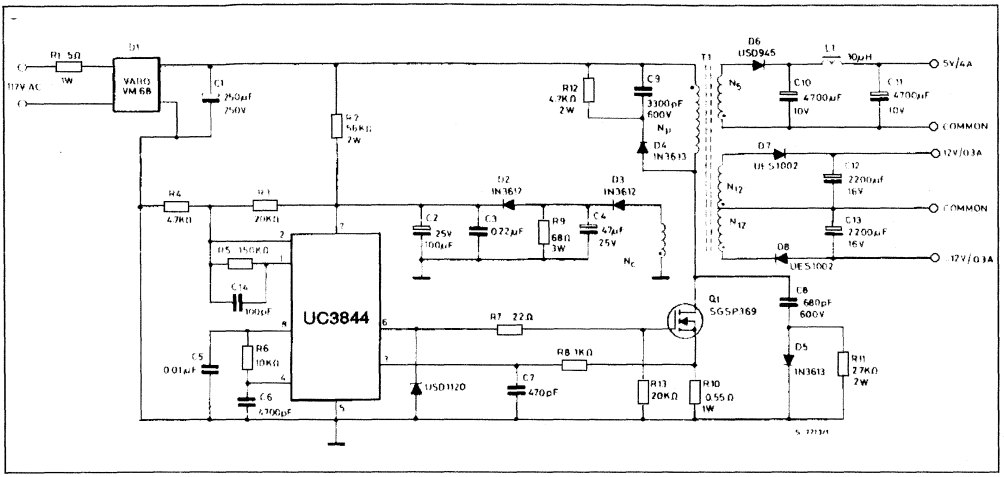
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.



Shutdown of the UC2842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

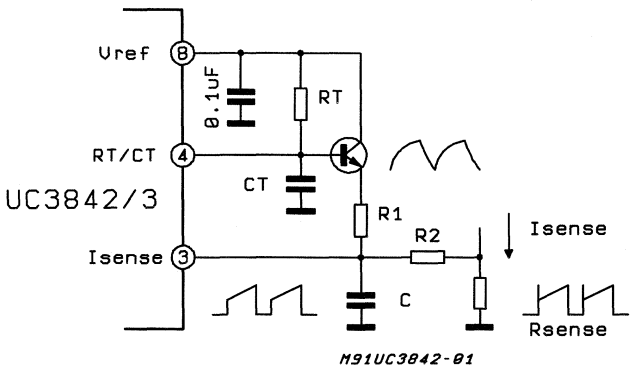
Figure 11 : Off-line Flyback Regulator.



Power Supply Specifications

1. Input Voltage : 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation : 3750 V
3. Switching Frequency : 40 KHz
4. Efficiency @ Full Load : 70 %
5. Output Voltage :
   A. + 5 V, ± 5 % : 1 A to 4 A load
   Ripple voltage : 50 mV P-P Max.
   B. + 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.
   C. – 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.

Figure 12 : Slope Compensation.



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50 %.

Note that capacitor, C, forms a filter with R_2 to supress the leading edge switch spikes.

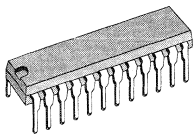
SGS-THOMSON MICROELECTRONICS

UDN2916A

STEPPER MOTOR DRIVER

ADVANCE DATA

- ABLE TO DRIVE BOTH WINDINGS OF BIPOLAR STEPPER MOTOR
- OUTPUT CURRENT UP TO 750mA EACH WINDING
- WIDE VOLTAGE RANGE 10V TO 50V
- HALF-STEP, FULL-STEP AND MICROSTEPPING MODE
- BUILT-IN PROTECTION DIODES
- INTERNAL PWM CURRENT CONTROL
- LOW OUTPUT SATURATION VOLTAGE
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- INTERNAL THERMAL SHUTDOWN



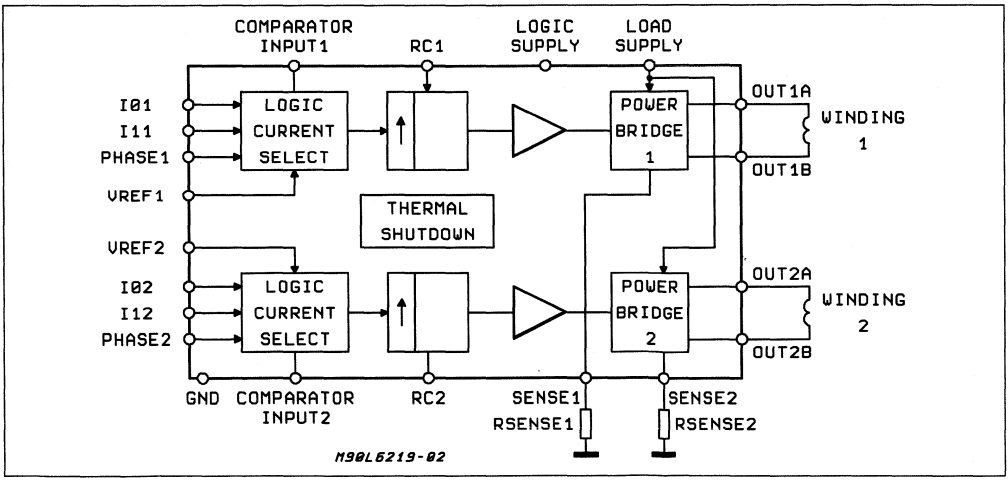
Powerdip 20+2+2

ORDERING NUMBER: UDN2916A

DESCRIPTION

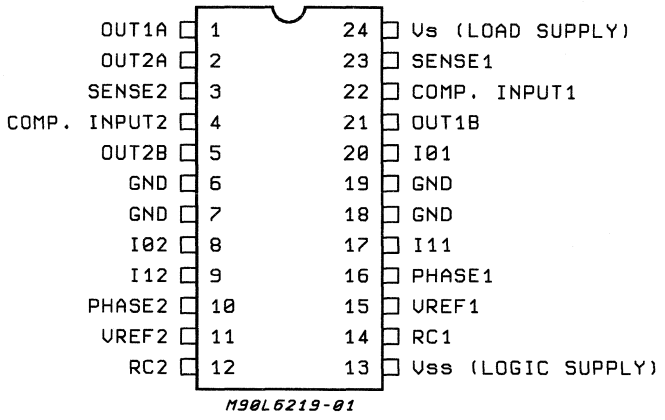
The UDN2916A is a bipolar monolithic integrated circuits intended to control and drive both winding of a bipolar stepper motor or bidirectionally control two DC motors.
The UDN2916A with a few external components form a complete control and drive circuit for LS-TTL or microprocessor controlled stepper motor system.
The power stage is a dual full bridge capable of sustaining 50V and including four diodes for current recirculation.
A cross conduction protection is provided to avoid simultaneous cross conduction during switching current direction.
An internal pulse-width-modulation (PWM) controls the output current to 750mA with peak start-up current up to 1A.
Wide range of current control from 750mA (each bridge) is permitted by means of two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction.
A thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (Top view)



PIN FUNCTIONS

N°	Name	Function
1;2	OUTPUT A	See pins 5;21
3;23	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor
4;22	COMPARATOR INPUT	Input connected to the comparators. The voltage across the sense resistor is feedback to this input throught the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_T C_T (t_{off} = 1.1 R_T C_T). See fig. 1.
5;21	OUTPUT B	Output Connection. The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
6;19	GROUND	See pins 7;18
7;18	GROUND	Ground Connection. With pins 6 and 19 also conducts heat from die to printed circuit copper.
8;20	INPUT 0	See INPUT 1 (pins 9;17)
9;17	INPUT 1	These pins and pins 8;20 (INPUT 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See Funcional Description.
10;16	PHASE	This TTL-compatible logic inputs sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
11;15	REFERENCE VOLTAGE	A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on R_S and the two inputs INPUT 0 and INPUT 1).
12;14	RC	A parallel RC network connected to this pin sets the OFF time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators (t_{off} = 1.1 R_T C_T).
13	V_{ss} - LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry
24	V_S - LOAD SUPPLY	Supply Voltage Input for the Output Stages.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
I_o	Output Current (peak)	±1	A
I_o	Output Current (continuous)	±0.75	A
V_{SS}	Logic Supply Voltage	7	V
V_{IN}	Logic Input Voltage Range	-0.3 to +7	V
V_{sense}	Sense Output Voltage	1.5	V
T_j	Junction Temperature	+150	°C
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{thj\text{-}ambient}$	Thermal Resistance Junction-ambient	Max	60	°C/W

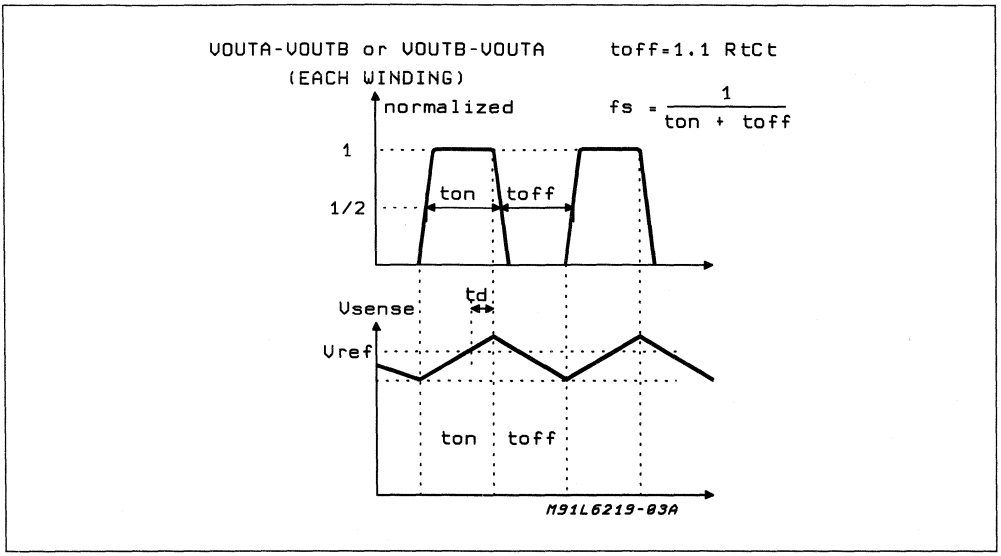
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, $T_{tab} \leq 70$°C, V_S = 50V, V_{SS} = 4.75V to 5.25V, V_{REF} = 5V; unless otherwise specified) See fig. 3.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT DRIVERS (OUT_A or OUT_B)						
V_S	Motor Supply Range		10		50	V
I_{CEX}	Output Leakage Current	V_{OUT} = Vs V_{OUT} = 0	- -	<1 <-1	50 -50	µA µA
$V_{CE(sat)}$	Output Saturation Voltage	Sink Driver, I_{OUT} = +500mA Sink Driver, I_{OUT} = +750mA Source Driver, I_{OUT} = -500mA Source Driver, I_{OUT} = -750mA	- - - -	0.3 0.7 1.1 1.3	0.6 1 1.4 1.6	V V V V
I_R	Clamp Diode Leakage Current	V_R = 50V	-	<1	50	µA
V_F	Clamp Diode Forward Voltage	Sink Diode Source Diode I_F =750mA		1 1	1.5 1.5	V V
$I_{S(on)}$	Driver Supply Current	Both Bridges ON, No Load	-	8	15	mA
$I_{S(off)}$	Driver Supply Current	Both Bridges OFF	-	6	10	mA
CONTROL LOGIC						
$V_{IN(H)}$	Input Voltage	All Inputs	2.4	-	-	V
$V_{IN(L)}$	Input Voltage	All Inputs	-	-	0.8	V
$I_{IN(H)}$	Input Current	V_{IN} = 2.4V	-	<1	20	µA
$I_{IN(L)}$	Input Current	V_{IN} = 0.84V	-	-3	-200	µA
V_{REF}	Reference Voltage	Operating	1.5	-	7.5	V
$I_{SS(ON)}$	Total Logic Supply Current	$I_o = I_1$ = 0.8V, No Load	-	54	64	mA
$I_{SS(OFF)}$	Total Logic Supply Current	$I_o = I_1$ = 2.4V, No Load	-	10	14	mA
COMPARATORS						
V_{REF} / V_{sense}	Current Limit Threshold (at trip point	$I_o = I_1$ = 0.8V	9.5	10	10.5	-
		I_o = 2.4V, I_1 = 0.8V	13.5	15	16.5	-
		I_o = 0.8V, I_1 = 2.4V	25.5	30	34.5	-
t_{off}	Cutoff Time	R_t = 56KΩ C_t = 820pF	-	50		µs
t_d	Turn Off Delay	Fig. 1	-	1		µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PROTECTION						
T_J	Thermal Shutdown Temperature		-	170	-	°C

Figure 1



FUNCTIONAL DESCRIPTION

The circuit is intended to drive both windings of a bipolar stepper motor.
The peak current control is generated through switch mode regulation.
There is a choice of three different current levels with the two logic inputs I_{01} - I_{11} for winding 1 and I_{02} - I_{12} for winding 2.
The current can also be switched off completely

Input Logic (I_0 and I_1)

The current level in the motor winding is selected with these inputs. (See fig. 2)
If any of the logic inputs is left open, the circuit will treat it has a high level input.

I_o	I_1	Current Level
H	H	No Current
L	H	Low Current 1/3 I_o max
H	L	Medium Current 2/3 I_o max
L	L	Maximum Current I_o max

Phase

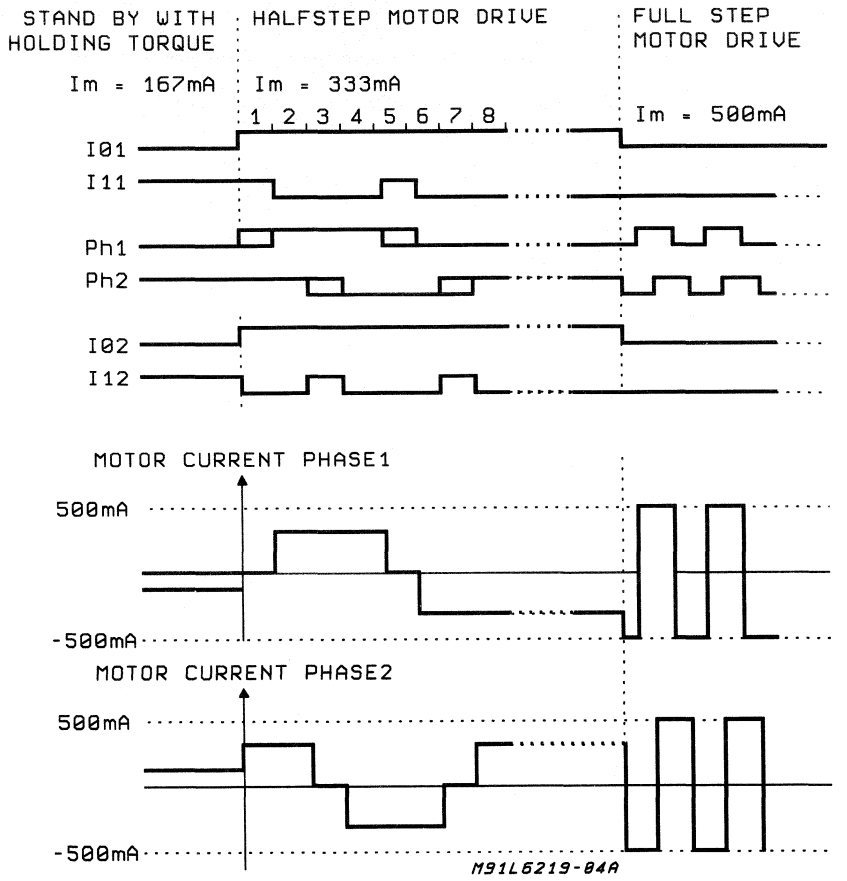
This input determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift.
High level on the PHASE input causes the motor current flow from Out A through the winding to Out B

Current Sensor

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators.
Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_o and I_1.
The motor current flows through the sensing resistor R_S.
When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator goes high, which triggers the pulse generator.
The max peak current I_{max} can be defined by:

$$I_{max} = \frac{V_{ref}}{10\ R_s}$$

Figure 2: Principle Operating Sequence



Single-pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off} , which is determined by the time components R_t and C_t.

$$t_{off} = 1.1 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.
If a new trigger signal should occur during t_{off}, it is ignored.

Output Stage

The output stage contains four Darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.
The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.
It should be noted however, that is not permitted to short circuit the outputs.
Internal circuitry is added in order to increse the accuracy of the motor current particularly with low current levels.

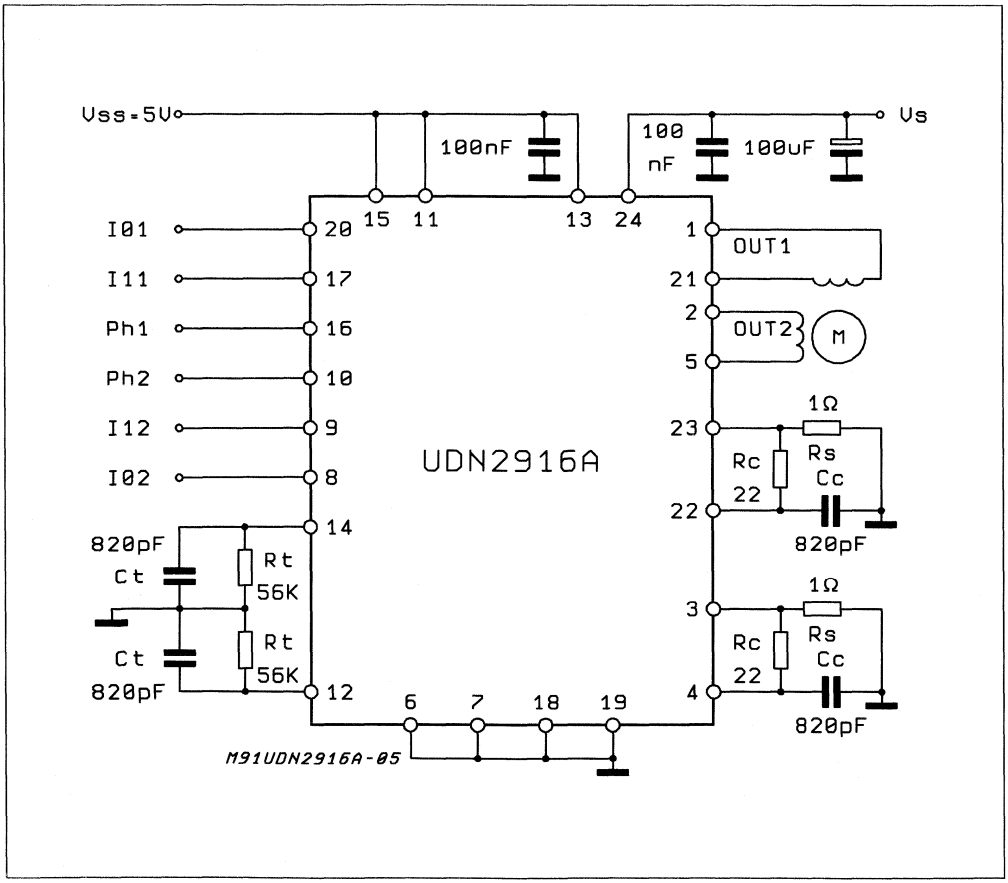
V_S, V_{SS}, V_{Ref}
The circuit will stand any order of turn-on or turn-off the supply voltages V_S and V_{SS}. Normal dV/dt values are then assumed.
Preferably, V_{Ref} should be tracking V_{SS} during power-on and power-off if V_S is established.

APPLICATION INFORMATIONS (Note 1)
Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.
Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.
Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100nF capacitor, located near the package between power line and ground.
The ground lead between R_S, and circuit GND should be kept as short as possible.
A typical Application Circuit is shown in Fig. 3.
Note that C_t must be NPO type or similar else.
To sense the winding current, paralleled metal film resistors are recommended (R_S)

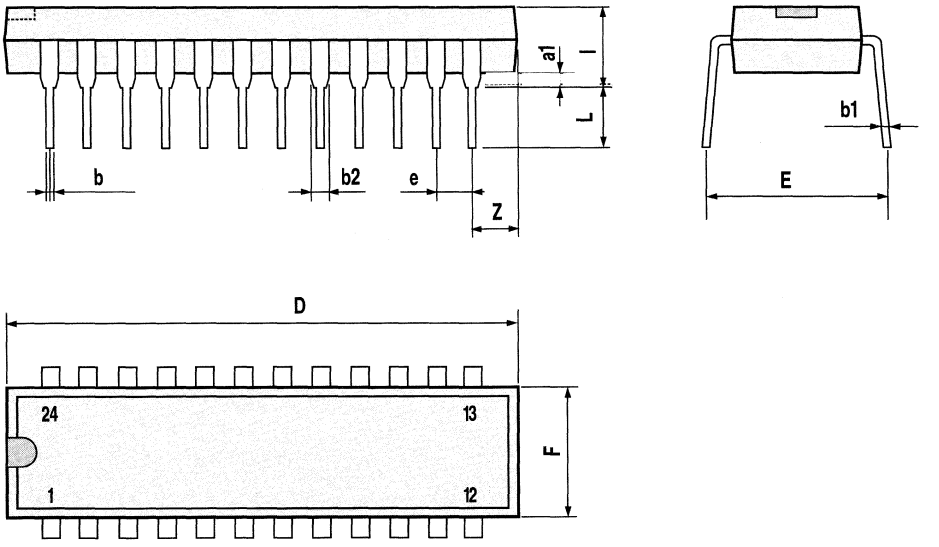
Note 1 - Other information is available as "Smart Power Development System": HWPC2916A.

Figure 3: Typical Application Circuit.



DIP24 (20+2+2) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.38			0.015		
b	0.41		0.51	0.016		0.020
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	1.40	1.52	1.65	0.055	0.060	0.065
D			30.23			1.19
E		7.62			0.300	
e		2.54			0.100	
F			6.86			0.270
I			4.32			0.170
L	3.18			0.125		



SGS-THOMSON MICROELECTRONICS

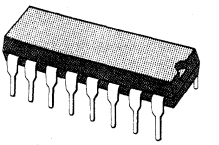
ULN2001A-ULN2003A
ULN2002A-ULN2004A

SEVEN DARLINGTON ARRAYS

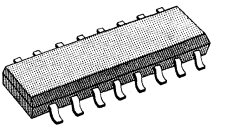
- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

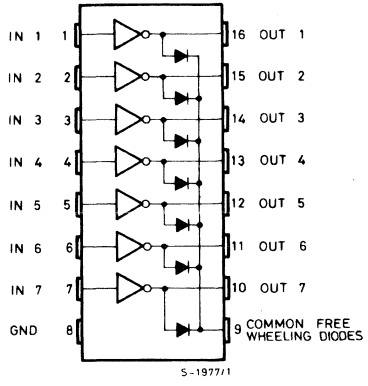
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL, CMOS
ULN2004A	6–15 V CMOS, PMOS

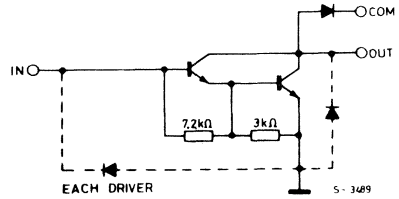
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

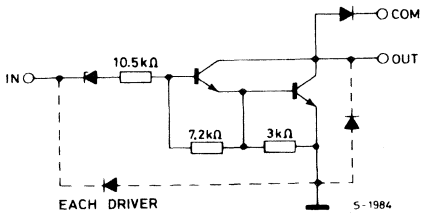
PIN CONNECTION



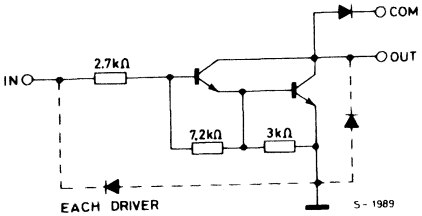
SCHEMATIC DIAGRAM



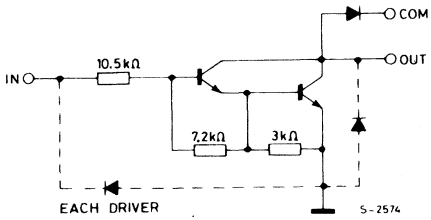
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2002A** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2004A** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULN2002A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2002A**					
		V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2003A**					
		V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULN2004A**					
		V_{CE} = 2 V I_C = 125 mA			5	V	5
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULN2001A** V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

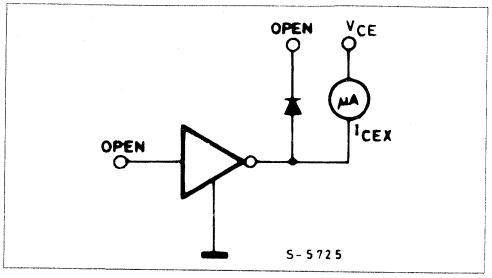


Figure 1b.

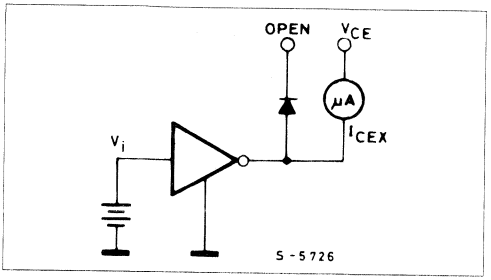


Figure 2.

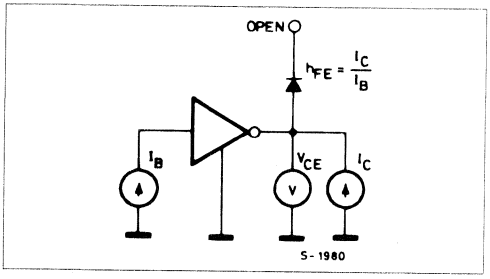


Figure 3.

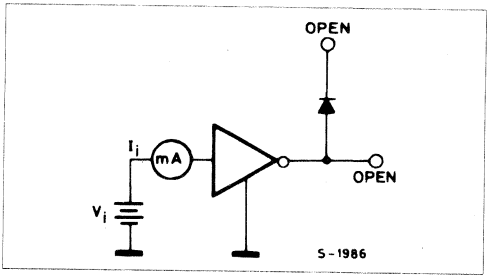


Figure 4.

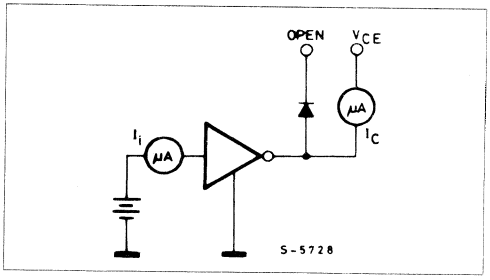


Figure 5.

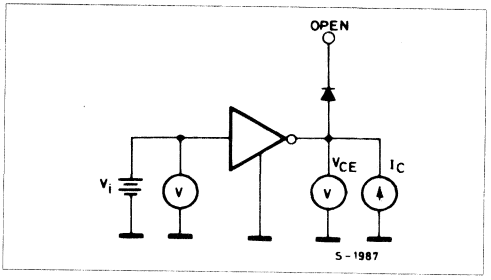


Figure 6.

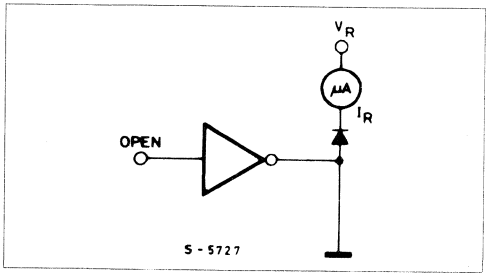
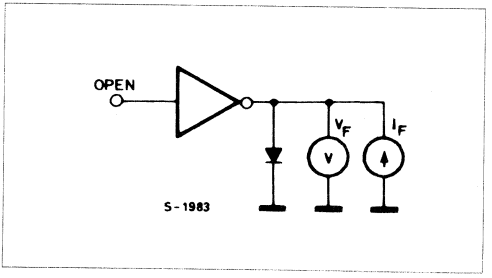


Figure 7.

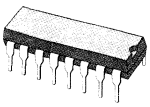


50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

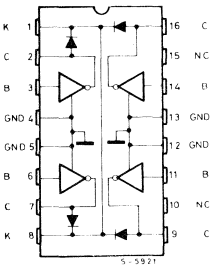
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

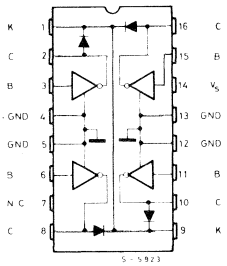


POWERDIP
12 + 2 + 2

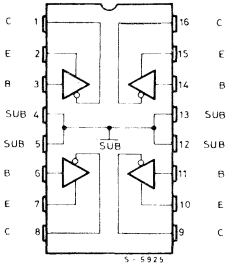
PIN CONNECTIONS (top view) and ORDER CODES



ULN2064B
ULN2068B



ULN2068B
ULN2070B

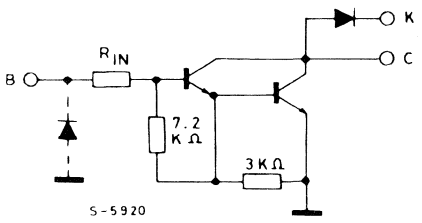


ULN2074B
ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_i	Input Voltage for **ULN2066B/70B/74B/76B** for **ULN2064B/68B**	30 15	V V
I_i	Input Current	25	mA
V_s	Supply Voltage for **ULN2068B** for **ULN2070B**	10 20	V V
P_{tot}	Power Dissipation : at T_{amb} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



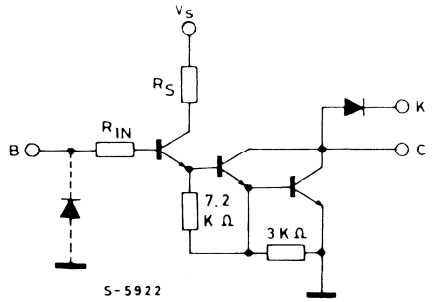
ULN2064B : R_{IN} = 35 Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2064B – ULN2066B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2064B – ULN2066B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2064B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2064B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2066B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2066B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2064B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2066B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn – on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn – off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2064B – ULN2066B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

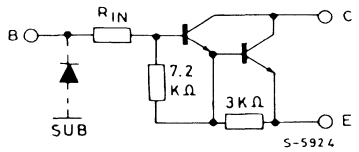


ULN2068B : R_{IN} = 2.5 kΩ R_s = 900 Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2068B, V_s = 12 V for ULN2070B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2068B – ULN2070B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2068B – ULN2070B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2068B**					2
		I_C = 500 mA V_i = 2.75 V			1.1	V	
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		for **ULN2070B**					
		I_B = 500 mA V_i = 5 V			1.1	V	
		I_B = 750 mA V_i = 5 V			1.2	V	
		I_B = 1 A V_i = 5 V			1.3	V	
		I_B = 1.25 A V_i = 5 V			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2068B** V_i = 2.75 V			550	µA	4
		for **ULN2068B** V_i = 3.75 V			1000	µA	
		for **ULN2070B** V_i = 5 V			400	µA	
		for **ULN2070B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					5
		for **ULN2068B**			2.75	V	
		for **ULN2070B**			5	V	
I_s	Supply Current	for **ULN2068B**					8
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2070B**					
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2068B – ULN2070B**					6
		V_R = 50 V			50	µA	
		V_R = 50 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2074B : R_{IN} = 350 Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2074B – ULN2076B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2074B – ULN2076B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2074B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2074B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2076B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2076B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2074B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2076B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

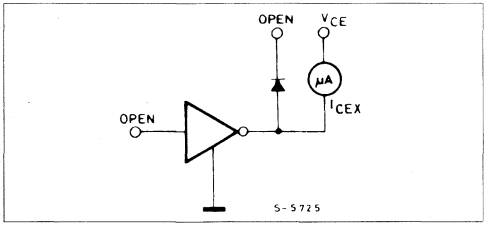


Figure 2.

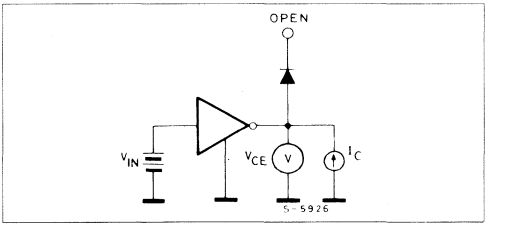


Figure 3.

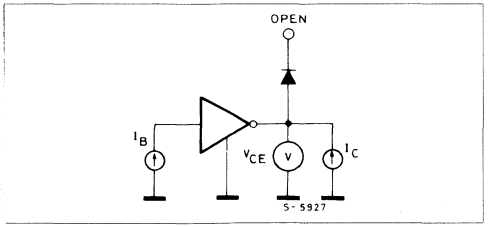


Figure 4.

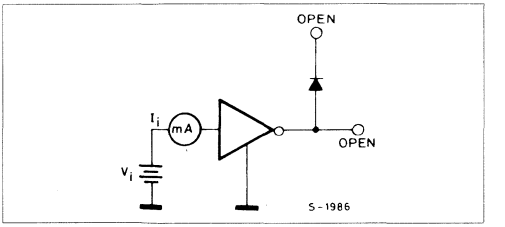


Figure 5.

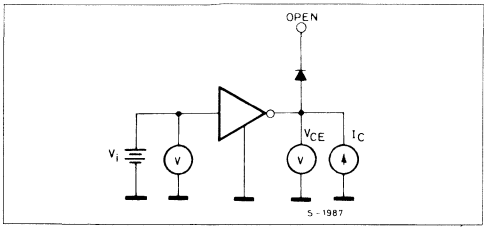


Figure 6.

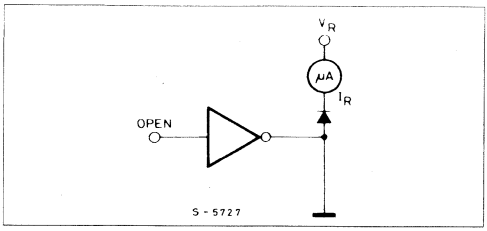


Figure 7.

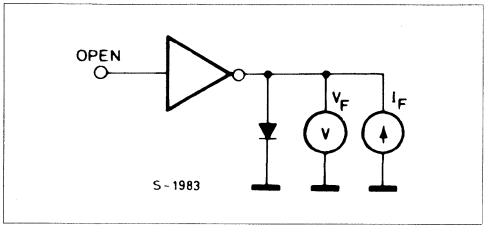


Figure 8.

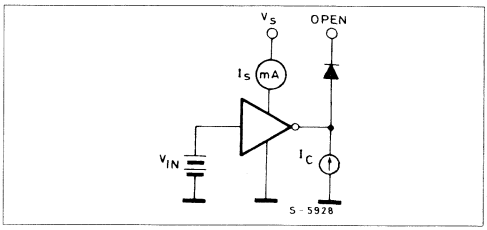


Figure 9 : Input Current as a Function of Input Voltage.

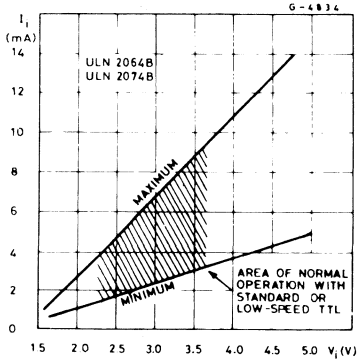


Figure 10 : Input Current as a Function of Input Voltage.

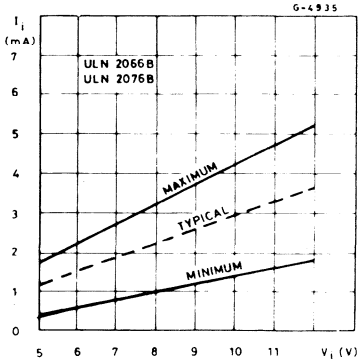
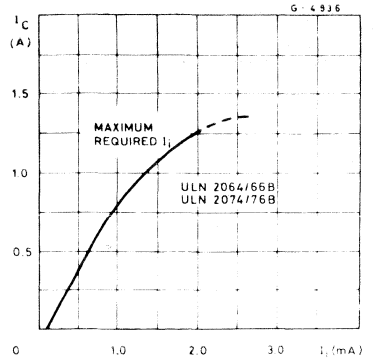


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

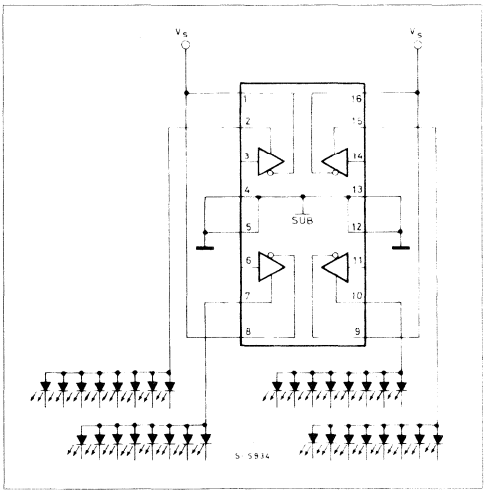
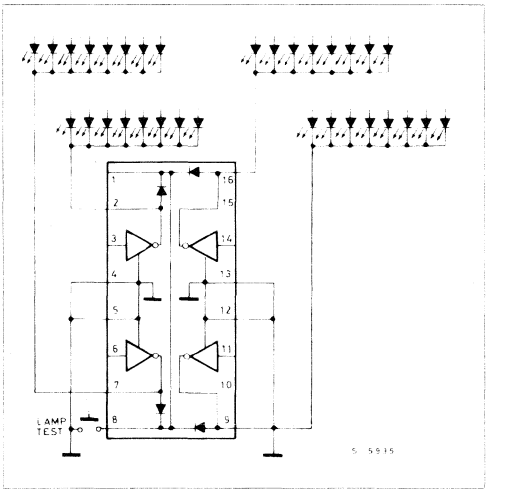


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

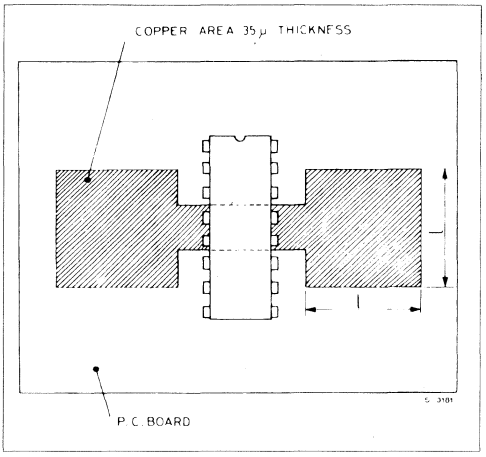


Figure 15 : External Heatsink Mounting Example.

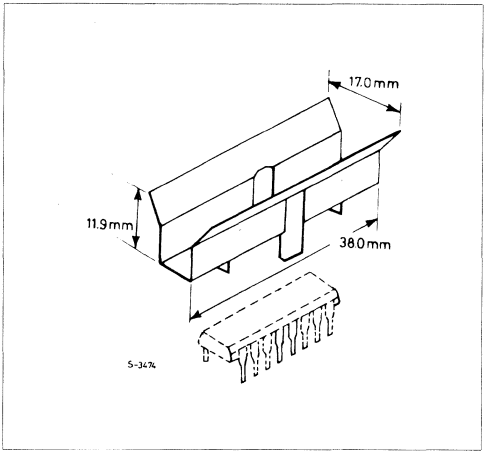


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

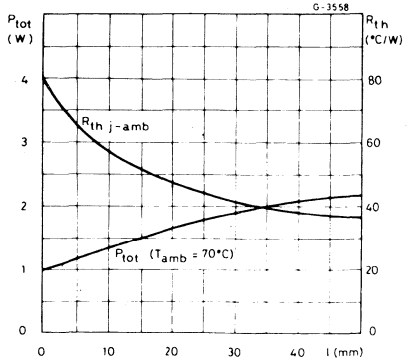
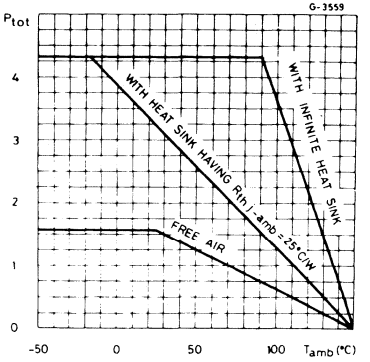


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



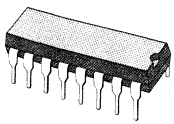
ULN2065B ULN2067B ULN2069B ULN2071B ULN2075B ULN2077B

80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

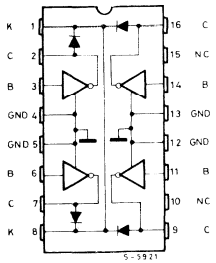
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

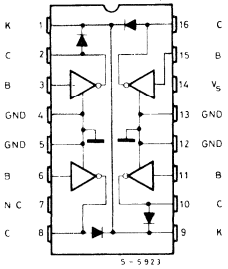


POWERDIP
12 + 2 + 2

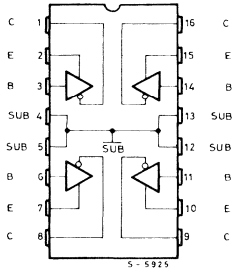
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



ULN2069B
ULN2071B

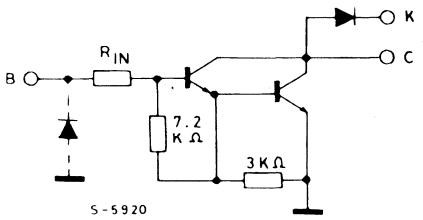


ULN2075B
ULN2077B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for **ULN2075B – 2077B** for **ULN2067B – 2071B** for **ULN2065B – 2069B**	60 30 15	V V V
I_I	Input Current	25	mA
V_S	Supply Voltage for **ULN2069B** for **ULN2071B**	10 20	V V
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



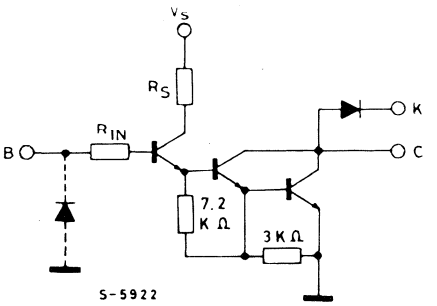
ULN2065B : R_{IN} = 350 Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2065B – ULN2067B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2065B – ULN2067B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2065B – ULN2067B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2065B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2065B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2067B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2067B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2065B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2067B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2065B – ULN2067B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

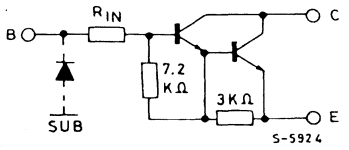


ULN2069B : R_{IN} = 2.5 KΩ, R_s = 900 Ω
ULN2071B : R_{IN} = 11.6 KΩ, R_s = 3.4 KΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2069B, V_s = 12 V for ULN2071B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2069B – ULN2071B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2069B – ULN2071B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2069B**					
		I_C = 500 mA V_i = 2.75 V			1.1	V	2
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		I_C = 1.5 A V_i = 2.75 V			1.5	V	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			1.1	V	
		I_C = 750 mA V_i = 5 V			1.2	V	
		I_C = 1 A V_i = 5 V			1.3	V	
		I_C = 1.25 A V_i = 5 V			1.4	V	
		I_C = 1.5 A V_i = 5 V			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2069B** V_i = 2.75 V			550	µA	4
		for **ULN2069B** V_i = 3.75 V			1000	µA	
		for **ULN2071B** V_i = 5 V			400	µA	
		for **ULN2071B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					5
		for **ULN2069B**			2.75	V	
		for **ULN2071B**			5		
I_s	Supply Current	for **ULN2069B**					8
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2069B – ULN2071B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350 Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2075B – ULN2077B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2075B – ULN2077B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2075B – ULN2077B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2075B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2075B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2077B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2077B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2075B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2077B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

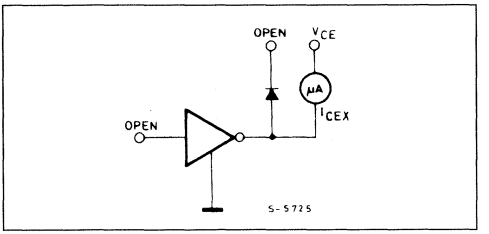
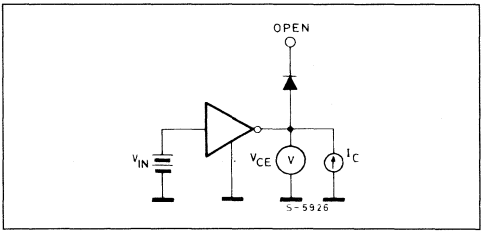


Figure 2.



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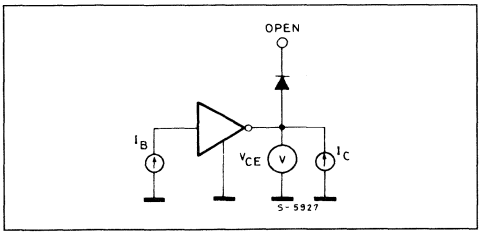

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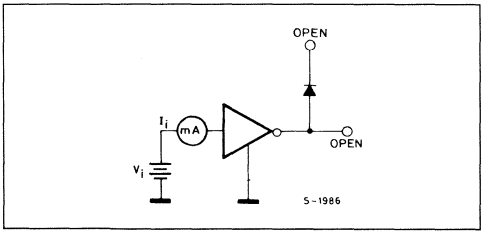


Figure 5.

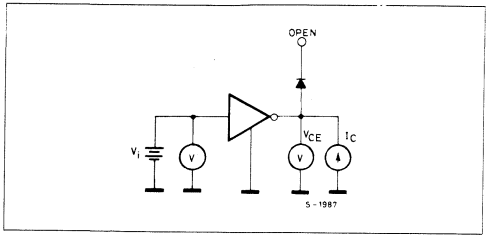


Figure 6.

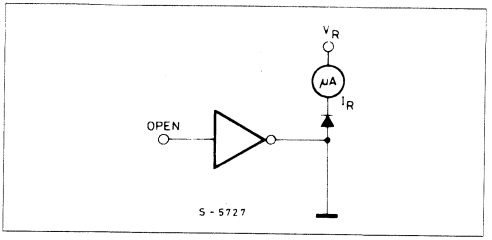


Figure 7.

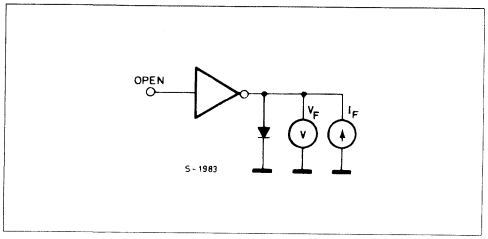


Figure 8.

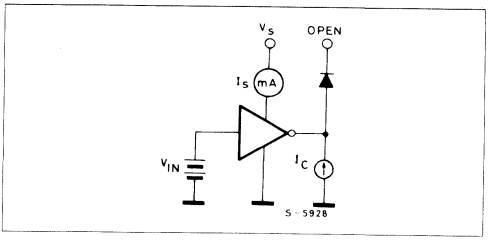


Figure 9 : Input Current as a Function of Input Voltage.

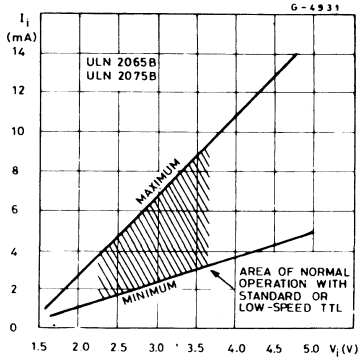


Figure 10 : Input Current as a Function of Input Voltage.

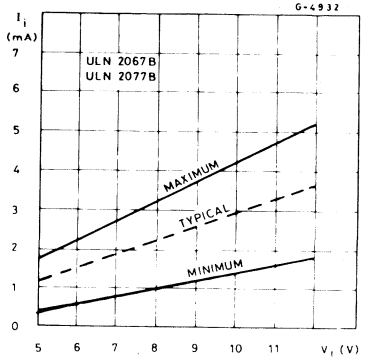
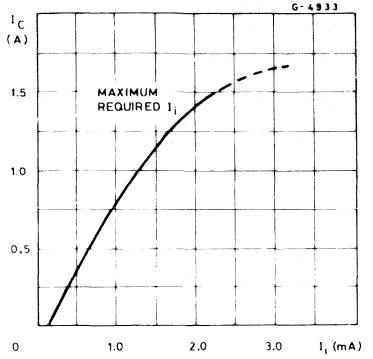


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

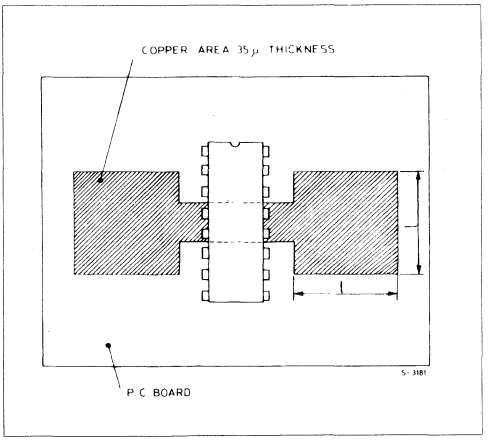


Figure 13 : External Heatsink Mounting Example.

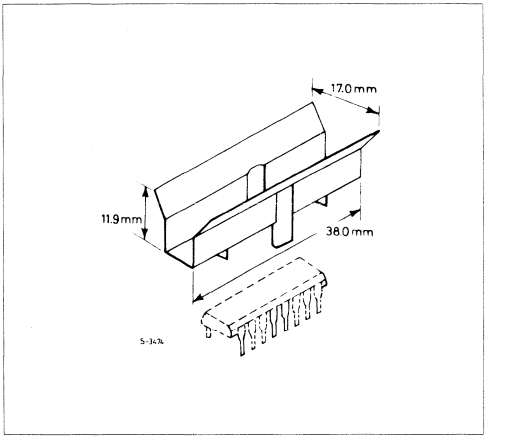


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

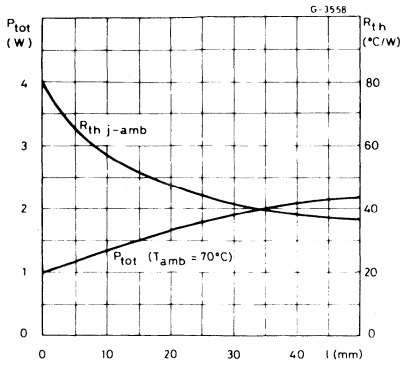
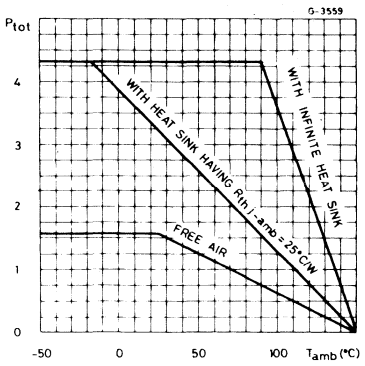


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



ULN2801A
ULN2802A ULN2803A
ULN2804A ULN2805A

EIGHT DARLINGTON ARRAYS

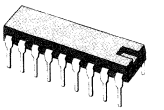
- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

DESCRIPTION

The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

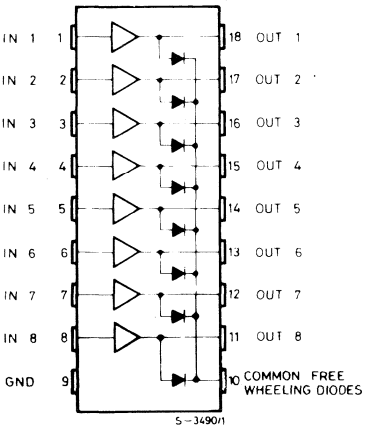
Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULN2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULN2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.



DIP-18
(Plastic)

CONNECTION DIAGRAM (top view)

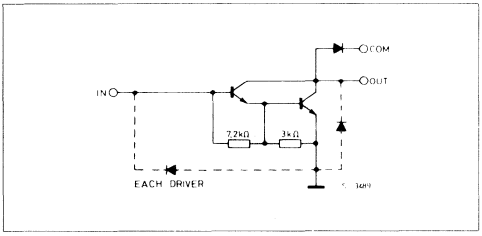


ABSOLUTE MAXIMUM RATINGS

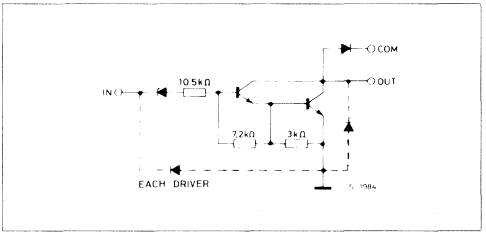
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, 2803A, 2804A for ULN2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

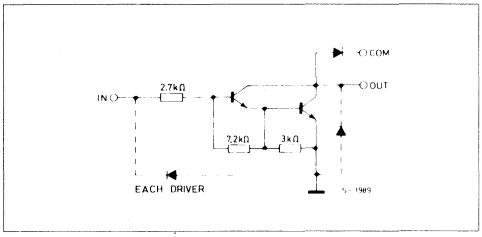
For ULN2801A (each driver for PMOS-CMOS)



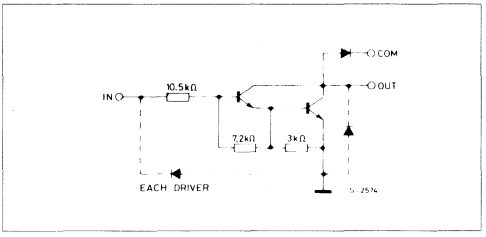
For ULN2802A (each driver for 14-15 V PMOS)



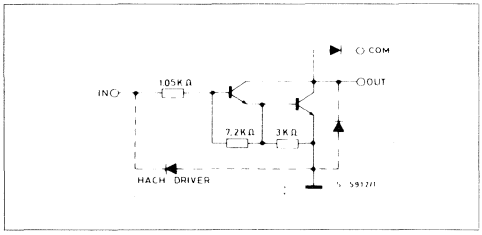
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2802A** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2804A** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULN2802A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2803A** V_i = 3.85 V		0.93	1.35	mA	
		for **ULN2804A** V_i = 5 V		0.35	0.5	mA	
		V_i = 12 V		1	1.45	mA	
		for **ULN2805A** V_i = 3 V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2802A** V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2803A** V_{CE} = 2 V I_C = 200 mA			2.4	V	
		V_{CE} = 2 V I_C = 250 mA			2.7	V	
		V_{CE} = 2 V I_C = 300 mA			3	V	
		for **ULN2804A** V_{CE} = 2 V I_C = 125 mA			5	V	
		V_{CE} = 2 V I_C = 200 mA			6	V	
		V_{CE} = 2 V I_C = 275 mA			7	V	
		V_{CE} = 2 V I_C = 350 mA			8	V	
		for **ULN2805A** V_{CE} = 2 V I_C = 350 mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULN2801A** V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

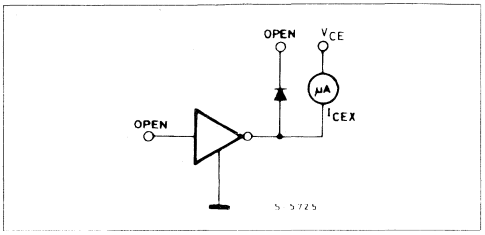


Figure 1b.

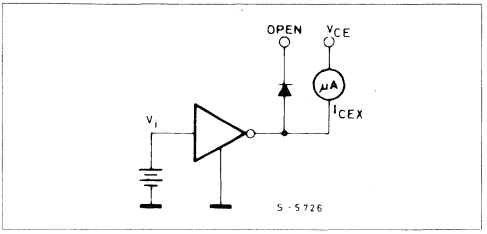


Figure 2.

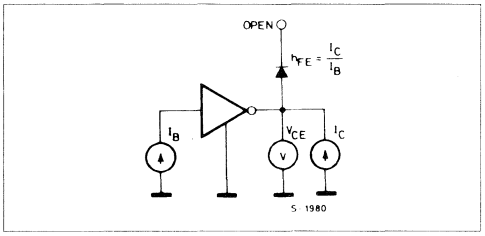


Figure 3.

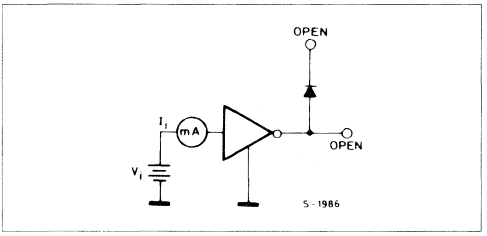


Figure 4.

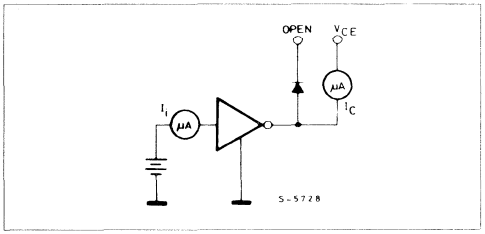


Figure 5.

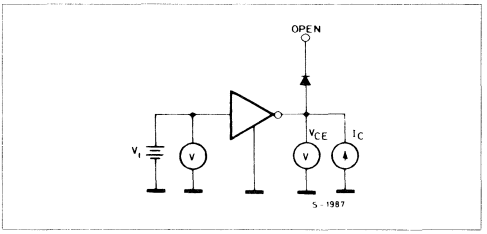


Figure 6.

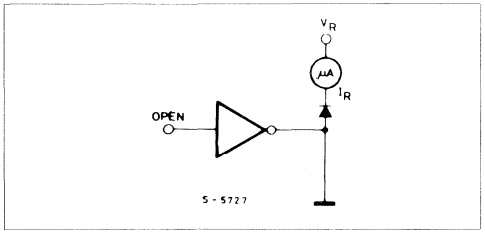


Figure 7.

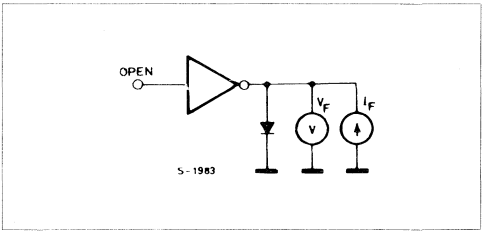


Figure 8 : Collector Current as a Function of Saturation Voltage.

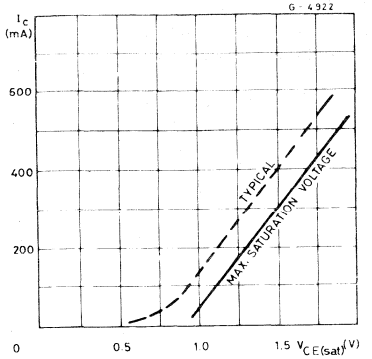


Figure 9 : Collector Current as a Function of Input Current.

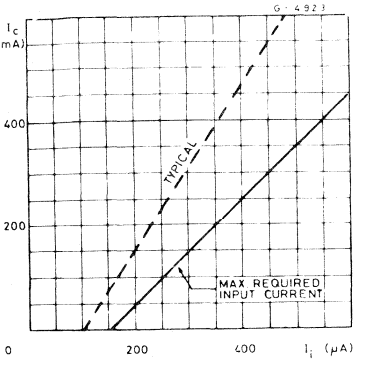


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

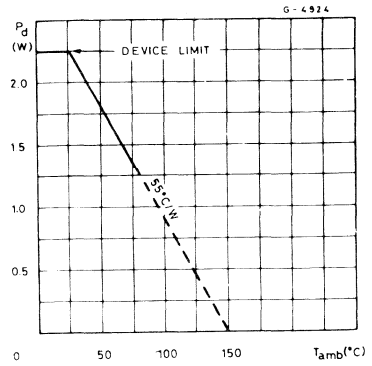


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

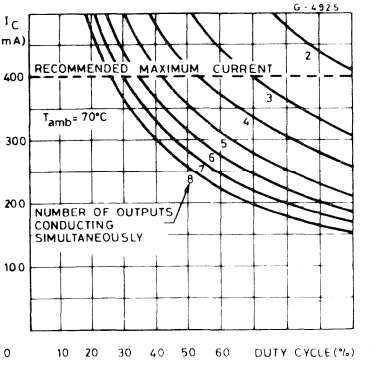


Figure 12 : Peak Collector Current as a Function of Duty.

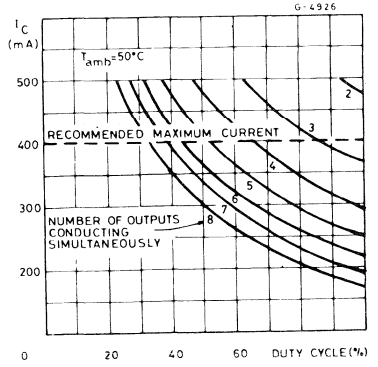


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

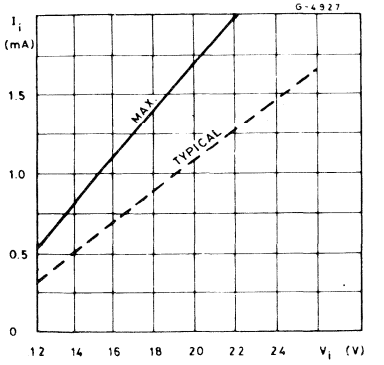


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

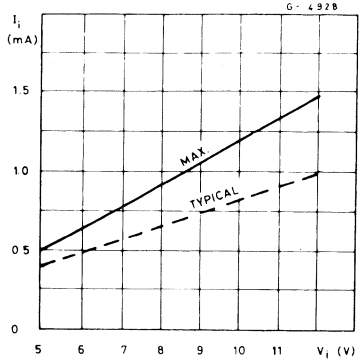


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

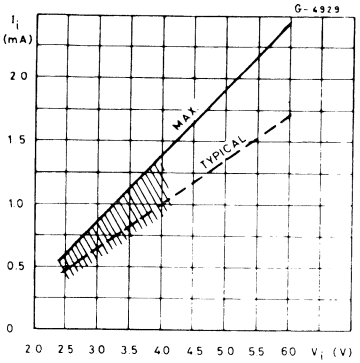
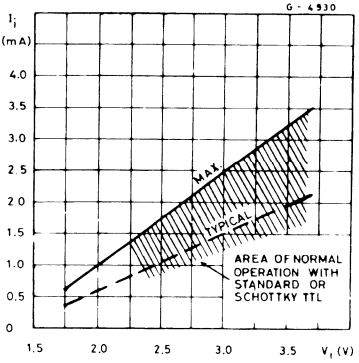


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)



SGS-THOMSON MICROELECTRONICS

ULQ2001A-ULQ2003A
ULQ2002A-ULQ2004A

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- **EXTENDED TEMPERATURE RANGE (–40 to 105°C)**
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

DESCRIPTION

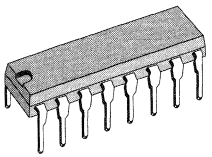
The ULQ2001A, ULQ2002A, ULQ2003 and ULQ2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families :

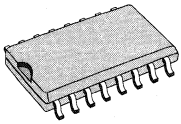
ULQ2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULQ2002A	14-25 V PMOS
ULQ2003A	5 V TTL, CMOS
ULQ2004A	6–15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC mo-tors, LED displays filament lamps, thermal printheads and high power buffers.

The ULQ2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULQ2001D1/2002D1/2003D1/2004D1.



DIP16



SO16

ORDERING NUMBERS:

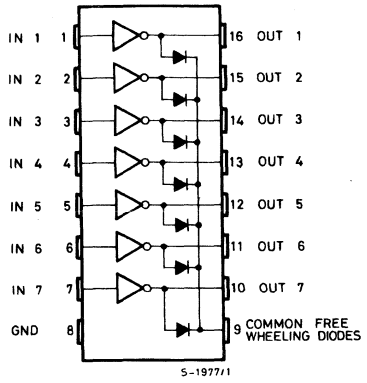
ULQ2001A/2A/3A/4A (DIP-16)

ULQ2001D1/2D1/3D1/4D1 (SO-16)

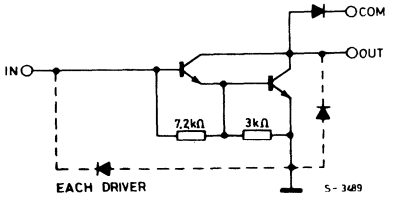
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULQ2002A/D1 - 2003A/D1 - 2004A/D1)	30	V
I_c	Continuous Colletor Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	–40 to 105	°C
T_{stg}	Storage Temperature Range	–55 to 150	°C
T_j	Junction Temperature	150	°C

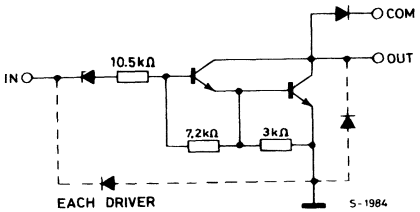
PIN CONNECTION



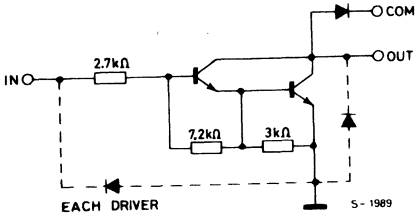
SCHEMATIC DIAGRAM



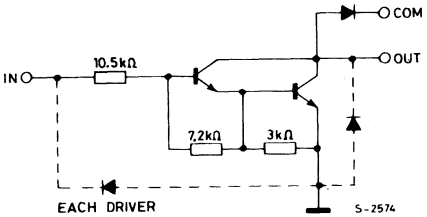
Series ULQ-2001A
(each driver)



Series ULQ-2002A
(each driver)



Series ULQ-2003A
(each driver)



Series ULQ-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_J = –40 to 105 °C for DIP16 unless otherwise specified)
(T_J = 25 to 105 °C for SO16 unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V				50	µA	1a
		T_J = 105 °C	V_{CE} = 50 V			100	µA	1a
		T_J = 105 °C for **ULQ2002A**						
		V_{CE} = 50 V for **ULQ2004A**	V_i = 6 V			500	µA	1b
		V_{CE} = 50 V	V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA	I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA	I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA	I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULQ2002A**	V_i = 17 V		0.82	1.25	mA	3
		for **ULQ2003A**	V_i = 3.85 V		0.93	1.35	mA	3
		for **ULQ2004A**	V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V			1	1.45	mA	3
$I_{i(off)}$	Input Current	T_J = 105 °C	I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULQ2002A**						
		V_{CE} = 2 V	I_C = 300 mA			13	V	5
		for **ULQ2003A**						
		V_{CE} = 2 V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V	I_C = 300 mA			3	V	5
		for **ULQ2004A**						
		V_{CE} = 2 V	I_C = 125 mA			5	V	5
		V_{CE} = 2 V	I_C = 200 mA			6	V	5
		V_{CE} = 2 V	I_C = 275 mA			7	V	5
		V_{CE} = 2 V	I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULQ2001A**						
		V_{CE} = 2 V	I_C = 350 mA	1000			–	2
C_i	Input Capacitance				15	25 (*)	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			0.25	1 (*)	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			0.25	1 (*)	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V				50	µA	6
		T_J = 105 °C	V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA			1.7	2	V	7

(*) GUARANTEED BY DESIGN.

TEST CIRCUITS

Figure 1a.

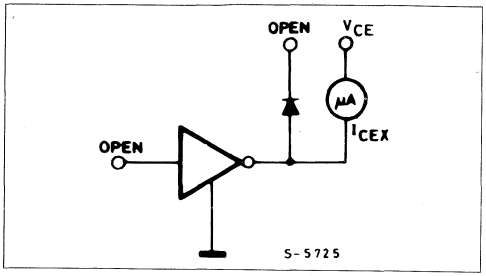


Figure 1b.

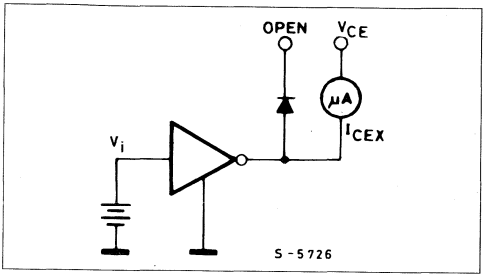


Figure 2.

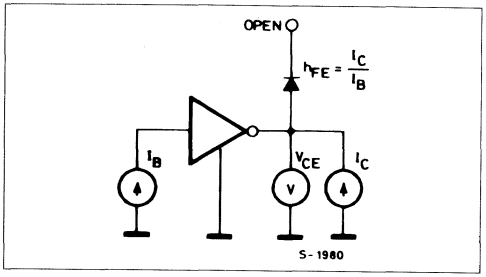


Figure 3.

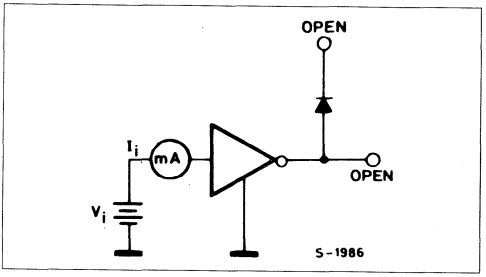


Figure 4.

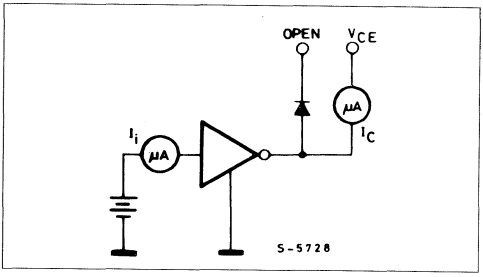


Figure 5.

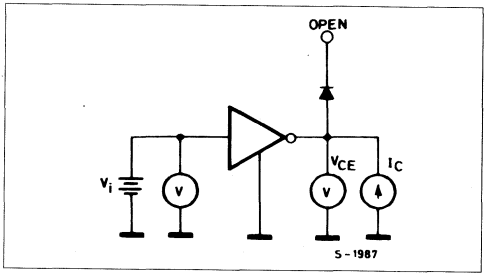


Figure 6.

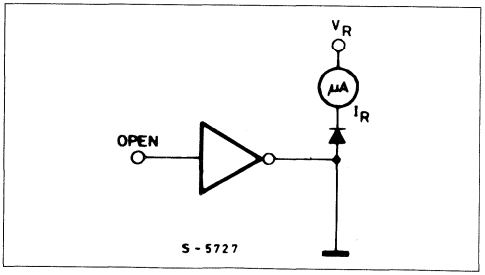
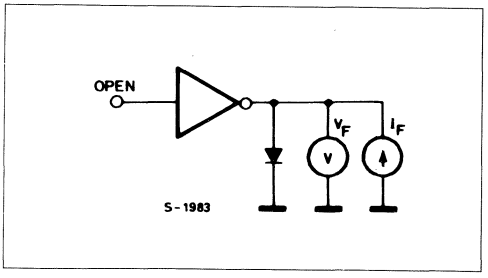


Figure 7.

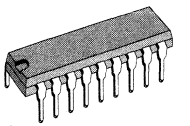


SGS-THOMSON MICROELECTRONICS

ULQ2801A ULQ2802A ULQ2803A ULQ2804A ULQ2805A

EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- **EXTENDED TEMPERATURE RANGE (– 40 to 105°C)**
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



DIP-18

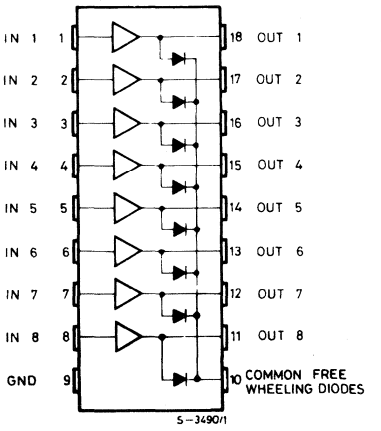
DESCRIPTION

The ULQ2801A-ULQ2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULQ2801A is designed for general purpose applications with a current limit resistor ; the ULQ2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULQ2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULQ2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULQ2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead frame and feature the convenient input-opposite-output pinout to simplify board layout.

PIN CONNECTION (top view)

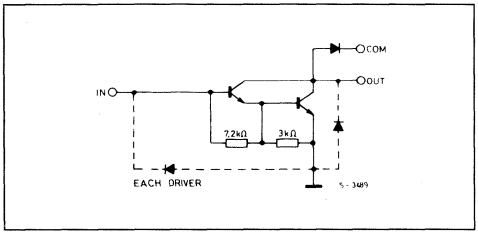


ABSOLUTE MAXIMUM RATINGS

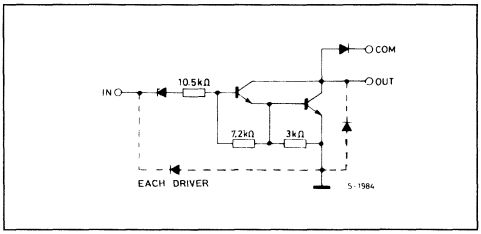
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULQ2802A, 2803A, 2804A for ULQ2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 40 to 105	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

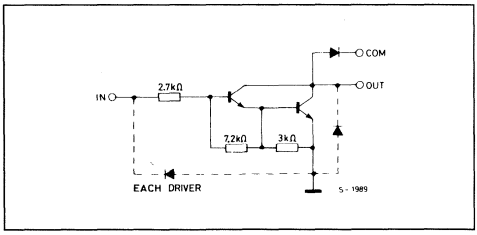
For ULQ2801A (each driver for PMOS-CMOS)



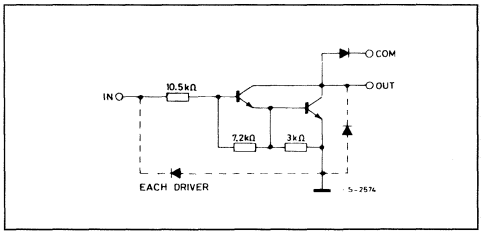
For ULQ2802A (each driver for 14-15 V PMOS)



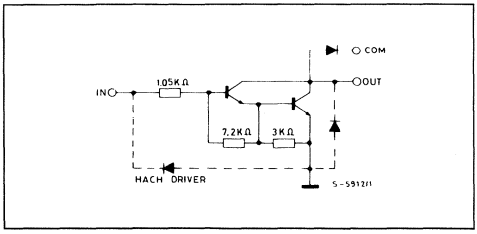
For ULQ2803A (each driver for 5 V, TTL/CMOS)



For ULQ2804A (each driver for 6-15 V CMOS/PMOS



For ULQ2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (Tj = –40 to 105°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V			50	µA	1a
		T_J = 105°C V_{CE} = 50V			100	µA	1a
		T_J = 105°C					
		for **ULQ2802A**					
		V_{CE} = 50V V_i = 6V			500	µA	1b
		for **ULQ2804A**					
		V_{CE} = 50V V_i = 1V			500	µA	1b
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA I_B = 250µA		0.9	1.1	V	
		I_C = 200mA I_B = 350µA		1.1	1.3	V	2
		I_C = 350mA I_B = 500µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULQ2802A** V_i = 17V		0.82	1.25	mA	
		for **ULQ2803A** V_i = 3.85V		0.93	1.35	mA	
		for **ULQ2804A** V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	
		for **ULQ2805A** V_i = 3V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_J = 105°C I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULQ2802A**					
		V_{CE} = 2V I_c = 300mA			13	V	
		for **ULQ2803A**					
		V_{CE} = 2V I_c = 200mA			2.4	V	
		V_{CE} = 2V I_c = 250mA			2.7	V	
		V_{CE} = 2V I_c = 300mA			3	V	
		for **ULQ2804A**					5
		V_{CE} = 2V I_c = 125mA			5	V	
		V_{CE} = 2V I_c = 200mA			6	V	
		V_{CE} = 2V I_c = 275mA			7	V	
		V_{CE} = 2V I_c = 350mA			8	V	
		for **ULQ2805A**					
		V_{CE} = 2V I_c = 350mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULQ2802A** V_{CE} = 2V I_c = 350mA	1000			–	2
C_i	Input Capacitance			15	25 (*)	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1 (*)	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50V			50	µA	6
		T_J = 105°C V_R = 50V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

(*) GUARANTEED BY DESIGN.

TEST CIRCUITS

Figure 1a.

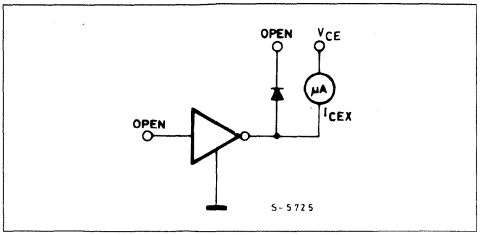


Figure 1b.

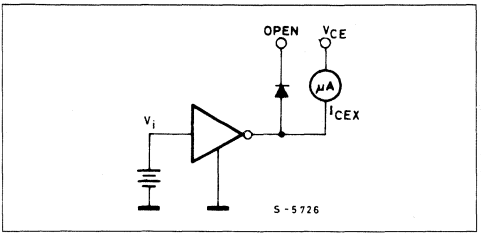


Figure 2.

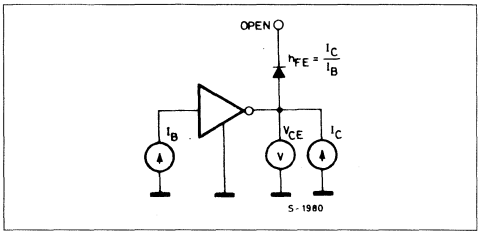


Figure 3.

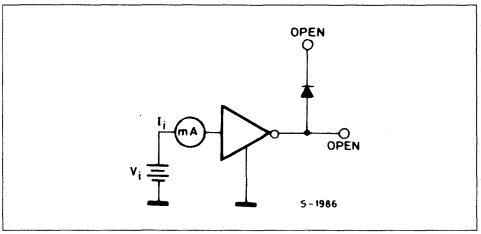


Figure 4.

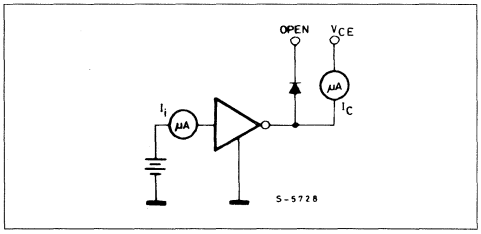


Figure 5.

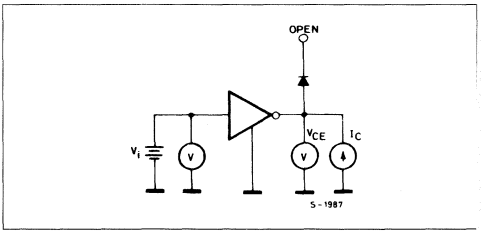


Figure 6.

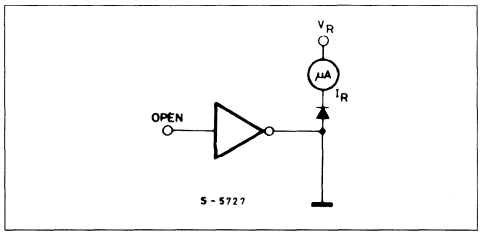


Figure 7.

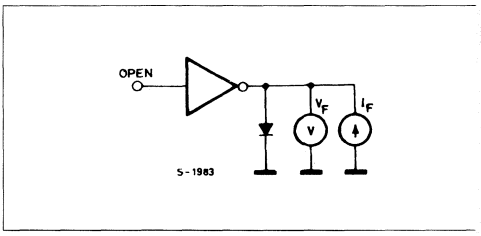


Figure 8 : Collector Current as a Function of Saturation Voltage.

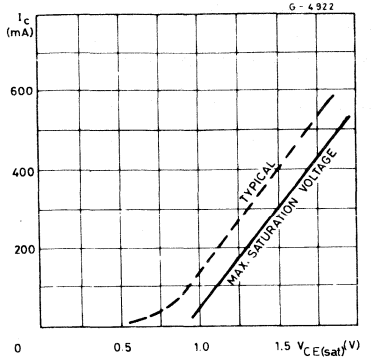


Figure 9 : Collector Current as a Function of Input Current.

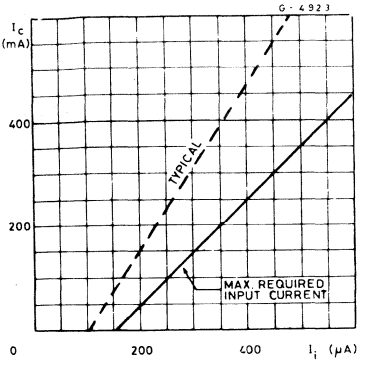


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

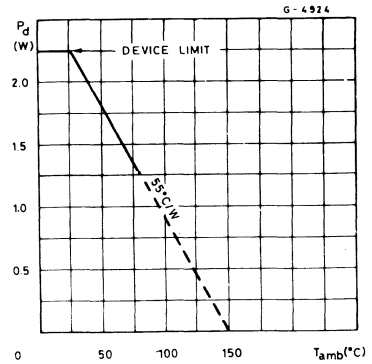


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

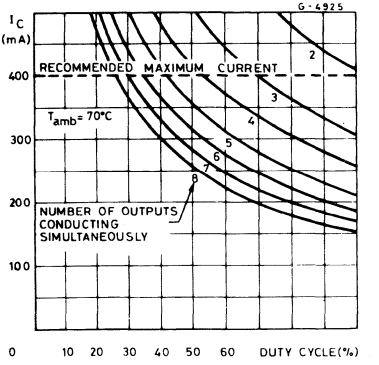


Figure 12 : Peak Collector Current as a Function of Duty.

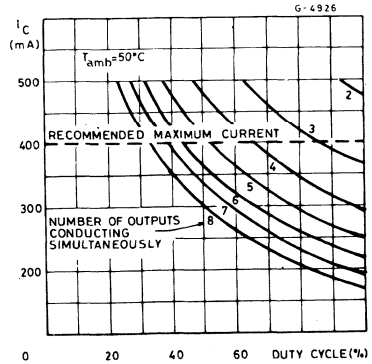


Figure 13 : Input Current as a Function of Input Voltage (for ULQ2802A).

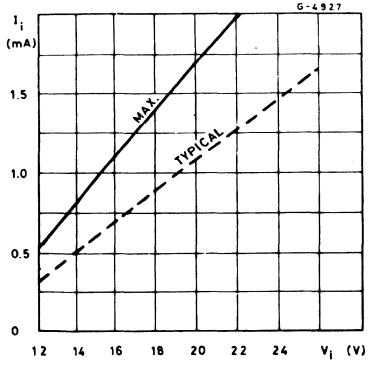


Figure 14 : Input Current as a Function of Input Voltage (for ULQ2804A)

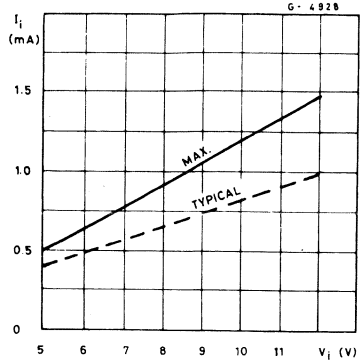


Figure 15 : Input Current as a Function of Input Voltage (for ULQ2803A)

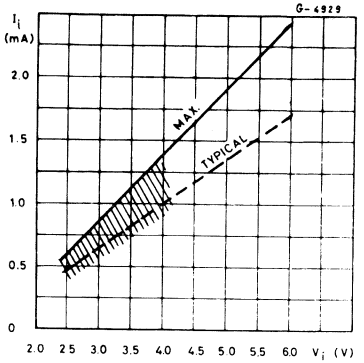
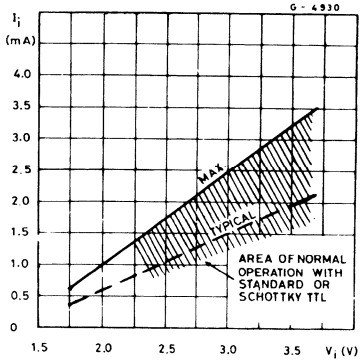


Figure 16 : Input Current as a Function of Input Voltage (for ULQ2805A)

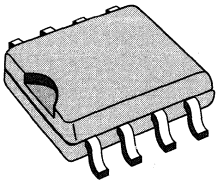


PACKAGES
INTEGRATED CIRCUITS

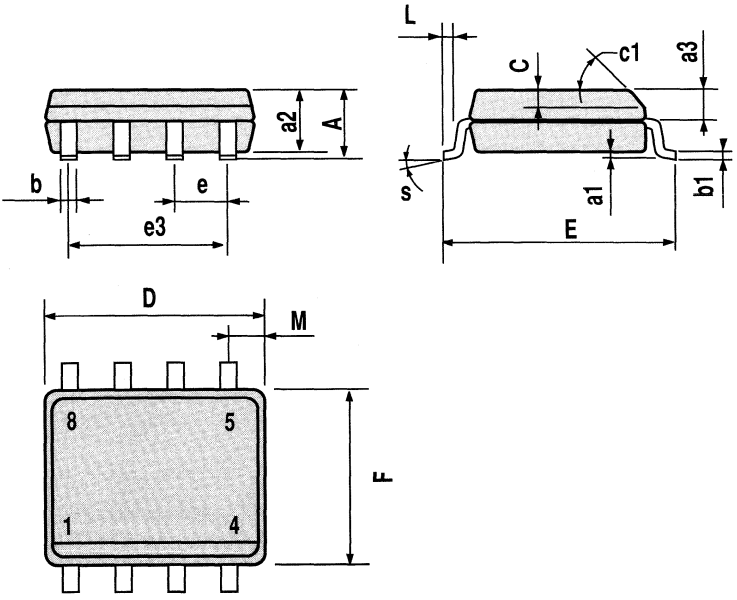
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

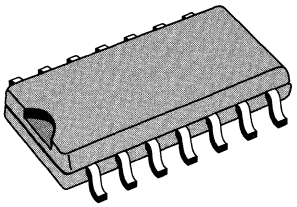


P013M

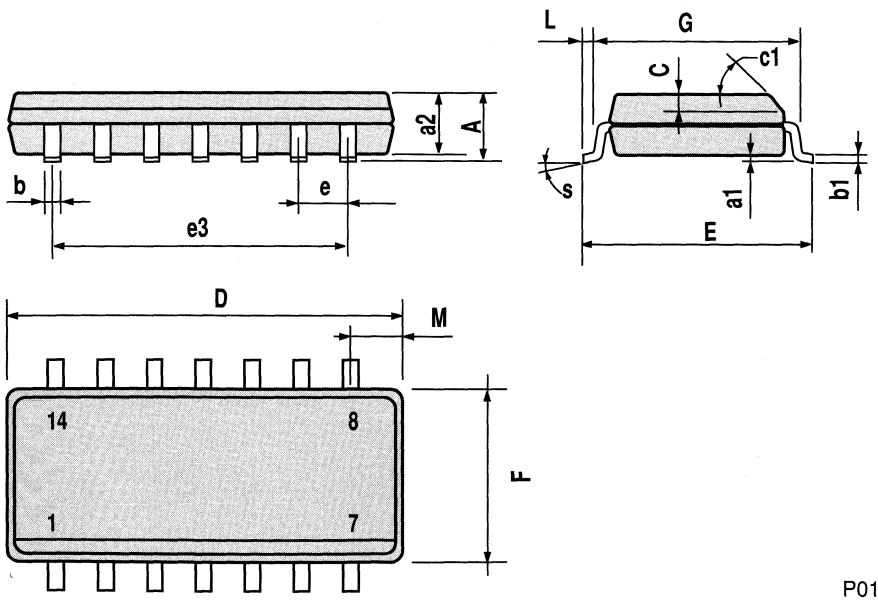
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO14

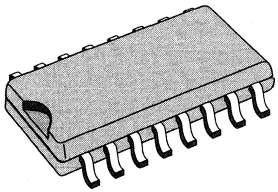


P013G

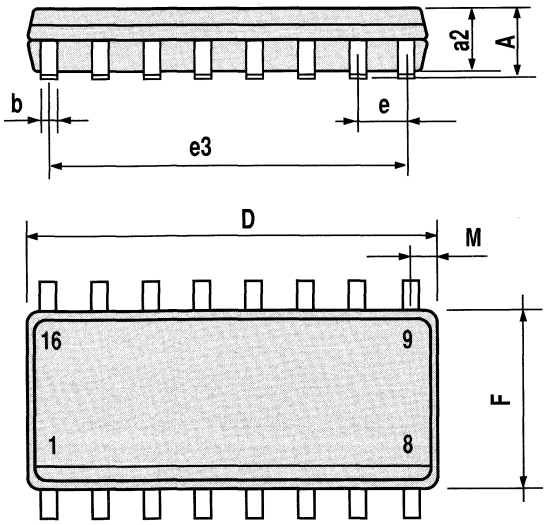
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16

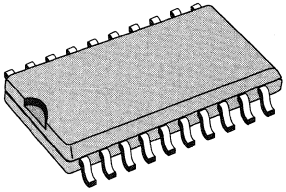


P013H

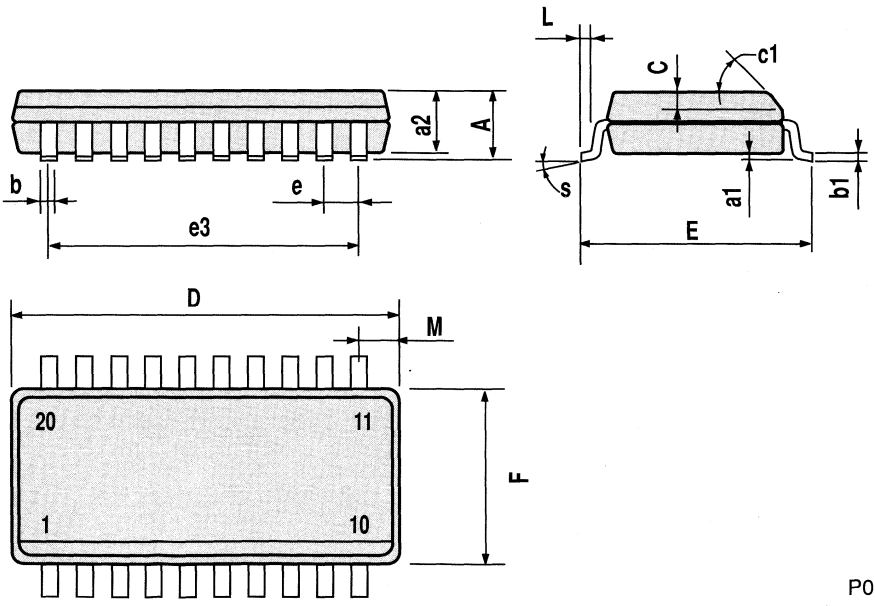
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

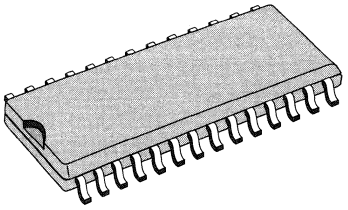


P013L

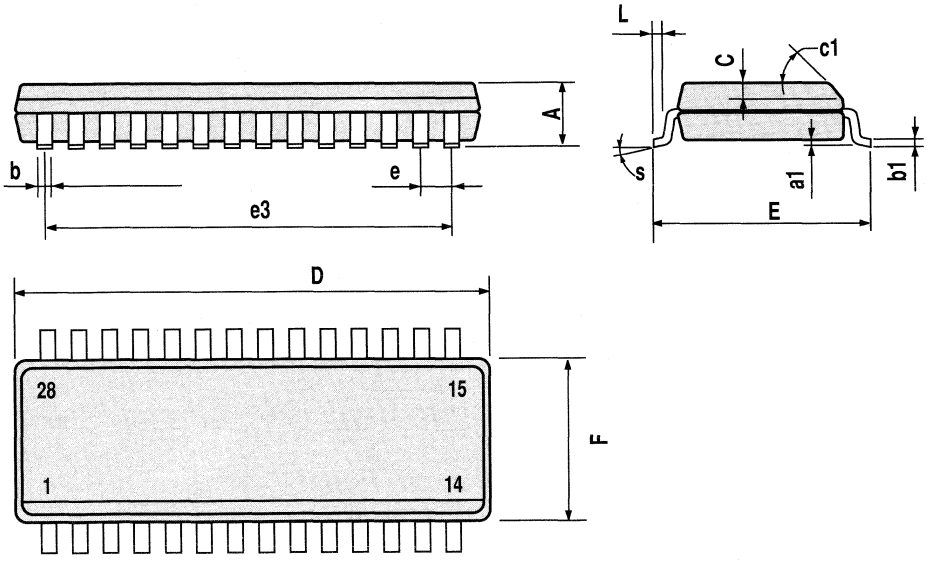
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28

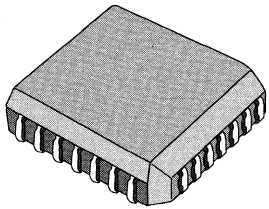


P013N

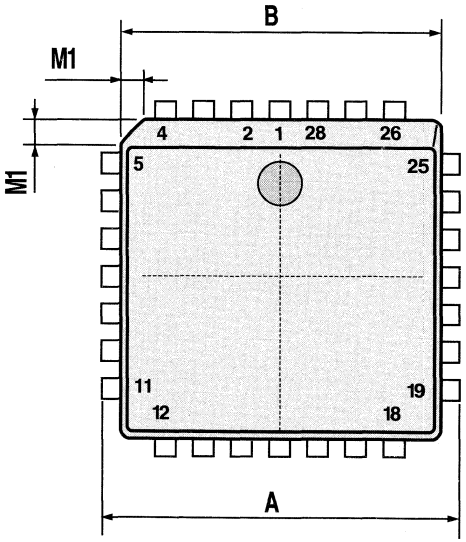
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC28

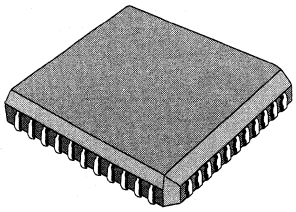


P027E

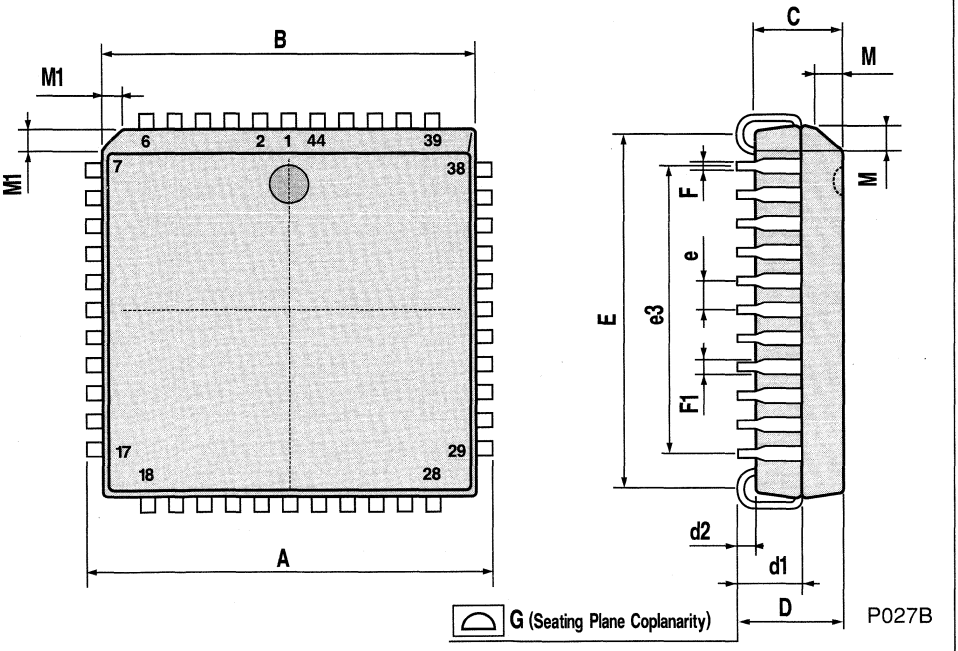
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



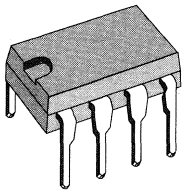
PLCC44



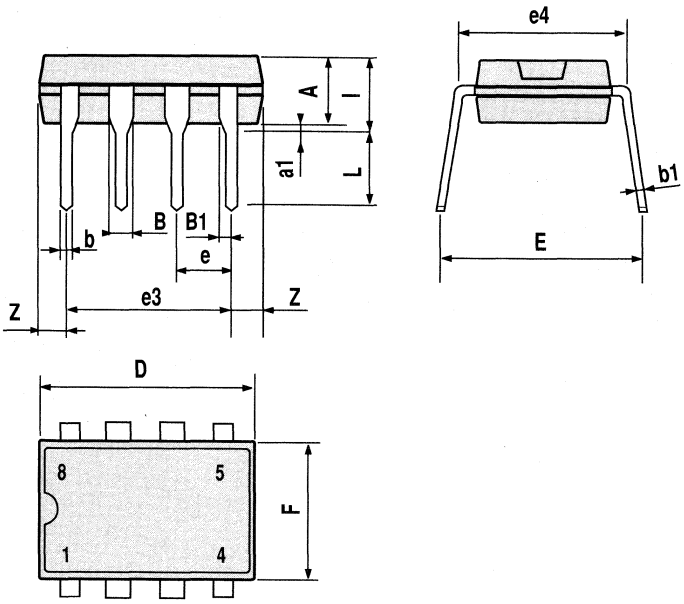
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.25)

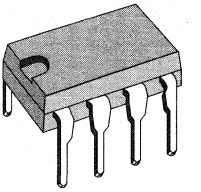


P001W

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



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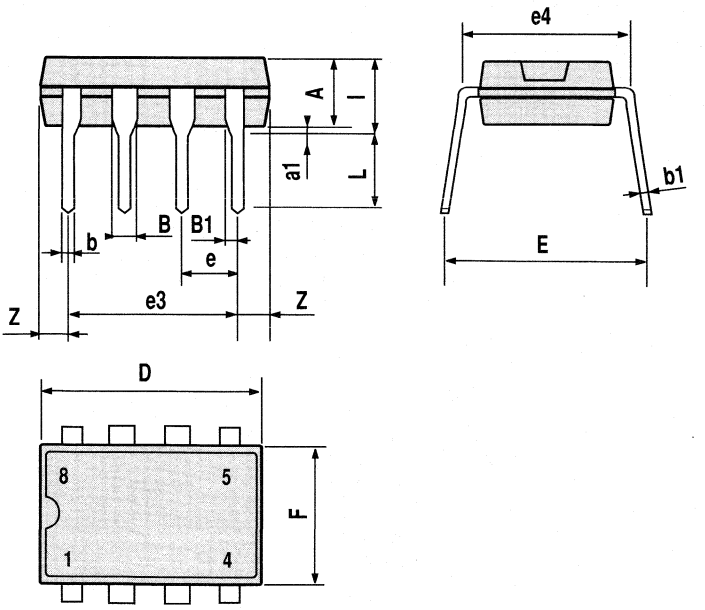
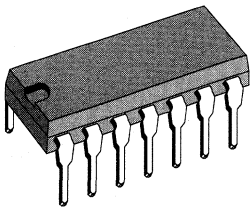


P001F

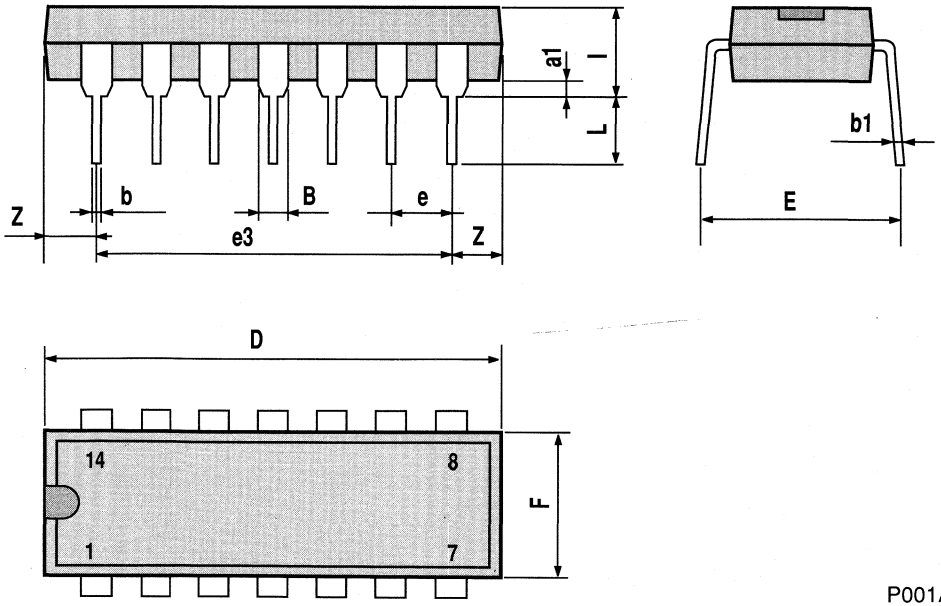
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP14

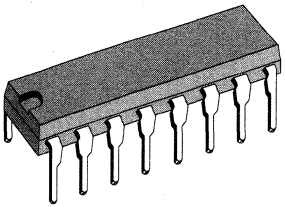


P001A

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



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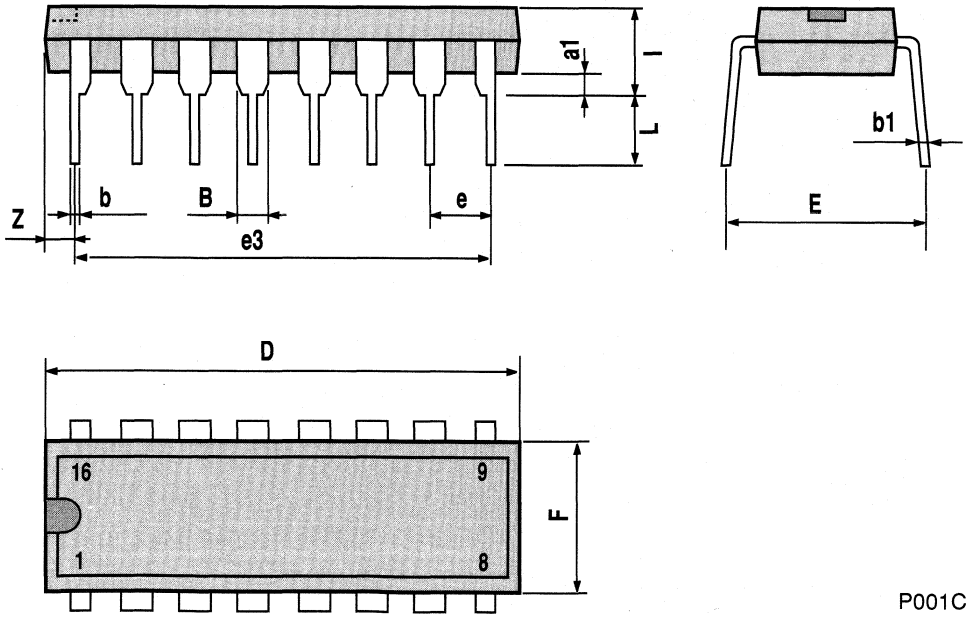
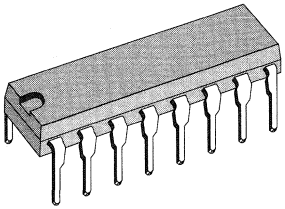


P001C

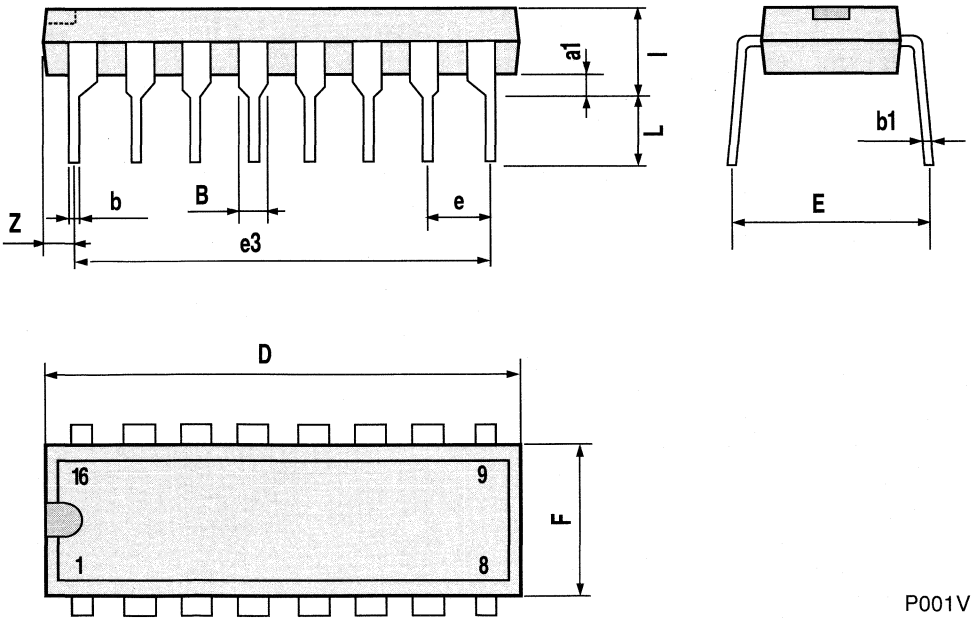
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (8+8), (12+2+2)

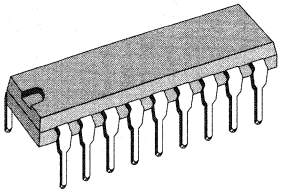


P001V

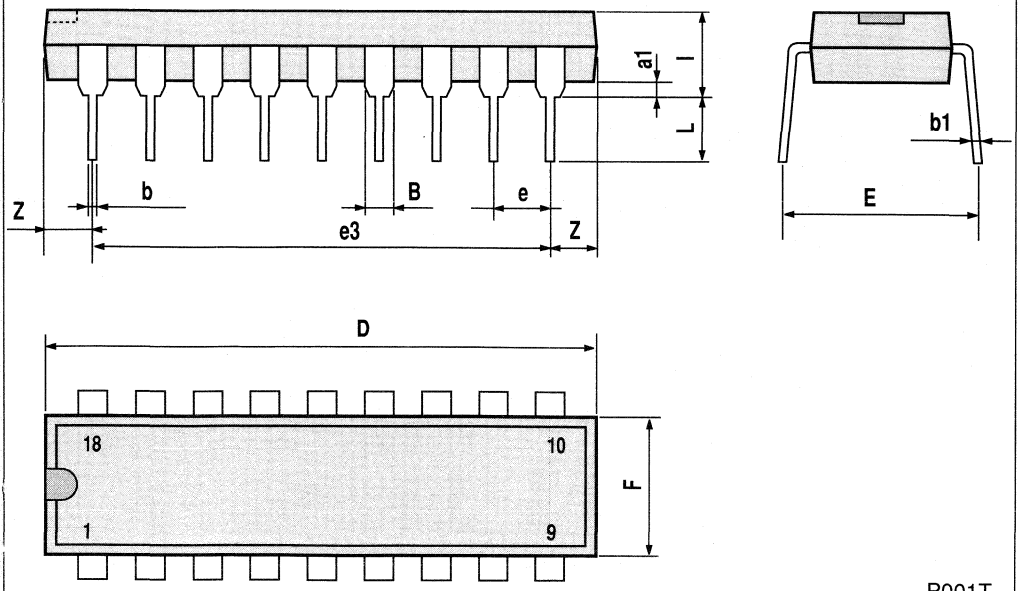
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.062

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18 (0.25)

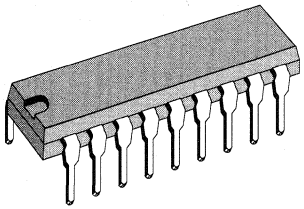


P001T

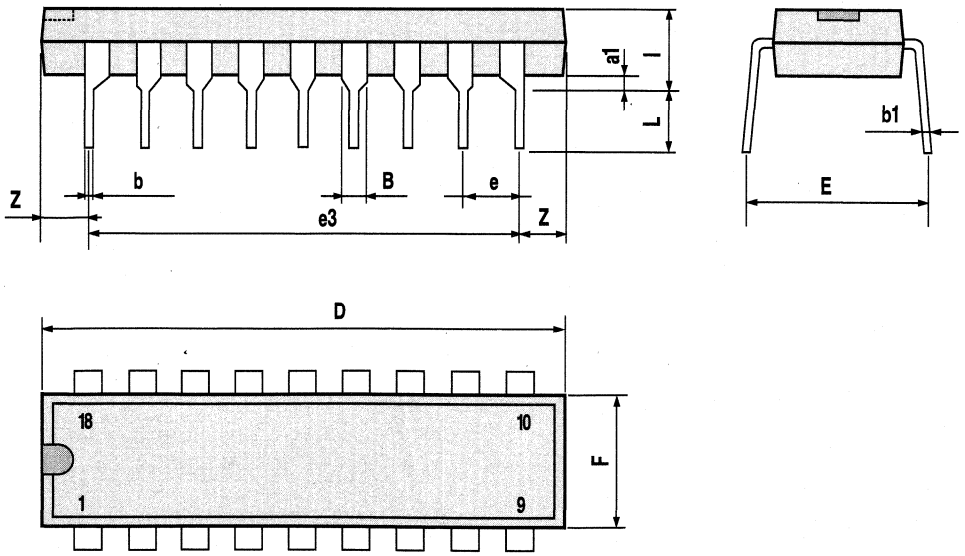
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (9+9), (12+3+3)

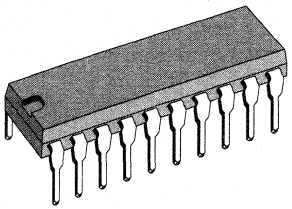


P001U

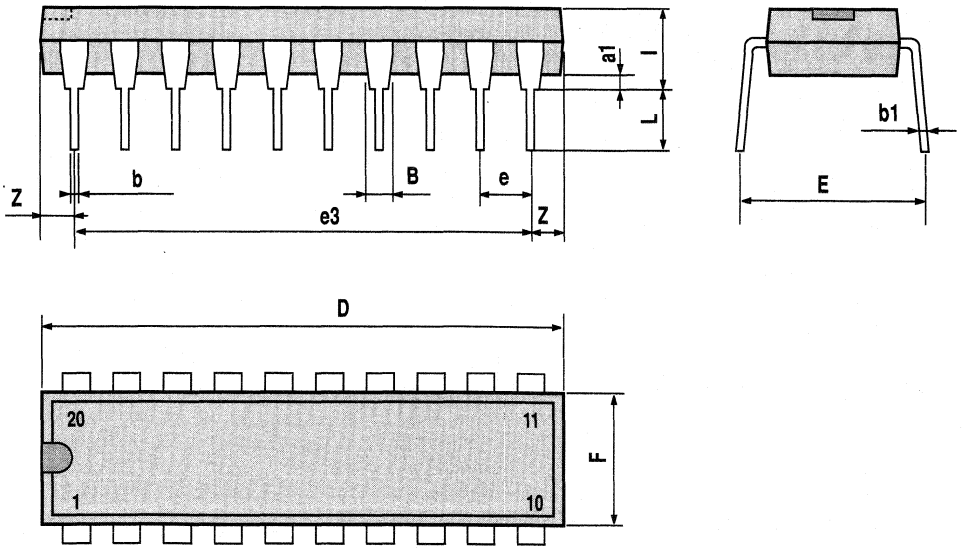
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

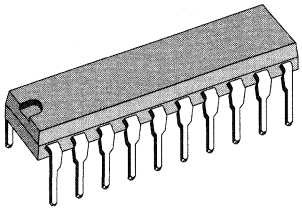


P001J

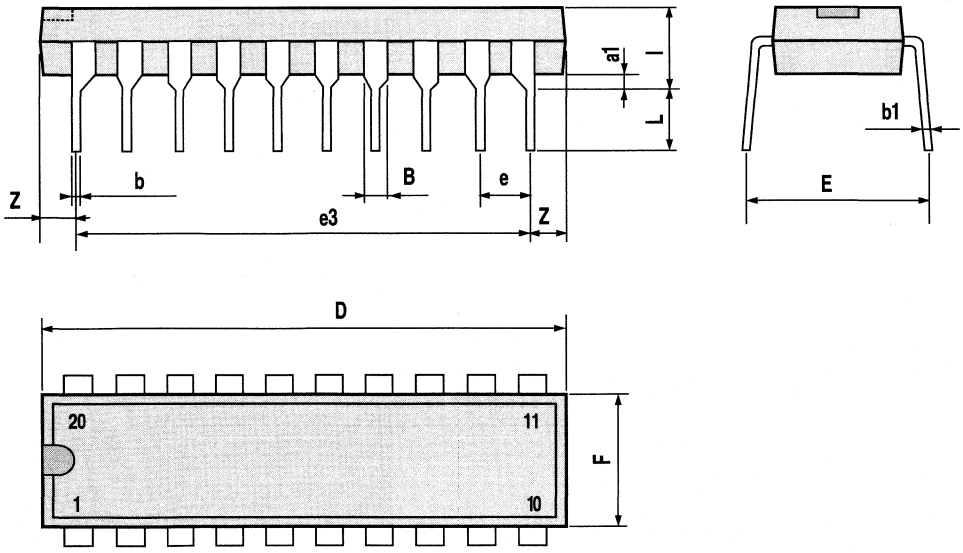
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP (16+2+2)

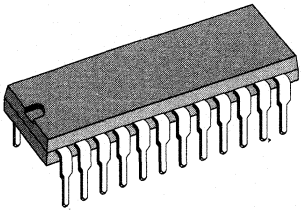


P001X

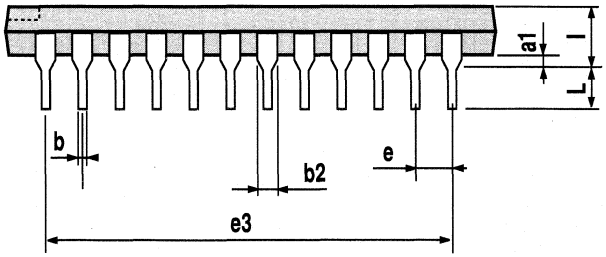
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

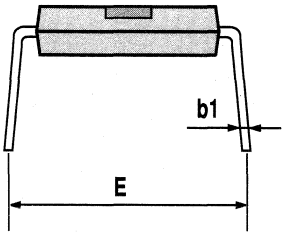
SGS-THOMSON MICROELECTRONICS

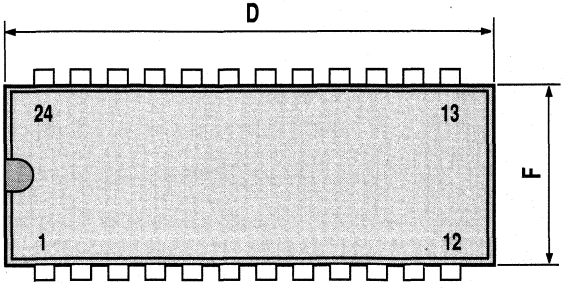
OUTLINE AND MECHANICAL DATA



DIP24 (0.25)





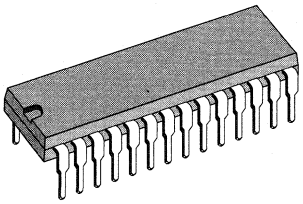


P043A

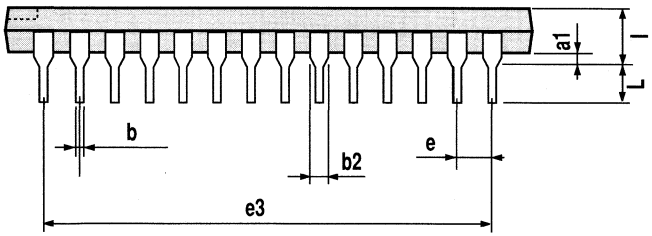
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

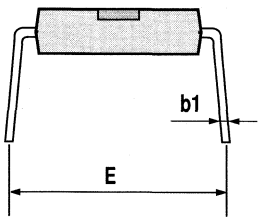
SGS-THOMSON MICROELECTRONICS

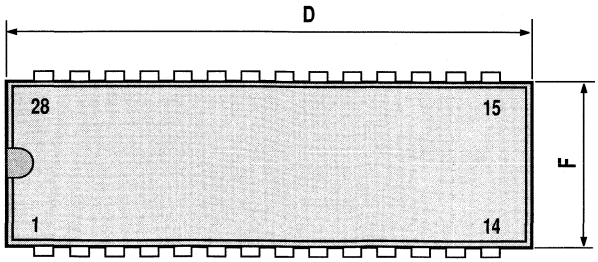
OUTLINE AND MECHANICAL DATA



DIP28





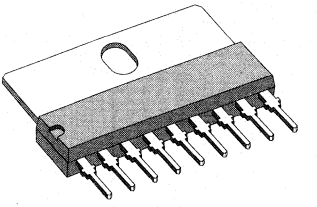


P043D

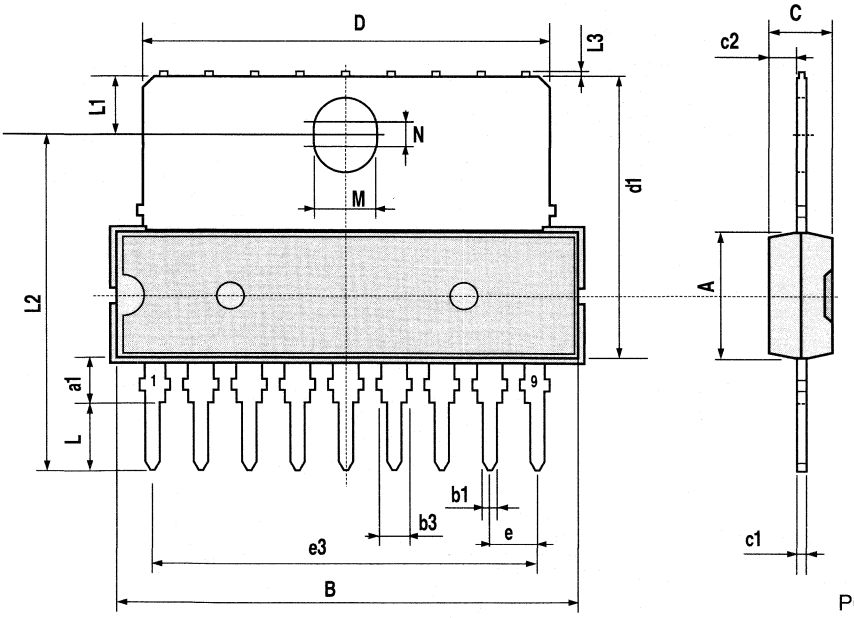
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SIP9

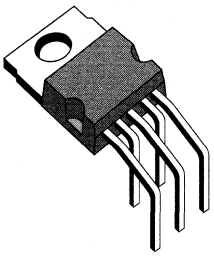


P030A

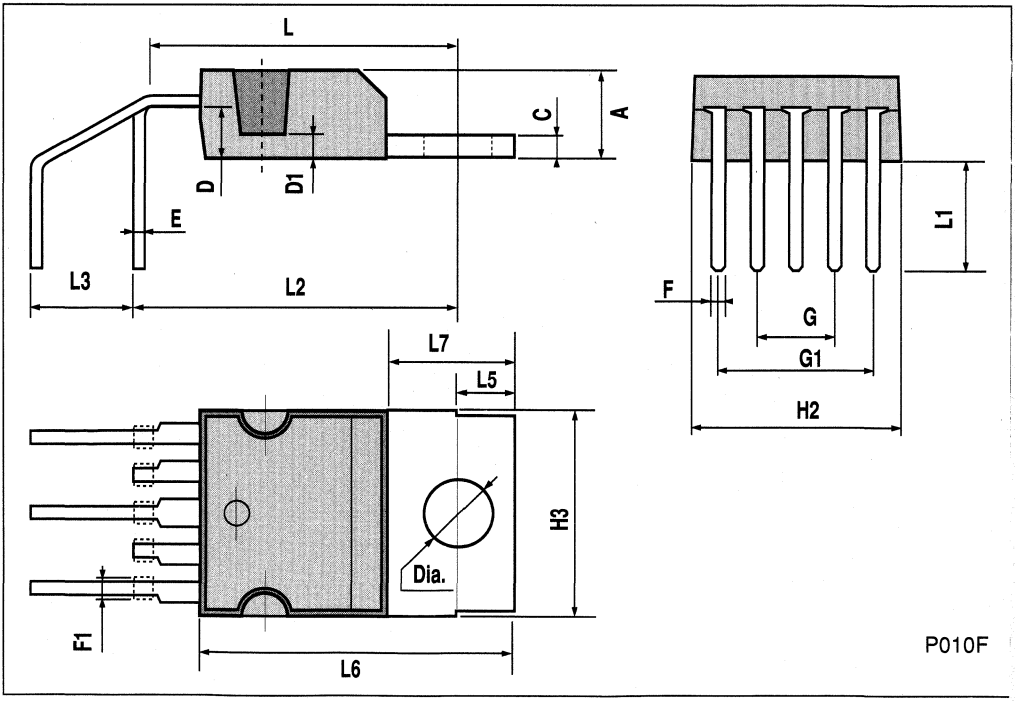
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		6			0.236	
L2		14.8			0.583	
L3	3.6		4.2	0.142		0.165
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt H

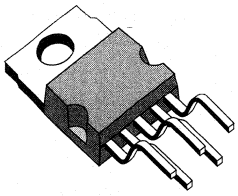


P010F

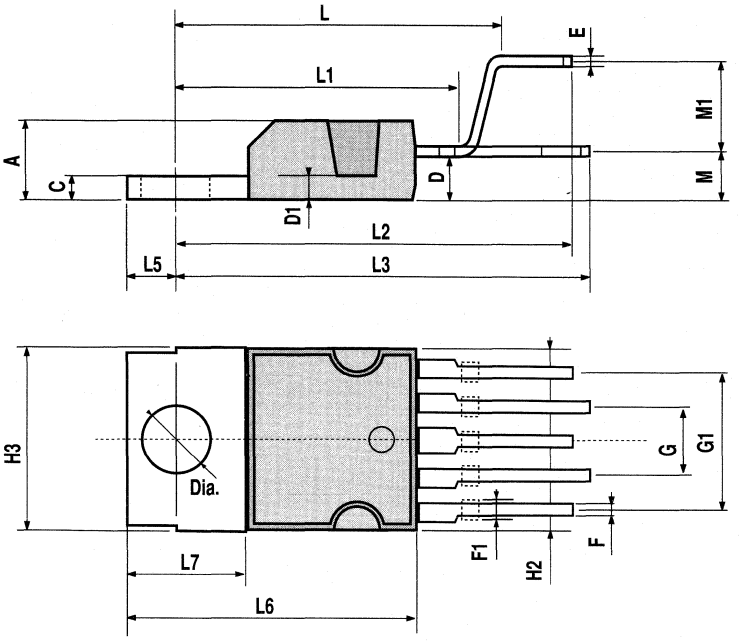
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt V

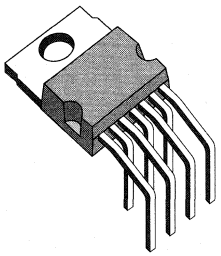


P010E

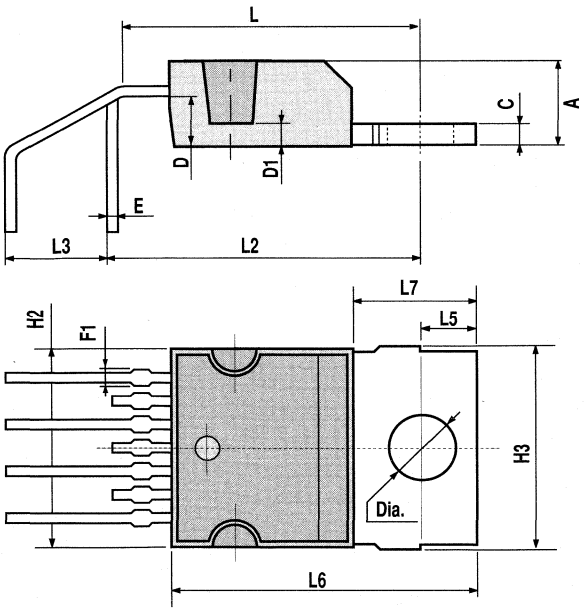
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		4.4			0.173	
L2		15.8			0.622	
L3		5.1			0.201	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
L9		4.44			0.175	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt H

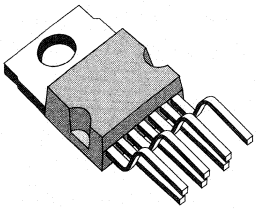


P023B

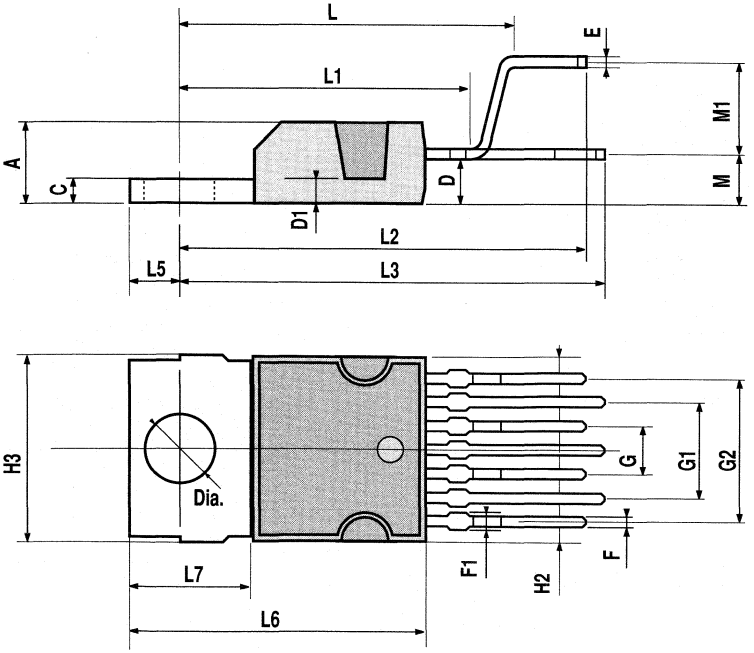
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt V

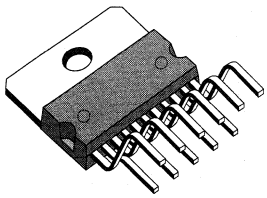


P023A

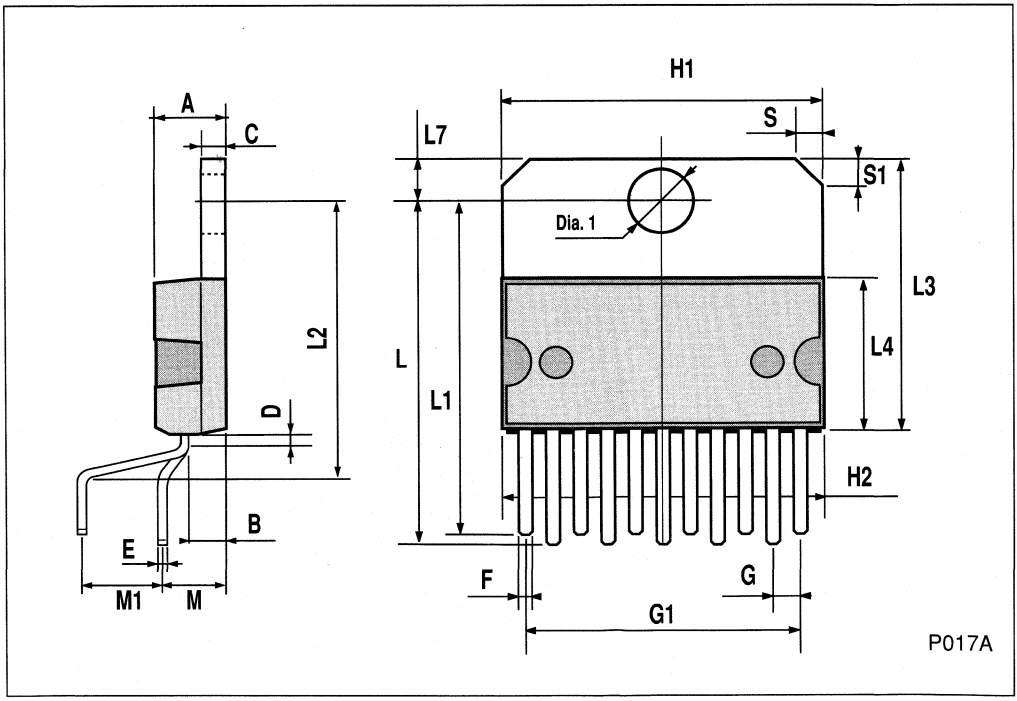
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	21.5		22.3	0.846		0.878
L1	21.4		22.2	0.843		0.874
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.1	4.3	4.5	0.161	0.169	0.177
M1	4.88	5.08	5.3	0.192	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



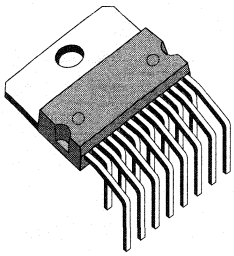
Multiwatt11 V



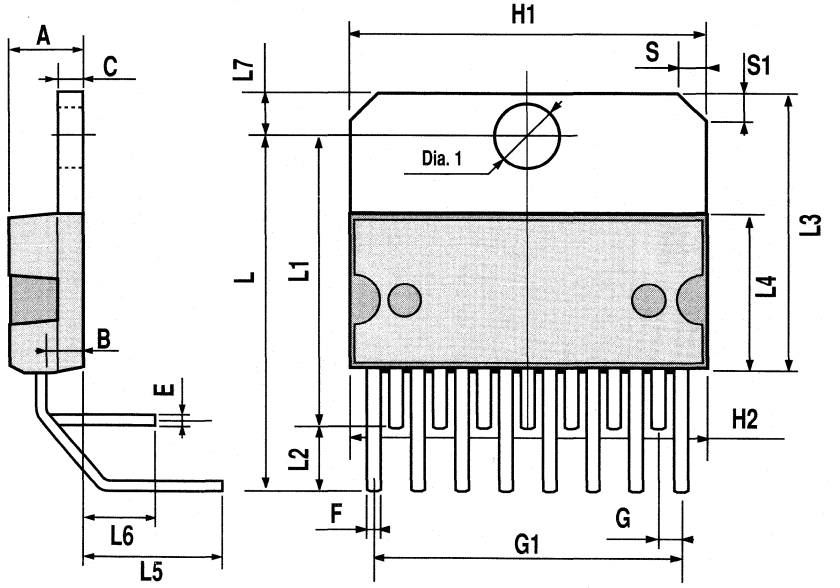
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt15 H

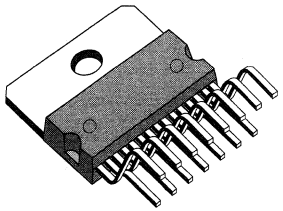


P017H

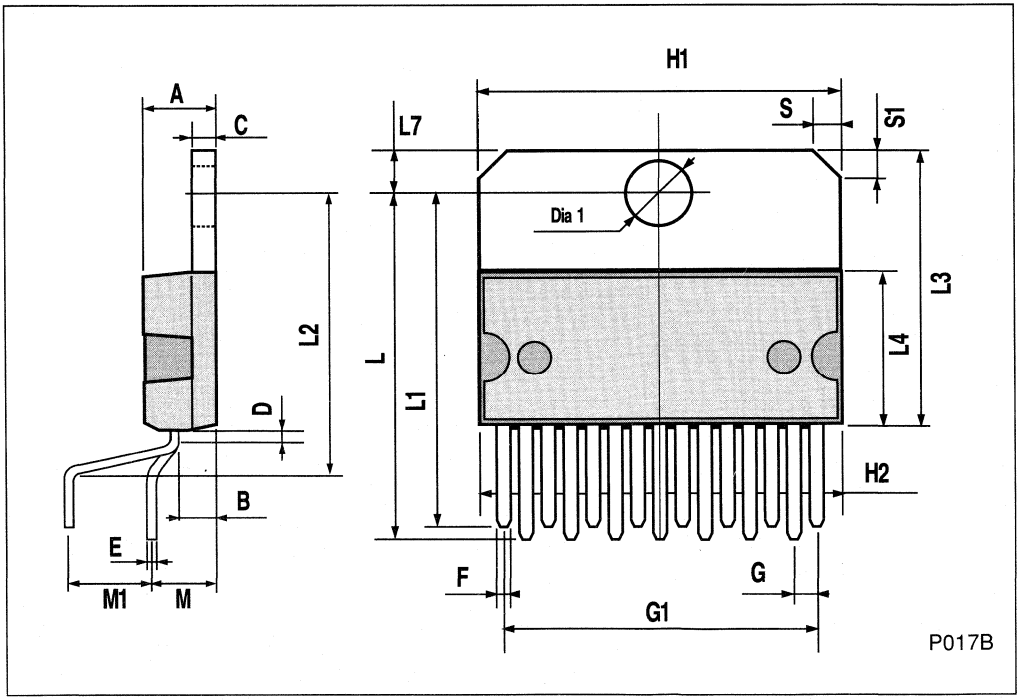
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



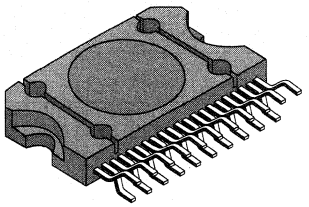
Multiwatt15 V



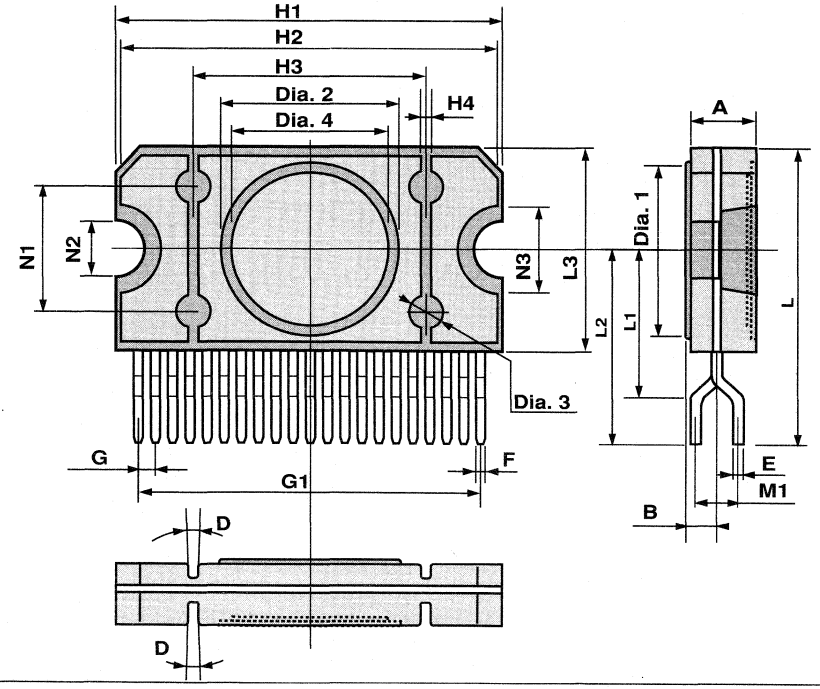
DiM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			1.9			0.075
D	4° (typ.)					
E	0.27		0.35	0.011		0.014
F	0.65		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	25.15	25.4	25.65	0.990	1.000	1.010
H1	28.9		29.1	1.138		1.146
H2		28			1.102	
H3		17			0.669	
H4		0.8			0.031	
L	22.4		23.0	0.881		0.905
L1	11.7		12.2	0.460		0.480
L2	14.7		15.2	0.579		0.598
L3	15.2	15.5	15.8	0.598	0.610	0.622
N1		10.0			0.393	
N2		4.2			0.165	
N3		6.8			0.268	
M1	2.2	2.54	2.85	0.087	0.1	0.112
Dia1		13.0			0.512	
Dia2		14.0			0.551	
Dia3		2.5			0.098	
Dia4		12.0			0.472	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Flexiwatt21 V

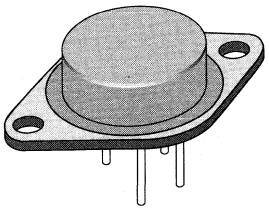


P035C

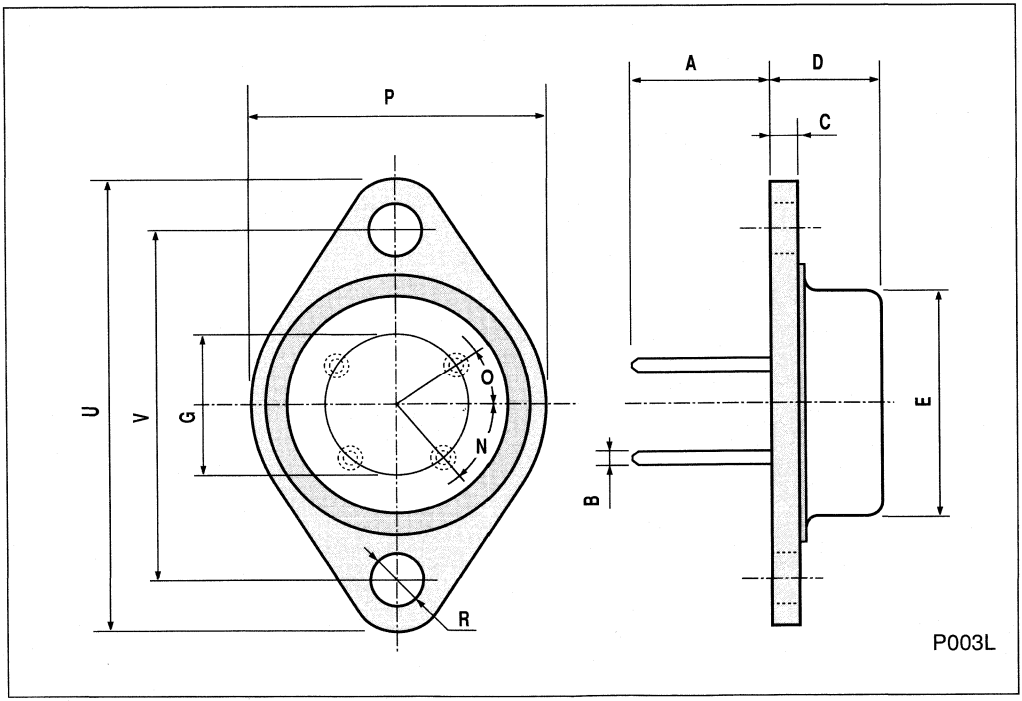
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		11.8			0.46	
B		1			0.39	
C			2.5			0.098
D			9.6			0.37
E			20			0.078
G		12.7			0.50	
N	50° (typ.)					
O	30° (typ.)					
P			26.2			1.03
R	3.88		4.20	0.15		0.16
U			39.5			1.55
V		30.1			1.18	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO3 (Four Leads)



DATASHEETS
SUBSYSTEMS MODULES

SGS-THOMSON MICROELECTRONICS

GS-C200
GS-C200S

INTELLIGENT STEPPER MOTOR CONTROLLERS

FEATURES

- Absolute and incremental positioning
- Up to 999,999 step per move
- Speed range to 10,000 steps/s
- Ramp lenght to 999 steps
- Single unregulated supply voltage
- Index and velocity mode
- Automatic and Home positioning
- Loops and Delay execution
- Conditional start and stop
- Status feedback to the host
- RS232 communication port
- Point to point and Multipoint protocol
- Closed loop operation
- Counter preset (GS-C200S only)
- Jump to (GS-C200S only)
- Jump to on-condition (GS-C200S only)
- Initialization during execution (GS-C200S only)
- Auxiliary output voltages +5V, ± 12V

DESCRIPTION

The GS-C200 and GS-C200S are powerful stepper motor control modules that interface every power sequencer/driver available on the market.

A sophisticated hardware and an easy to learn programming language result in minimal development and debugging time of motion control systems. The modules are supported by dedicated software that includes both an on-screen editor and a debugger that greatly improve the module ease of use.

The instruction sets comprise respectively 25 (GS-C200) and 29 (GS-C200S) different commands which can be executed either under host control or in a stand alone environment. An on board EEPROM is used for program saving and retrieving.

The availability of three User inputs and three programmable User outputs, each of which can be tested or set under program control, assures to the designer a high level of system power and flexibility.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
T_{stg}	Storage Temperature Range	– 40 to + 85	°C
T_{op}	Operating Temperature Range	0 to + 50	°C
	Humidity (non condensing)	0 to 90	%

ELECTRICAL CHARACTERISTICS (T_A = 25C and V_S=24V unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit
V_S	DC Supply Voltage		12		40	V
I_S	Quiescent Supply Current			80		mA
V_i	Logic Input Voltage (TTL compatible)	Low High	 2		0.8 5	V V
V_o	Logic Output Voltage (TTL compatible)	Low High	 2		0.8 5	V V
tcpw	Clock Pulse Width				5	µs
trpw	Reset Pulse Width (Internal)				500	µs

MOTION CHARACTERISTICS

SPEED RANGE	10 to 10000 steps
SPEED RESOLUTION	10 steps
RAMP LENGHT	1 to 999 steps
RAMP RESOLUTION	1 step
POSITIONING RANGE(C200) (C200S)	0 to 9999999 – 8388608 to + 8388607
SINGLE MOVEMENT RANGE	1 to 999999 steps
POSITIONING RESOLUTION	1 step
POSITIONING REPEATIBILITY	+/– 0 step
PROGRAM STORAGE CAPABILITY	119 bytes

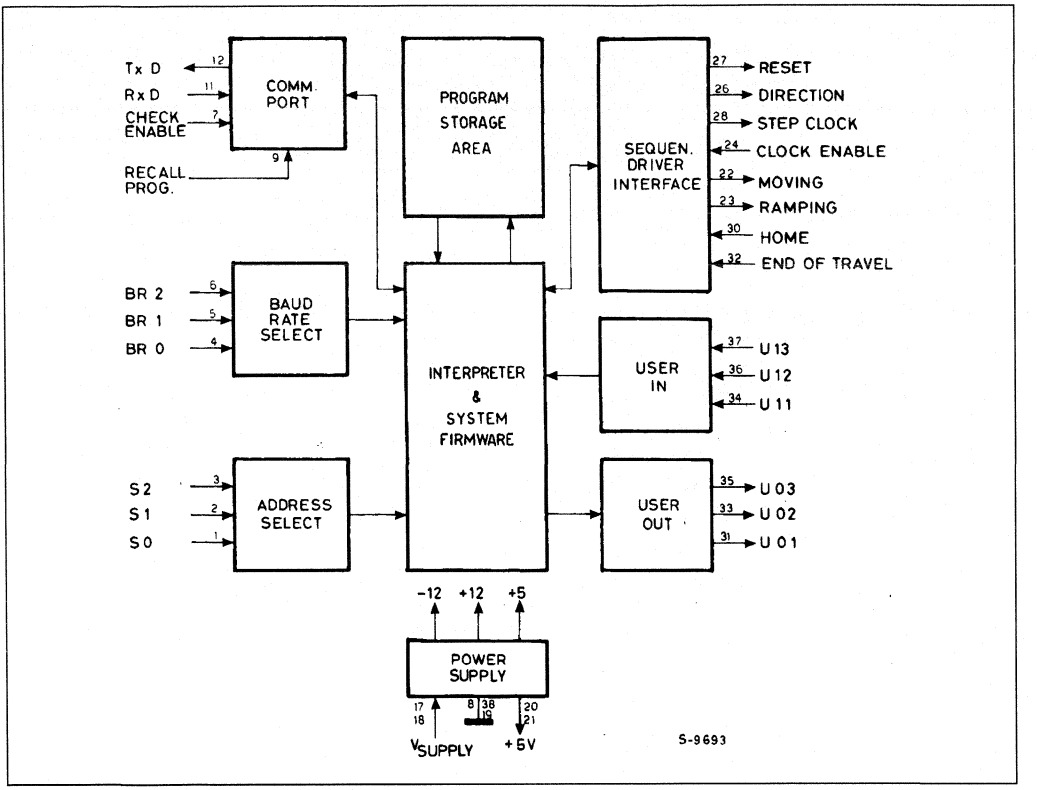
COMMUNICATION PORT CHARACTERISTICS

SIGNAL LINES	3 (TxD, RxD, GND)
BAUD RATE RANGE	110 to 9600
FORMAT	1 Start Bit 7 Data Bit 2 Stop Bit Odd parity

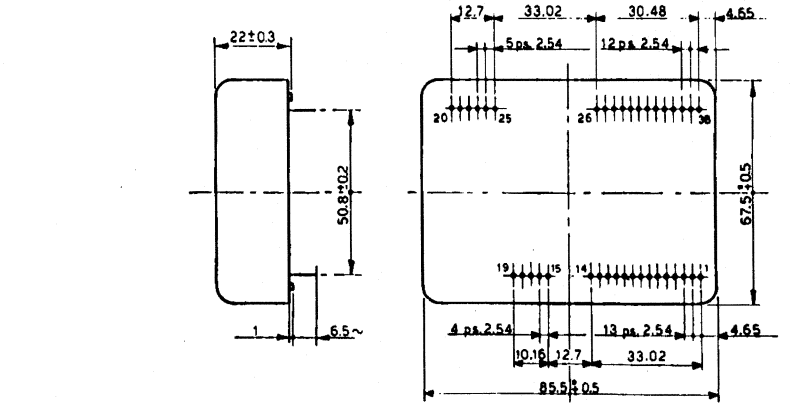
STORAGE CAPACITY

MINIMUM NUMBER OF COMMANDS	30
MAXIMUM NUMBER OF COMMANDS	45

Figure 1. Block Diagram



CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm.

Bottom view

PIN DESCRIPTION

Pin	Function	Description
1	SEL0	Protocol/address LSB select input
2	SEL1	Protocol/address SSB select input
3	SEL2	Protocol/address MSB select input
4	BR0	Baud rate LSB select input
5	BR1	Baud rate SSB select input
6	BR2	Baud rate MSB select input
7	CHS	Checksum enable input
8	GND	Ground
9	REC	Program autorecall input
10		Must be connected to pin 8
11	RXD	RS232 received data input
12	TXD	RS232 transmitted data output
13	TXPD	Transmitted data pull-down resistor
14	RDY	Status logic output
15	–VSL	Unregulated –12V supply output (note 1)
16	+VSL	Unregulated +12V supply output (note 1)
17	Vs	Supply voltage input
18	Vs	Supply voltage input
19	GND	Ground
20	5V	5V Auxiliary output (note 2)
21	5V	5V Auxiliary output (note 2)
22	MOV	Motor moving logic output
23	RAMP	Motor ramping logic output
24	ENABLE	Stop enable logic input
25		Not connected
26	DIR	Direction selection logic output
27	RESET	Power driver Reset logic output
28	CLOCK	Step clock logic output
29		Not connected
30	HOME	Home position logic input
31	UO1	User 1 logic output
32	EOT	End of travel switch logic input
33	UO2	User 2 logic output
34	UI1	User 1 logic input
35	UO3	User 3 logic output
36	UI2	User 2 logic input
37	UI3	User 3 logic input
38	GND	Ground

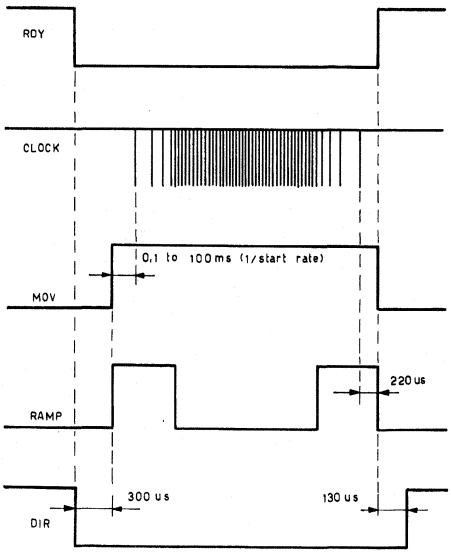
Notes: 1 – Maximum available current is 10mA
2 – Maximum available current is 100mA

The various signals that characterize the GS-C, their function and the active level are described in detail in the following:

Pin	Function
1 - 2 - 3	The SEL0 (pin1), SEL1 (pin2) and SEL2 (pin3) inputs are used to select the communication protocol and the module address. They have an internal pull-up and when unconnected they are at the 1 logic level.
4 - 5 - 6	The BR0 (pin4), BR1 (pin5) and BR2 (pin6) inputs are used to select the Baud rate of the communication port. They have an internal pull-up and when unconnected they are at the 1 logic level.
7	The CHS checksum generation conditioning input enables the user to include or exclude the checksum character from the data exchange string. A "zero" logic level applied to this input disables the control and the generation of the checksum character thus allowing the GS-C to be connected to a video terminal.
8	This pin is the common terminal for all logic signals and for the power supply return path.
9	The REC Recall Program Enable input pin, when brought to "zero", enables the automatic recall of the program stored in the EEPROM and its immediate execution.
10	This pin is for testing purpose only and it must be grounded for normal operation.
11	The RxD input of the serial communication port is used by the module to receive commands from the Host Computer. The input logic levels are compatible with the RS232 and V24 standards.
12	The TxD output of the serial communication port is used by the module to send data to the Host Computer. The logic levels of this output are compatible with the RS232 and V24 standards.
13	The TxPD Transmitted data pull-down resistor pin must always be connected to the TxD output (pin 12) when the Point-to-Point protocol is used. When the Multipoint protocol is selected, this pin must be left open on all modules except the chain terminator unit, in order to avoid the TxD output overload.
14	The RDY hardware status output (open collector) signal pin is used as the controller status flag. RDY assumes a "zero" logic level when a command or a program is in execution
15	–12V unregulated output. A maximum of 10mA can be sinked from this pin.
16	+12V unregulated output. A maximum of 10mA can be sinked from this pin.
17 - 18	Module supply input. For correct operations a supply voltage ranging from 12 to 40 Volt is required.
19	See pin 8.
20 - 21	5 Volt regulated output, available either for the Sequencer-Driver logic section or for a custom interface logic supply. The maximum current that can be sinked from this pin is 100mA.
22	The MOV Motor moving output becomes the logic level "one" when the GS-C is executing a movement. This output can be used to program the phase current level when the motion is running at a level higher than for the rest condition.
23	The RAMP Ramp in execution output is rised to the logic level "one" when the GS-C is executing an acceleration or a deceleration ramp. This output can be used to program the phase current level when the motion is ramping at a level higher than for the rest or slewing condition.
24	The ENABLE input pin allows the user to control the Step clock logic output to avoid the motor being stepped if the previous step was not correctly executed. A "zero" logic level applied to this pin stops the generation of the step pulses. This input can be used to stop the system when an emergency occurs, to execute the motion according to externally generated timing, or to implement a closed loop control system.
25, 29	Not connected.
26	The DIR Direction selection output is used to inform the Sequencer-Driver on the direction of rotation. The logic level "one" determines a clockwise rotation, but of course the rotation depends on the motor phases connection to the Sequencer-Driver.
27	The RESET Power driver Reset output is brought to the "zero" logic state for 400µs when the unit is powered-on, or when the GS-C receives the "Initialize position counter" command. This output is normally used to assure the correct start-up of the Sequencer-Driver or any other external custom logic.

Pin	Function
28	The CLOCK Step clock output is used to inform the Sequencer-Driver to perform a step. The direction (clockwise or counterclockwise) is defined by the logic status of the DIR output. In steady conditions, the CLOCK is at the "one" logic level, and the step is represented by a negative going pulse with a 1.7µs duration.
30	The HOME Home position input allows the system to find its reference point. This input can be driven by a mechanically activated contact indicating the "zero" position. It is normally used together with the EOT End-of-travel signal.
31	The UO1 User output 1 is intended for user purposes. The status of this output can be set and cleared under program control and it can be used for various functions. It is normally used for the control of external devices, the selection of the Sequencer-Driver operating mode, or the synchronization of complex movements.
32	The EOT End-of-travel input allows, in combination with the HOME input, the correct mechanical initialization of the system. For this purpose it must be brought to the "zero" logic level when the system reaches the run end position.
33	The U02 User output 2 is intended for user purposes. See pin 31 description.
34	The UI1 User input is intended for user purposes. The status of this input can be read by the Host Computer or tested during the program execution, and used to condition the start of a movement, the execution of a specific portion of a program (GS-C200S only), or any other similar operation.
35	The UO3 User output 3 is intended for user purposes. See pin 31 description.
36	The UI2 User input 2 input is intended for user purposes. See pin 34 description.
37	The UI3 User input 3 input is intended for user purposes. See pin 3 and pin 4 description.
38	See pin 8.

Figure 2. GS-C Timing Diagram



S.I.M.P.L.E. Interpreter Command and Functions
(**S**GS-**T**HOMSON **I**nteractive **S**tepper **M**otor **P**rogramming **L**anguage and **E**xecutor)

Command	Byte Length	Function
Ax	2	Activate the specified (x) User output.
Cx	2	Clear the specified (x) User output.
Dxxx	2	Delay for the specfied number (xxx) of tenth of second.
E	–	Start executing the program currently stored into RAM memory.
F	–	Feedback the GS-C status (i.e. Ready or Busy).
f+/–xxxxxxx	4	Preset the position counter to the specified absolute value (C200S).
G+/–xxxxxxx	4	Go to the specified target position (C200S).
g(+/–)	4	Move the motor indefinitely in the specified direction.
g(+/–)x	4	Move the motor in the specified direction until the specified (x) input is brought to zero.
H(+/–)	–	Find Home position moving clockwise (+), or moving counterclockwise (–).
Ix	2	Initialize the position counter (x=1), the user outputs (x=2), or both (x=3).
jx	2	Jump to memory location (x). Location (x) ranges between 0 and 118 (C200S).
jcy, x	2	Jump to memory location (x) if the binary value of the user inputs matches (y) value (C200S).
K	–	Kill the program in execution.
Lx	2	Loop for the specified (x) number of times.
M	–	Transfer the RAM memory content to EEPROM.
P	–	Enter the programming mode (C200).
Po	–	Enter the programming mode (C200S).
Px	–	Exit the programming mode (C200S).
Q	–	List to the host the program currently in RAM memory.
Rxxx	4	Set the Ramp length to the specified (xxx) value.
Sxxx	4	Set the start-stop speed to the specified (xxx) value.
Txxx	4	Set the slew rate speed to the specified (xxx) value.
Ux	2	Execute the program until the specified (x) user input is brought to a low level.
Vx	–	Read back the curent position (x=1) or the user I/O status (x=2).
X	–	Transfer the program from EEPROM to RAM.
Wx	2	Wait until the specified (x) user input is raised to a logic one level.
Z	–	Stop through a deceleration ramp.
+/–xxxxxx	4	Move clockwise (+) or counter-clockwise (–) for the specified (xxxxxx) number of steps.

GS-200 AND GS-200S DESCRIPTION

The increasing popularity of microprocessors and their very low cost, have contributed to a fast growth of stepper motors usage in a large numbers of application previously covered by more complex, bulk and expensive DC motors servo loops. The GS-C200 and the GS-C200S modules have been conceived to help the industrial designer in designing the stepper motor applications based on microprocessor control.

These modules are programmable intelligent stepper motor controllers that coordinate highly complex movements and sequential operations. This capability is performed through the integration of sophisticated hardware and an easy to learn and very functional and powerful programming language.

Thanks to this high level programming language, the power of the instruction set and the ability to condition and control the program execution through the USER inputs and outputs, the GS-C200 and GS-C200S drastically reduce the design time and start-up manufacturing phase of very complex systems. The GS-C200S offers an advanced and powerful instruction set that includes also the conditional jump which allows for more efficient program-ming. The GS-C200, the GS-C200S and their companion modules, the GS-D200 and the GS-D200S, can be used to drive in chopped mode of bipolar stepper motor with a 2/2.5A maximum phase current rating.

The two modules (GS-C and GS-D) are available also on a single Eurocard board named respectively GS-DC200, GS-DC200S and GS-DC200SS according to the various modules combination (see the relevant data sheet). In the following the modules will be generically named GS-C. The specific module part number will be used when the feature is unique to that module.

A MOTION SYSTEM ARCHITECTURE

A complete motion system controlled by a host computer is normally configured as per fig. 3.

The GS-C logical and functional architecture is shown in fig. 1 and it includes the following basic blocks:

- Interface to the Host Computer via an RS232 communication port.
- Address and baud rate selection.
- Interface to the Sequencer-Driver (in particular but not exclusively, to the GS-D200 or GS-D200S) via 5 output and 3 input lines
- Command Interpreter and Executor.
- Program storage area
- Power Supply.

The above mentioned functions are performed by the GS-C without the addition of any external component, and the module flexibility is further enhanced by the use of only one unregulated supply voltage that can be the same used to supply the Sequencer-Driver (from 12V up to 40V).

Commands are sent to the module by a Host Computer or by a simple video terminal during the programming/debugging phase through an RS232 serial port. They are interpreted and validated by the command interpreter and executed through the Sequencer-Driver interface.

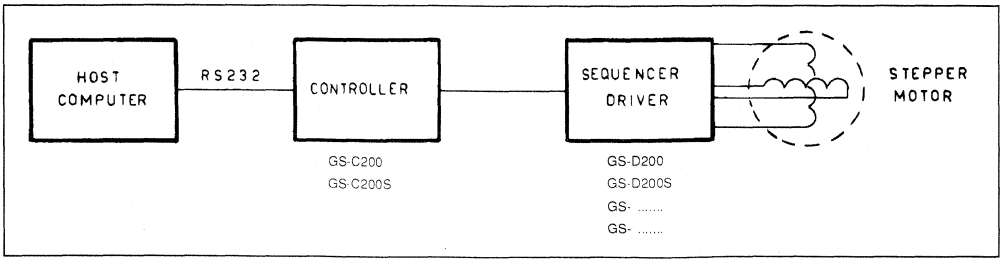
Command execution can be conditioned and controlled by the status of the USER IN-OUT interface.

A program storage area has been added to permanently store a program in an on-board EEPROM; this is particulary beneficial to obtain a low cost stand-alone controller that does not need any connection to an external computer or to store programs frequently used in complex motion sequencies thus reducing the host computer burden and speeding up the system processing.

Particular attention has been given to the simplicity of the instruction set to allow an easy design of the system to those designers that are not very familiar with microprocessor software and programming.

In the following a detailed description of the various functional blocks is given.

Figure 3. A Motion System Block Diagram



INTERFACE TO THE HOST COMPUTER AND DATA PROTOCOL

The interface to the Host Computer is through an RS232 or V24 serial communication port.

Baud Rate Programming

The Baud rate is programmed between 110 and 9600 bit/sec by using the BR0, BR1 and BR2 inputs according to the following table:

BR0 (p4)	BR1 (p5)	BR2 (p6)	Baud Rate
0	0	0	9600
1	0	0	4800
0	1	0	2400
1	1	0	1200
0	0	1	600
1	0	1	300
0	1	1	150
1	1	1	110

This setting is obtained by connecting the pins 4, 5, and 6 to ground (0 status) or by leaving them open (1 status). The communication port does not use any control line but just the transmit and receive signals. The host computer must handle the data excange in the proper way.

Module Address Programming

The communication protocol can be either Point to Point or Multipoint. In the first case a single communication line is required for each module, while in the latter more than one module (up to seven) can share the same communication line.

The Multipoint protocol as well as the peripheral device address are selected through SEL0, SEL1 and SEL2 inputs. The Point-to-Point protocol is selected by connecting all the SEL inputs to the 5V output pin (pin 20) or by leaving them open.

The following table defines the protocol and the address setting:

SEL2	SEL1	SEL0	Address	Protocol
0	0	0	7	Multipoint
1	0	0	6	Multipoint
0	1	0	5	Multipoint
1	1	0	4	Multipoint
0	0	1	3	Multipoint
1	0	1	2	Multipoint
0	1	1	1	Multipoint
1	1	1	–	Point-to-Point

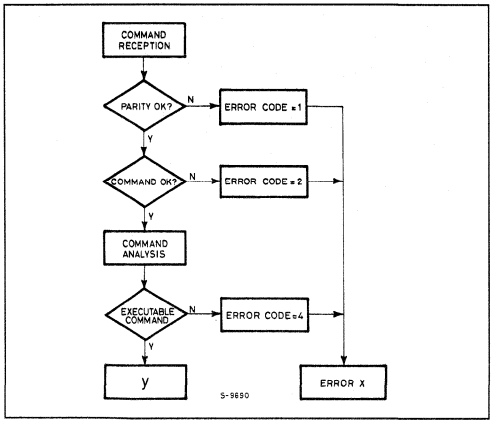
When the multipoint connection is chosen, the address of each module is obtained by connecting the various SEL pin (1, 2, 3) to ground (0 status) or by leaving them open (1 status).

The basic difference between the two protocols is represented by the sytem wiring complexity and the data throughput. The Point-to-Point offers the higher throughput data rate but it requires a connecting cable for each unit, while the Multipoint minimizes the connecting cables but at reduced throughput rate. When this latter protocol is chosen, the command must always be preceeded by the address of the unit.

Data Excange Protocol

The dialogue is always driven by the Host Computer which sends the string containing the command or the request to be implemented. The GS-C module stores the instruction sent by the Host and then it checks if the string has been correctly received by analyzing the parity bit. It then analyzes the consistency of the received instructions by verifying the presence and correctness of the argument, and finally, it checks whether the request can be processed or not (for example, an attempt to move outside the system limits, etc.) reporting to the Host the analisys result. If no error is detected, the GS-C replies to the Host by a "Y" message. In case of error, the message will be "Error X" requesting the Host to send the message again or to modify some parameters of the previous message to fix the error detected by the GS-C. The actual value of X (see fig. 4 and error code table) gives the Host the information on the type of detected error. The procedure implemented for the dialogue with the Host is shown on the flowchart of fig. 4.

Figure 4. Controller-Host Dialogue Flowchart.



The general format of a command string is the following:

ADDRESS	COMMAND	ARGUMENT	CHECKSUM	CAR.RETURN

The **Address** must be the first transmitted character and it is present only if the Multipoint protocol is used (at least one of SEL0, SEL1, SEL2 is different from zero).

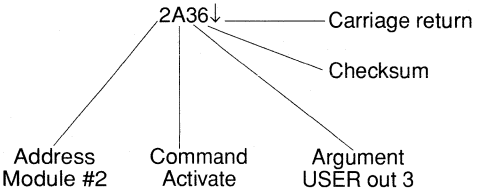
The **Command** is the second character(s) of the string, in the Multipoint protocol, but it becomes the transmission opening character when the Point-to-Point protocol is used (SEL0, SEL1 and SEL2 = 0).

The **Argument**, if required, is specified immediately after the command and its length depends on the command type.

The **Checksum** character verifies the correctness of the received string; its value is determined by the sum of the binary values of the preceding characters. The result is cut at the seventh least significant bit and ORed with exadecimal 10 (C200S/C200 from V2.2) to make the result compatible with the transmission system. The last character, the string ending character, is always a **Carriage Return** that will be identified in the following by the symbol (↓).

By connecting the pin CHS (pin 7) to ground, the checksum character is not anymore requested, and the task of guaranteeing the correctness of the message is left to the parity bit. It should be noted that by using this dialogue mode, the data integrity confidence level is reduced. Because motion systems normally operate in manufacturing premises subjected to heavy electro-magnetic noise, and because any communication problem may have catastrophic effects on the system actions, it is a good practice to use the checksum character whenever possible. The checksum character is normally not used (pin CHS connected to ground) when the GS-C is connected to a video-terminal, i.e. during the initial programming and debugging phase. In the following, three examples of command strings sent to a GS-C module are given.

Example 1 - MULTIPOINT PROTOCOL. The Host Computer wants to set the USER output 3 of the module #2. The command will have the following format:



The checksum character **6** results from the binary sum of the character **2** (ASCII value = 32) + character **A** (ASCII value = 41) + character **3** (ASCII value = 33) truncated at the seventh bit.

Example 2 - POINT-TO-POINT PROTOCOL.

The same instruction is given by the Host to a Point to Point connected module.

The command will have the following format:

A3t↓

The checksum character has an ASCII value **t** that derives from the sum of the ASCII code A+3 = 41+33 = 74 in binary weighted code or **t** in ASCII code.

Example 3 - POINT-TO-POINT PROTOCOL WITHOUT CHECKSUM.

For the same instruction, the command format will be:

A3↓

The string consists of command and argument only.

The GS-C feeds back information to the Host every time it receives a command, therefore it has not to identify itself to the Host when answering in a Multipoint connection.

The format of the string answered back by the GS-C is the following:

ANSW.CODE	ARGUMENT	CHECKSUM	CAR.RETURN

The first character, which always identifies the answer type, may assume one of the following values:

Y The command string has been correctly received.

B The controller is Busy and cannot process commands.

R The controller is Ready to process commands.

E An error has been detected. The type of error is specified by the number following the "E".

V A controller status (a position or an USER input/output status) is sent back and its value is specified by the characters following the "V".

The length of the Argument, present only for "E" and "V" answers, can range between 1 and 7 characters, and it is a function of the received command. The number following the "E" code, i.e. the error argument, specifies the detected error type according to the following table:

Error code	Type of error
1	Parity error when receiving one or more characters, checksum error, or too long a command string.
2	Command argument out of limit or not requested.
3	Storage capacity overflow.
4	Not allowed or not executable command.
5	Overflow error during program execution (GS-C200 only).
6	EEPROM programming error.

The number following the "V" code depends on the type of the received command.

When the GS-C answers to a "V1" request (feedback the actual absolute position against the Home position), the answer will be:

Vxxxxxxx↓

where the xxxxxxx represent the absolute position.

When the GS-C answers to a "V2" request (feedback the USER input/output status), the answer will be:

Vxy↓

where the x and y meaning is:

x = 1	User Input 1 = 1
x = 2	User Input 2 = 1
x = 4	User Input 3 = 1
y = 1	User Output1 = 1
y = 2	User Output 2 = 1
x = 4	User Output 3 = 1

The logic values of the inputs and outputs are added together. For example the answer:

V36↓

indicates the following USER I/O status:

UI1 =	1	UO1 =	0
UI2 =	1	UO2 =	1
UI3 =	0	UO1 =	1
	3		6

The presence of Checksum character, whose value is calculated by using the method described in the previous example, is conditioned by the CHS pin status.

When CHS is grounded (either by a logic signal or by a strap to ground) the checksum is deleted.

The string terminator is, as in the previous case, a Carriage Return.

THE SEQUENCER-DRIVER INTERFACE

The interface to the Sequencer-Driver and, through it, to the mechanical environment, consists of eight logic signals (5 outputs and 3 inputs) which enable the GS-C intelligent controller to interface the GS-D200 or the GS-D200S modules as well as any Sequencer Drivers currently available. The eight signals can be divided into two groups, named respectively:

PRIMARY SIGNALS

UTILITY SIGNALS

The primary signals are those necessary for the correct system operation:

RESET	Output to reset the Sequencer-Driver.
CLOCK	Step clock output.
DIR	Direction output.
ENABLE	Step enable input.

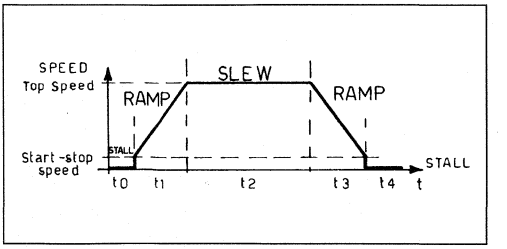
The function of each signal is described in detail in section **PIN DESCRIPTION** on page 4/31; it will be shown later that the Step Enable Input in conjunction with the position sensor of the motor, allows the implementation of closed loop systems (see paragraph **Closed Loop Operation** on pag. 27). The Utility signals allow the optimization of the driving system and the minimization of the hardware. They are:

MOV	Movement in execution output.
RAMP	Ramp in execution output.
EOT	Mechanical End of Travel input.
HOME	Electrical Home Position input.

By using these signals it is possible to correctly define the system starting point or reference position, or to change the current in the motor windings during the acceleration and deceleration phases in order to optimize the motor performance.

A typical example of the utility signals implementation is given here. Let's suppose that the required speed profile is as shown in fig. 5.

Figure 5. Speed-Time Profile.



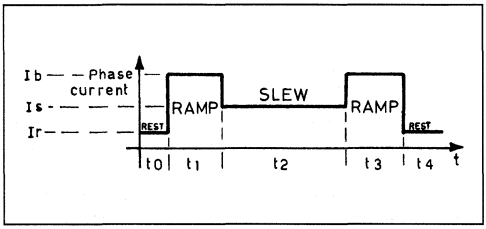
To optimize the motor torque during the acceleration and deceleration (t_1 and t_3) it is convenient to use a phase current profile as shown in fig. 6. During the SLEW phase (t_2) when the motor rotates at constant speed, the current is reduced to the minimum value necessary to compensate the system losses (friction) and the load inertia. During the STALL phase (t_0 and t_4) the current is further reduced to the bare value necessary to maintain the load in the right mechanical position. By using this current profile the power dissipation of the Sequencer-Driver and motor is optimized.

This profile can easily be implemented by using the utility signals:

MOV Movement in execution.

RAMP Ramp in execution.

Figure 6. Phase Current-Time Profile.



The status of these two outputs can be used to set the appropriate phase current value for the power driver, by a simple but effective interface circuit that is described in detail in fig. 11 of paragraph **PHASE CURRENT PROGRAMMING** on page 24.

THE USER INTERFACE

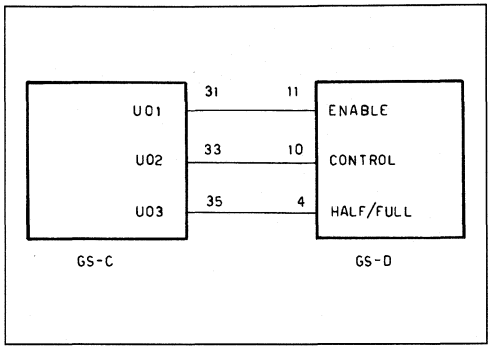
The USER interface consists of three inputs and three outputs which are TTL compatible. They can be read and/or activated during the execution of a program under the complete user control; therefore they condition a program execution.

These signals allow the implementation of complex movements, minimizing the program length and the use of external hardware. The start of a movement or of a sequence can be conditioned by a logic level applied to one or more inputs, thus performing the "mechanical tree" function.

The USER outputs logic state is set by program instructions and this information can be used by other controllers to synchronize multiple movements or to control external drivers.

By using only these signals, it is possible to build up simple systems which implement cyclic movements and create a true stand-alone system. The example reported in figure 7 shows one of the possible utilization of USER output. The example

Figure 7. USER Output Applicative Example



refers to a complete motion control system implemented by using the GS-C200 controller and the GS-D200 Sequencer-Driver. The USER output UO1 is used to enable the GS-D200 (UO1 High) or to inhibit it (UO1 Low).

The USER output UO2 is used to select the motor current decay inherent to the chop mode control of GS-D200. When UO2 is high a slow decay is imposed to the phase current during recirculation; when UO2 is low a fast decay is selected.

The USER output UO3 allows the selection between the half and full-step mode of operation of the GS-D200. Half-step occurs when UO3 is high.

The GS-C200S is capable of executing a jump command either direct or conditioned by the logic status of the USER inputs. This capability is very useful because it allows complex programs to be written by using a limited number of instructions. This feature makes also possible to have a segmented program contained in the internal memory; the selection and the subsequent execution of the needed program segment is started by a specific logic status applied to the USER inputs.

THE S.I.M.P.L.E. COMMAND INTERPRETER AND EXECUTOR AND THE PROGRAMMING LANGUAGE

The GS-C modules contain an interpreter program named S.I.M.P.L.E., acronym for **S**GS-THOMSON **I**nteractive **S**tepper **M**otor **P**rogram **L**anguage and **E**xecutor, that recognizes simple mnemonic commands, verifies the correctness of the received commands and executes the instruction sequences of each command or a complete command sequence by translation into complex executable instructions. The interpreter recognizes three different types of commands:

DIRECT EXECUTION COMMAND

DELAYED EXECUTION COMMAND

UTILITY COMMANDS

Direct execution commands are immediately actuated. They include: start and stop the program execution, set the programming mode, check position, check I/O, etc...

Delayed execution commands are run when requested by the sequence currently stored in memory. By using a combination of these commands, it is possible to perform very complex movements including also the conditioning by external stimulus, the iteration of a specific sequence for a defined number of times.

Utility commands allow the GS-C modules to perform several additional functions such as the detection of the position, phase current optimization etc... These commands, when properly used, speed up the system debugging phase and they increase the system efficiency.

Note: To easily learn how to program the GS-C and to minimize development time, a P.C. based self explaining and interactive program named **F.A.S.T.** (**F**irst **A**dvanced **S**tepper motor **T**raining program), able to communicate with the module by using the Point-to-Point protocol, has been developed and it is available to the end user. (See GS-C200PROG data sheet).

Command strings can be easily implemented also by using a high level language such as BASIC, or they can be generated by a dedicated microcontroller programmed in machine language. The dialogue speed is limited by the time required to construct the command string and to analyze the GS-C data, and it results noticeably reduced when a "machine language" program is used.

The program, after testing, can be stored in the EEPROM included in the GS-C module and then loaded and automatically executed at power-up, resulting in a low cost stand-alone system. It is also possible to save the program as a DOS file on a floppy disk for future retrieval, or to ease the field update of the program itself.

Every command is identified by one or two characters and by a variable length argument (from 0 to 7 characters). If the Multipoint communication protocol is used, the address is specified by the number that preceeds the command. All the commands sent by the Host, as well as the data generated by the GS-C, are terminated by a Carriage Return (ASCII value = 0D).

In the following pages all the commands which may be executed by the GS-C200 and the GS-C200S are detailed, as well as their format. A practical example of the command usage is also given. The presence of an asterisk at the end of the command denotes that the command is executable only by the GC-C200, while two asterisk denote a command executed only by the GS-C200S.

Each command is shown in the same format used during the programming phase, i.e. the command identifier plus the argument:

Gs**x**x**x**x**x**x**x**

The argument can be single, double or missing according to the various command types.

The various argument are identified by different letters according to the particular type i.e.:

s = sign	+ or –
x = figure	1 to 3
y = figure	0 to 7
v = value	1 to 999 depending on command
p = position	1to 999999 incremental or the absolute position

Apart the different number of executable commands and functions, the GS-C200S and the GS-C200 look very similar each other. The only foundamental difference is the way they manage the position counter.

The position counter is the reference ruler for the microprocessor to move correctly from the actual position to the targeted one, executing the proper number of steps in the right direction.

The GS-C200 position counter allows a maximum of ten million steps to be executed, and the home position corresponds to the 0 count position. When a movement is larger than the position ruler limits an Error 5 is reported to the Host.

The GS-C200S position counter allows a maximum total count of 2^{24} step ranging from –8388608 to +8388607 steps. When the maximum count is exceeded the counter wraps-around. For example if the position counter is +8388606 and a +5 steps movement is executed, the final position will be:

+8388606	Initial position
+8388607	After 1 step execution
–8388608	After 2 steps execution
–8388607	After 3 steps execution
–8388606	After 4 steps execution
–8388605	Final position

Of course no error is reported.

Command	Description
Ax	The **Activate** command sets a User output to the active logic level "one". The command is always followed by an argument whose value ranges between 1 and 3, and that specifies the User output to be activated. The command string: A2↓ causes the UO2 output to be set to the logic level "one". The **Activate** command is of the delayed execution type and it occupies 2 memory locations.
Cx	The **Clear** command clears a User output, i.e it forces the logic level to "zero". The command is always followed by an argument whose value ranges between 1 and 3, and that specifies the User output to be cleared. The command string: C3↓ cleares the UO3 output by forcing it to the logic level "zero". The three USER outputs are automatically cleared at power-up. The **Clear** command is of the delayed execution type and it occupies 2 memory locations.
Dvvv	The **Delay** command allows the execution of a delay. The instruction is always followed by an argument whose value ranges between 1 and 255, and that specifies the duration in tenth of sec. of the delay to be executed. The command string: D15↓ causes a 1.5 seconds delay to be executed before the next instruction is considered. The **Delay** command is of the delayed execution type and it occupies 2 memory locations.
E	The **Execute** command starts the execution of the program stored in memory. It is also used to terminate the GS-C200 programming session and no argument is required. The **Execute** command is of the immediate execution type.
F	The **Feedback** command allows the host computer to know whether the controller is ready to receive a command or not. To comply with this request, the GS-C replies by: B↓ (Busy) in case it is executing a program, or: R↓ (Ready) if it is ready to receive a command, or: E5↓ (Error) This latter answer, used only by the GS-C200, indicates that during the program execution the position counter has reached the overflow condition (i.e. > 9999999). The feedback command is of the immediate execution type.
fsxxxxxxx **	The **force** command, executable only by the GS-C200S, allows the user to preset the position counter to the desired value. This command is always followed by the sign and the value of the position that spans from – 8388608 to + 8388607. The **force** command is of the delayed/immediate execution type and it occupies 4 memory locations.
Gxxxxxxx *	The **Goto** command forces the motor to reach the specified target position. This command, executed exclusively by the GS-C200, is always followed by an argument whose value ranges between 0 and 9999999, and it defines the position to be reached. The 0 position coincides with the Home position or with the position where an Initialize command has been sent. The **Goto** command is of the delayed execution type and it occupies 4 memory locations.

Command	Description
Gs *	The "velocity mode" **Goto** command allows to move the motor continuously, i.e. the motor is accelerated to the programmed speed and then it slews indefinitely in the selected direction until a "stop" command is received. The command is always followed by the direction information. The command string : G+↓ move the motor in the clockwise direction while: G–↓ move the motor in the counterclockwise direction. To stop the motor either the Z or the K command can be used. The "velocity mode" **Goto** command is of the delayed execution type and it occupies 4 memory locations.
Gsx *	A further possibility offered by the Goto command, that greatly improves the GS-C200 flexibility, is the "controlled velocity mode" operation. This command is followed by the direction information and by the User input to be tested to stop the operation. This occurs when a "zero" level is applied to the specified User input. For example the command string: G+2↓ causes the motor to ramp to the programmed slew speed and to move at this speed until the UI2 input is brought to "zero". The "controlled velocity mode" **Goto** command is of the delayed execution type and it occupies 4 memory locations.
Gsxxxxxxx **	The Goto command forces the motor to reach the specified target position. This command, executed exclusively by the GS-C200S, is always followed by an argument whose value ranges from – 8388608 and + 8388607, and it defines the position to be reached. The 0 position coincides with the Home position or with the position where an Initialize command has been sent. The **Goto** command is of the delayed execution type and it occupies 4 memory locations.
gs **	The "velocity mode" **Goto** command allows to move the motor continuously, i. e. the motor is accelerated to the programmed speed and then it slews indefinitely in the selected direction until a "stop" command is received. g+1↓ move the motor in the clockwise direction while: g–↓ move the motor in the counterclockwise direction. To stop the motor either the Z or the K command can be used. The "velocity mode" **Goto** command is of the delayed execution type and it occupies 4 memory locations.
gsx **	An additional possibility offered by the **Goto** command, further improving the GS-C200S flexibility, is the "controlled velocity mode" operation. This command is followed by the direction information and by the User input to be tested to stop the operation. This occurs when a "zero" level is applied to the specified User input. For example the command string: gt1↓ causes the motor to ramp to the programmed slew speed and to move at this speed until the UI1 input is brought to "zero". The "controlled velocity mode" **Goto** command is of the delayed execution type and it occupies 4 memory locations.

Command	Description
Hs	The **Home** command allows the GS-C to find the mechanical reference position. The command is followed by the argument that specifies the searching direction of the End Of Travel switch. The argument can be omitted and in such a case the GS-C will execute the command: H+↓ As soon as the GS-C receives the **Home** command, it moves the motor in the selected direction at the Start-Stop speed (defined as the first instruction at the beginning of the program) until the End Of Travel input is brought to "zero". When this condition is reached the direction is reversed and the movement continues until the Home input reaches the "zero" logical level. The position counter is then cleared as well as the program contained in the RAM memory, and the controller is ready to process a new command. In the GS-C200S, the position is also cleared, but the previous program, present in the RAM is saved. When the Home and the End Of Travel inputs are tied toghether the system reference point will correspond to the End Of Travel position. To allow the system homing also in a stand alone application, an **Home** command is automatically executed at start-up after the program recall. The Home direction is defined by the logic state of the RxD input (pin 11) that when unconnected is equivalent to a **H+** command, while when connected to the +5V pin it forces a **H–** command. In a stand-alone environment, when the **Home** command is not needed, it is mandatory to ground the End od Travel and the Home inputs (pins 32 and 30). The **Home** command is of the immediate execution type.
Ix	The **Initialize** command forces the GS-C module to be selectively inizialized. The command is followed by an argument whose value ranges between 1 and 3, and that specifies where the action is addressed according to the following table: 1 = Position counter is cleared 2 = User outputs are cleared 3 = Position counter and User outputs are cleared. The **Initialize** command is used to create a logic Home position for the GS-C200 if the 9999999 steps are not enough for the specific application. This function is better performed by the force command in the GS-C200S, for which it is also possible to insert this command into the program. The **Initialize** command is of the immediate execution type for the GS-C200, while it results of the delayed/immediate execution type for the GS-C200S and it occupies 2 memory locations.
jv **	The **jump** command, executed only by the GS-C200S, allows the user to move inside the program and to repeat indefinitely a portion of the program itself. The argument specifies the memory location to be reached and it ranges from 0 (that is the program starting point) to 118. The **jump** command is of the delayed execution type and it occupies 2 memory locations.
jcv,y **	The **conditional jump** command, executed only by the GS-C200S module, allows the user to move inside the program as a function of the logic state of the User inputs. The argument specifies both the memory location to be reached (**v**), that must range between 0 and 118, and the User input condition to be matched (**y**) in order to execute the **conditional jump.** The following example shows how powerful this command is: jc0,40↓ jc1,52↓ jc2,74↓ When the first command is encountered the module tests the status of the User input pins and if their value is 0 a jump to the memory location 40 is executed. If the condition is not met the jump is not executed and the following instruction is examined, and so on. The **conditional jump** command is of the delayed execution type and it occupies 2 memory locations.
K	The **Kill** command aborts the program execution. The program can be restarted just by issuing the Execute instruction which will start the sequence from the first program instruction and not from the interrupt point; it is therefore advisable to always send a Home instruction after a **Kill** instruction in order to allow the system to start from a known position. The **Kill** command is of the immediate execution type.

Command	Description
Lo	The **Loop start** command marks the memory location where the portion of a repeatedly executed command sequence begins. This command is normally used together with the Loop repetition number command. The **Loop start** command is of the delayed execution type and it occupies 2 memory locations.
Lxxx	The **Loop repetition number** command allows an instruction, a sequence or a whole program to be repeated for the specified number of times. The command must be followed by an argument ranging from 1 to 255, that specifies how many times the portion of the program contained between the Loop start command and the **Loop repetition number** has to be executed. The sequence: L0↓ • • • L10↓ forces the command sequence included between L0 and L10 to be repeated ten times. This command in normally used togheter with the Loop start command. If the loop starting point is not specified, the interpreter repeats the sequence starting from the beginning of the program. The **Loop repetition number** command is of the delayed execution type and it occupies 2 memory locations.
M	The **Memory save** command allows the program currently stored in the RAM memory to be permanently saved in the EEPROM. The program can then be reloaded both automatically or under command. In the first case, it is executed automatically at power on, while in the latter the X command must be issued. The **Memory save** command is of the immediate execution type.
P *	The **Program enter** command sets the GS-C200 in the programming mode and it allows a new program to be entered in the memory. The instruction doesn't require any argument and it causes the cancellation of the program contained in the RAM memory The programming session is terminated by the Execute command. The **Program enter** command is of the immediate execution type.
Po **	The **Program enter** command sets the GS-C200S in the programming mode and it allows a new program to be entered in the memory. The instruction doesn't require any argument and it causes the cancellation of the program contained in the RAM memory. The programming session is terminated either by the program exit or the Execute command. The **Program enter** command is of the immediate execution type.
Px **	The **Program exit** command sets the GS-C200S in the execution mode and it allows the unit to wait for a command. The instruction doesn't require any argument. The **Program exit** command is of the immediate execution type.
Q	The **Query** command instructs the GS-C to send to the Host computer the program currently stored in the RAM memory. Every program instruction is separated by a carriage return (ASCII 13), and the program end is evidenced by the transmission of a message "END" that is the sequence terminator and it must be recognized by the Host. The instruction does not require any argument. The **Query** command is of the immediate execution type.

Command	Description
Rvvv	The **Ramp** command allows the user to define the length of the acceleration and deceleration ramps that are always identical. The command is followed by an argument whose value ranges from 1 to 999 and it determines the number of steps necessary to pass from the Start-Stop speed to Slew speed. The instruction: R50↓ specifies an acceleration or deceleration ramp 50 steps long. When the number of steps to be executed is lower than the length of the two ramps (acceleration and deceleration), the ramping is reversed before the maximum speed is reached to guarantee the correctness of the final position. More than one ramp length can be used during the program execution just by introducing an R command in the proper sequence place. R25↓ 3000↓ • • R85↓ –800↓ • This program executes a 25 steps ramp length for the movements until the R85 command is encountered; from that moment all the movements are executed with a 85 steps ramp length. This feature allows the user to optimize the motion system to adapt for different friction and load conditions. The **Ramp** command is of the delayed execution type and it occupies 4 memory locations.
Svvv	The **Start-Stop** command allows the user to choose the step rate at which the motion is started. The command is always followed by an argument whose value ranges between 1 and 1000 and it corresponds to a **Start-Stop** step rate of 10 to 10,000 steps/second (a by 10 multiplier is used). The range normally used is from 1 to 50 corresponding to a 10 to 500 steps/second rate. The command: S30↓ indicates a 300 step/sec or 300Hz Start-Stop frequency. A **Start-Stop** command must initiate any program to be executed in stand alone environment. More than one **Start-Stop** rate can be used during the program execution just by introducing a new **Start-Stop** command when needed, as shown in the following program sequence: S20↓ T200↓ • • S35↓ • T300↓ • The **Start-Stop** command is of the delayed execution type and it occupies 4 memory locations.
Tvvv	The **Top-speed** command allows the user to choose the motion system Slew speed. The command is always followed by an argument whose value ranges between 1 and 1000 that correspond to a **Top-speed** step rate of 10 to 10000 steps/second (a by 10 multiplier is used). The range normally used is from 30 to 500, corresponding to a 300 to 5000 steps/second rate. The command: T300 indicates a 3000 steps/sec or 3kHz rate (equivalent to 900 turns/minute for a motor with 200 steps/turn). More than one **Top-speed** rate can be used during the program execution just by introducing a new **Top-speed** command in the proper sequence place as per the example reported in the Start-stop speed command description. The **Top-speed** command is of the delayed execution type and it occupies 4 memory locations.

Command	Description
Ux	The **Until** command allows the program currently stored in RAM memory to be continuously executed until a specific USER input is brought to "zero". The command is always followed by an argument whose value ranges between 1 and 3, and it specifies the User input to be tested. The command: U2↓ states that the program, once started, will be continuously executed as long as the User input UI2 is at the logic level "one". Just after User Input UI2 is set to "zero", the program processes the next command after U2. The **Until** command is of the delayed execution type and it occupies 2 memory locations.
Vx	The **Verify** command allows the Host to know the current absolute position of the motor versus the Home position or the status of the USER inputs and outputs. The instruction is always followed by an argument whose value, 1 or 2, specifies the type of requested information. The request for the current absolute position is obtained by issuing the instruction: V1↓ the GC-C200 answer can be 1234567↓ while the GS-C200S answer can be: +1234↓ The request of the USER outputs status is obtained by using the instruction: V2↓ the GS-C answer can be: 25↓ that denotes the following Input/Output status: UI1 = 0 UO1 = 1 UI2 = 1 UO2 = 0 UI3 = 0 UO1 = 1 2 5 The **Verify** command is of the immediate execution type.
X	The **eXchange** command allows the user to transfer the program currently stored in the EEPROM into the RAM. This command is used either during the program debugging phase when the F.A.S.T. program is utilized, or when the fast execution of a frequently used program is needed. In this latter case the Host recalls the program from the EEPROM by simply issuing the following command string: E↓ X↓ The **eXchange** command is of the immediate execution type.
Wx	The **Wait-for** command allows the program start or a portion of program execution to be conditioned by the rising edge of an external signal applied to the a USER input. The command is always followed by an argument whose value ranges between 1 and 3, and it specifies the User input to be tested in order to conditions the next command execution. The instruction: W2↓ states that the program execution is conditioned by the presence of a "one" logic level at the User Input UI2. The **Wait-for** command is of the delayed execution type and it occupies 2 memory locations.

Command	Description
Z	The **Zero the speed** command allows a smooth stop of the motion system. When the GS-C receives this command it reduces the stepping rate to "zero" through a deceleration ramp and it stops the program execution. If there is no motion when activated, the program execution is immediately stopped. By using this command it is possible to stop the motor still maintaining trace of the system position. The program can be subsequentely restarted through an E command.
±XXXXXX	The **incremental positioning** command allows the user to perform a movement referenced to the actual position. The command can be issued either with a + or – sign that defines the direction of the motion, and it is followed by an argument ranging from 1 and 999999 that defines the number of steps to be executed. The **Incremental position** command can be mixed to the Goto absolute positioning command in a program, and it is normally used in a subroutine. The **Incremental position** command is of the delayed execution type and it occupies 4 memory locations.

During the program execution, the GS-C accepts only the **F**, **Z** and **K** commands. Any other command sent to the GS-C during the program execution has no effect, and the module will respond to the Host Computer by sending the answer B (Busy).

The GS-C200S programming requires a specific attention because, when a program includes a jump command, it is mandatory to address the proper memory position to correctly execute the sequence.

For this purpose it is mandatory to define the jump memory location by adding, for each program instruction, the proper bytes length that is specified in the command description. The program starts from memory address 0.

THE PROGRAM STORAGE AREA

The GS-C contains two storage areas reserved to the User. The first is the microprocessor Random Access Memory from where the motion program is executed, the second is an EEPROM where the programs are saved. The EEPROM contains a program or a command sequence programmed by the user that can be transferred into the RAM memory by using the X command.

The RAM contains either a program or a command sequence sent by the Host computer or transferred from the EEPROM. In any case the program that is executed when an E or Goto command is issued. is the one contained in the RAM.

If the program is sent by the Host, it is checked to verify if the logical and physical correctness has been respected and if the storage capability is not exceeded. In case an error is detected, it is notified to the Host through an appropriated error message.

The number of instructions that can be stored depends on the type of instruction, and typically it ranges between 30 and 60, for a total of 119 memory locations.

THE POWER SUPPLY

The GS-C module contains a high efficiency switch mode power supply. It generates the various regulated voltages required for the proper operation of the internal logic and the communication port, starting from an unregulated input voltage that can range from 12 to 40 Volt. The module also features a 5V output capable of delivering up to 100mA, which can be used to supply external devices or the logic port of a GS-D module. This output is protected against short circuit to ground. Two outputs at ±12V are available with a current capacity of 10mA.

PROGRAM EXAMPLES

After the description of the communication protocol, of the various commands and of the various messages, some simple programs examples are given in the following.

Example 1

The required action is to run a motor at 1000 steps/sec. rate, with a start-stop rate of 100 steps/sec., and a ramp length of 50 steps. The target position to be reached is the step 500000.

The operative sequence is the following:

1) Connect the GS-C200 to an Host Computer equipped with the advanced Basic program.
2) Power-on the GS-C200.
3) Enter the DOS operating system and then run the F.A.S.T. program (see the **GS-C200PROG** datasheet).
4) Start the programming session by typing the following command sequence:

F↓	Read the controller status. A Ready is answered by the GS-C.
I3↓	Clear the position counter and the USER outputs.

P↓	Enter the programming mode
S10↓	Set the Start-stop rate to 100 steps/sec.
T100↓	Set the Slew speed rate to 1000 steps/sec.
R50↓	Set the Ramp length to 50 steps.
G500000↓	Goto the target position
E↓	End of the programming session. The GS-C starts the program execution.

The G500000 command can be substituted by the +500000 command. The program can also be stored in the GS-C EEPROM by typing an M↓ command before the E↓ command.

Example 2

The program chosen for this example drills 5 equidistant holes on a metal bar. A GS-C and GS-D motion system is used to control the vertical position of the drill, while a second GS-C and GS-D motion system is used for the proper bar loading and positioning. To better clarify the operations to be executed and to show the program simplicity, the two command sequences and the relative process flowcharts are also reported.

The programming session is entered following the points 1 to 4 of the previous example. The first command sequence, used to correctly position the metal bar, is the following:

S10↓	Set the Start-stop speed to 100 steps/sec
T100↓	Set the Slew speed to 1000 steps/sec
R40↓	Set the ramp length to 40 steps
W1↓	Wait for the external Start
+250↓	Reach the first drilling position
L0↓	Loop starting point
A2↓	Activate the unit 2 forcing UO2 = 1
D1↓	Wait 0.1 sec
C2↓	Then reset UO2
W2↓	Wait until drilling completion
+120↓	Reach the drilling position 120 steps CW
L4↓	Repeat the loop 4 times
A2↓	Activate the unit 2 forcing UO2 = 1
C2↓	Then reset UO2
W2↓	Wait until drilling completion
+250↓	Reach the cutting position 250 steps CW
A1↓	Activate the cutting blade forcing UO1 = 1
D5↓	Wait 0.5 sec
C1↓	Clear cutting command resetting UO1

The second command sequence, used to drill the metal bar, is the following:

S15↓	Set the Start-stop rate to 150 steps/sec
T200↓	Set the Slew rate to 200 steps/sec
R25↓	Set the Ramp length to 25 steps
W1↓	Wait for start
W2↓	Wait for a drilling command from unit 1
A2↓	Activate the drill motor forcing UO2 = 1
+150↓	Pull down the drill
D1↓	Wait 0.1 sec
G0↓	Lift the drill up
C2↓	Stop the drill motor
A1↓	Notify drilling completion to unit 1 forcing UO1 = 1
D1↓	Wait 0.1 sec
C1↓	Then clear UO1

The combination of these two programs operates only on one bar, then the two GS-C become available again to the Host both for the repetition of the program or for the entering of a new command sequence.

If the operation has to be repeated till the exhaustion of bars, it will be sufficient to add, at the beginning of the first sequence, the command;

U3↓ execute until UI3 = 1

which allows the drilling cycle to continue until the controller which takes care of the bar positioning, is notified to stop the operations.

This notification is accomplished by clearing the User input UI3 of GS-C devoted to the positioning.

To demonstrate the efficiency of the GS-C programming language it is worth to mention that the program for the bar positioning uses 50 memory locations, while the program for the drill control needs only 36 memory locations. The two programs can be contained in the GS-C memory thus making the system simpler and easier to maintain.

Figure 8. Automatic Drilling And Positioning System Block Diagram.

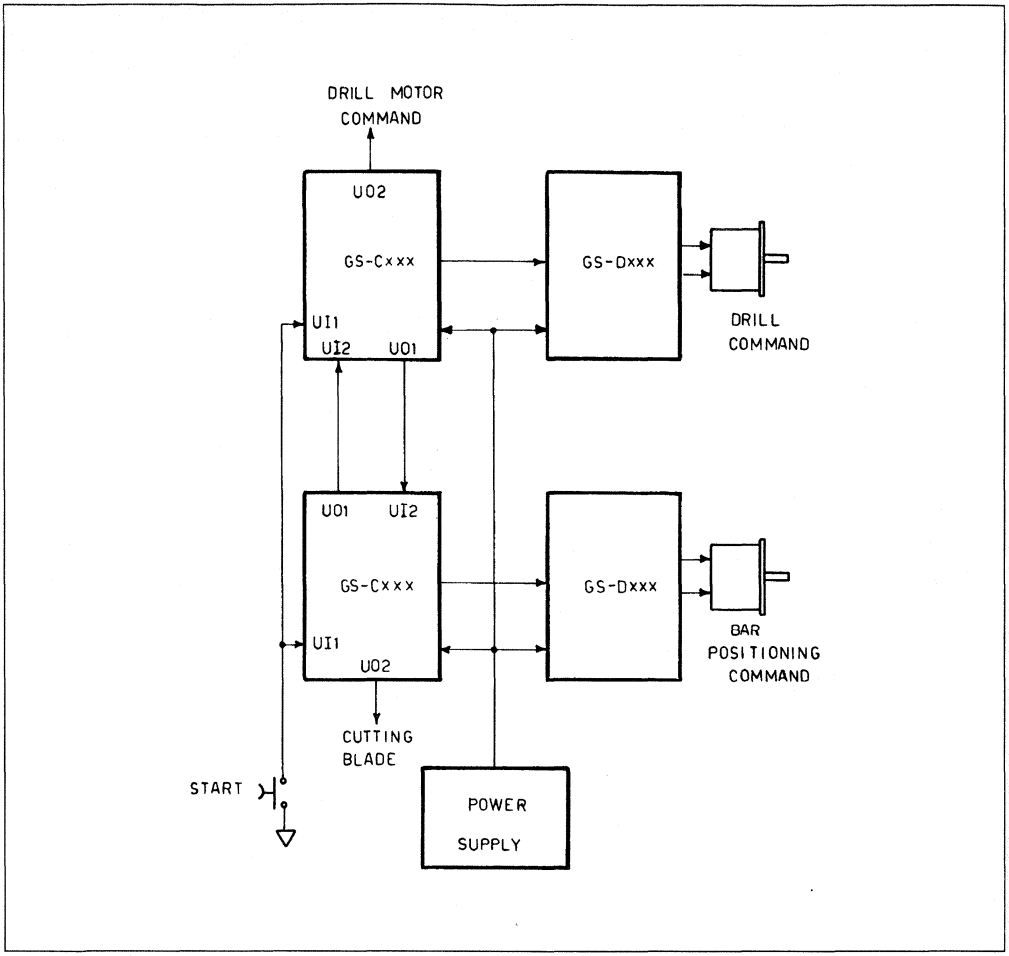
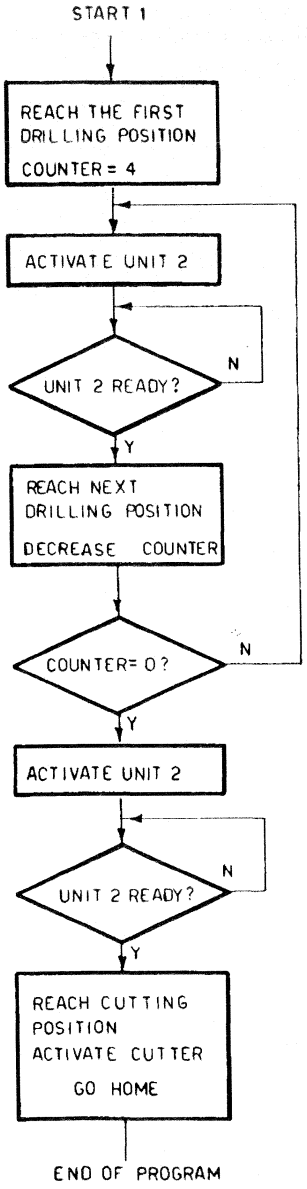
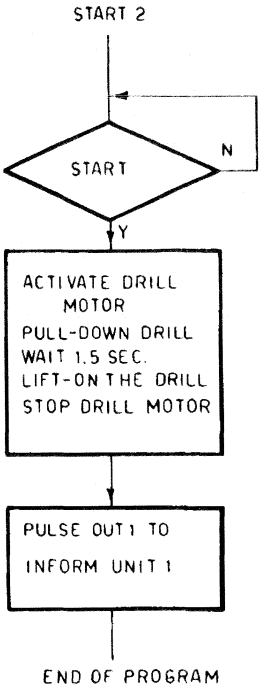


Figure 9. Programs Flow-charts.





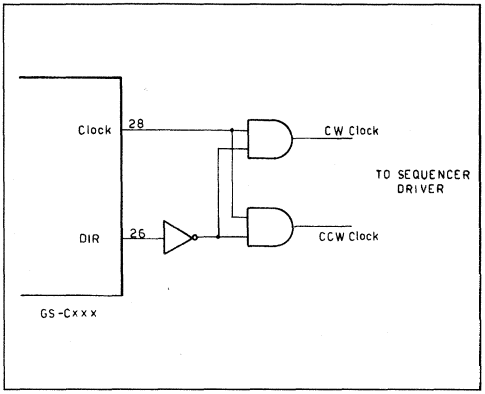
GS-C200 AND GS-C200S APPLICATION

THE SEQUENCER-DRIVER INTERFACE

The GS-C is a general purpose stepper motor controller capable to drive any type of motor, i.e. two, three and five phases motors, by just interfacing it to the right Sequencer-Driver.

Sometime the available Sequencer-Driver requires two separate Clock lines, one for each direction, and this requirement is easily fulfilled by the circuit of figure 10.

Figure 10. Alternative Sequencer-Driver driving.



PHASE CURRENT PROGRAMMING

As already explained, the possibility to modify the phase current of a stepper motor according to different operating conditions, gives substantial improvements in term of efficiency and system reliability because it minimizes the resonance effects and the dissipated power.

The phase current programming can be implemented in various modes, either via a software command by changing the status of the USER output lines, or by hardware. Of course, the Sequencer-Driver must have the current programming capability. An example of a hardware solution, implemented around a GS-C and GS-D200/200S module, is shown in fig.11.

The application utilizes the two outputs:

MOV	Movement in execution output (pin 22)
RAMP	Ramp in execution (pin 23)

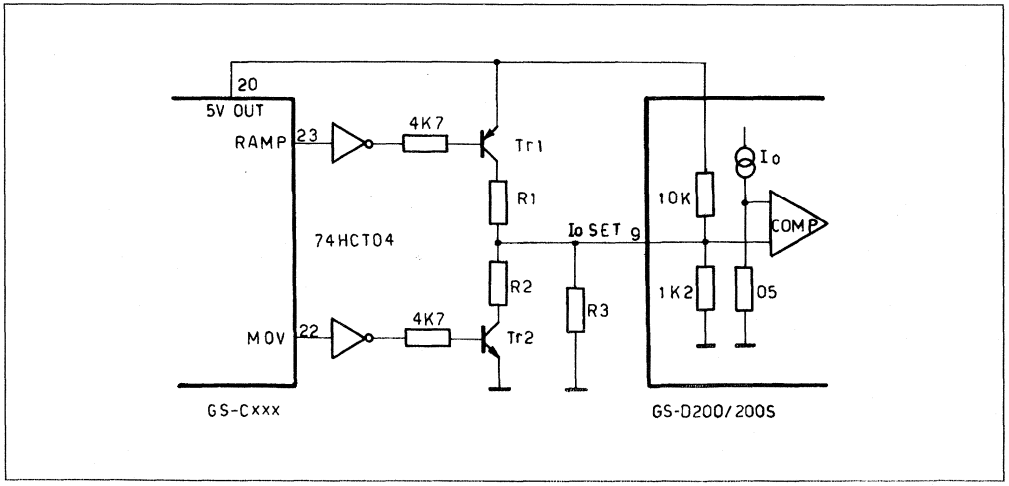
of the GS-C module and the

I_{oset}	Current programming input (pin 9)

of the GS-D module.

The phase current has the shape shown in fig.6, i.e. it is minimized when the motor is stopped, it has its maximum value during the acceleration/deceleration ramps, and an intermediate value during the slew phase.

Figure 11. Phase Current Programming of the GS-D200/200S



Let's assume the following values are needed:

I_{rest} = 0.25A

I_{ramp} = 1.5A

I_{slew} = 0.5A

The logic condition of the RAMP and MOV outputs in the various states is:

During the ramping phase both pins 22 and 23 are high: Tr1 is ON and Tr2 is OFF.

During the slew phase pin 23 is low and pin 22 is high: Tr1 and Tr2 are OFF.

In stall condition Tr1 is OFF and Tr2 is ON.

The value of R1, R2, R3 is determined as follows (for further details please see the GS-D200/200S data sheet). The value of R3, that fixes the I_{slew} = = 0.5A (Tr1 and Tr2 OFF), is easily calculated by referring to the GS-D data sheet:

$$R3 = \frac{I_{slew}}{1 - 0.933 \cdot I_{slew}}$$

$$R3 = 937\ \Omega$$

The value of the R2 resistor, when paralleled to R3, fixes the value of I_{rest} = 0.25A (Tr1 OFF, Tr2 ON).

$$R2 \,//\, R3 = \frac{I_{rest}}{1 - 0.933 \cdot I_{rest}}$$

$$R2 \,//\, R3 = 326\Omega$$

$$R2 = 500\Omega$$

The value of R1, that depends on the value of R3 and the resistors contained in the GS-D200/200S module, fixes I_{ramp} = 1.5A (Tr1 ON, Tr2 OFF).

The values of the internal resistors are:

1.2kΩ to ground and 10kΩ to V_{SS} for the GS-D200

750Ω to ground and 10kΩ to V_{SS} for the GS-D200S

Assuming the GS-D200S is used, after some straightforward calculations, it results:

$$R1 = 4245\Omega$$

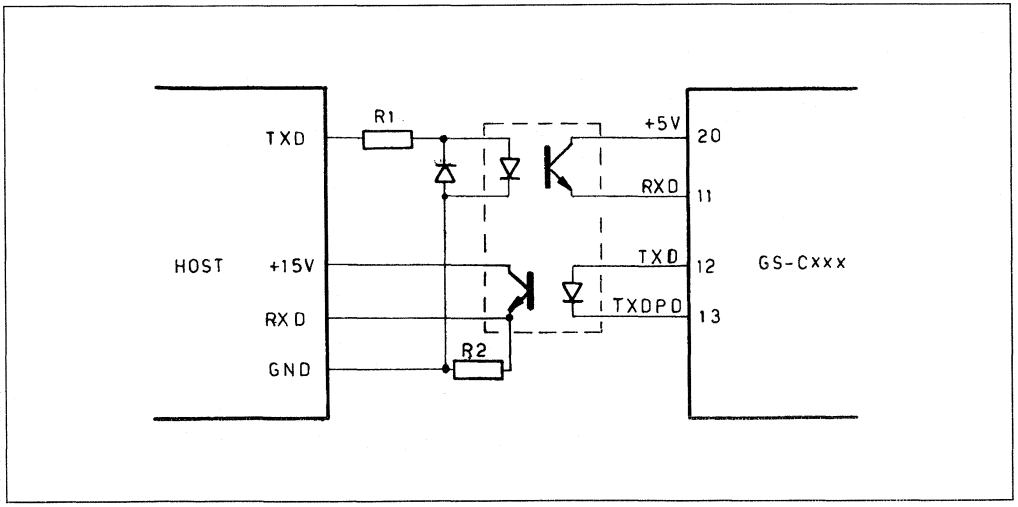
of course all these values do not take into account the transistors saturation losses and in some cases, when a very precise current is needed, a trimming is required.

GALVANIC ISOLATION

The industrial environment, where normally a stepper motor and its driving system operate, is very noisy and for this reason it is often advisable to have a galvanic isolation between the Host computer and the motion system. Because the connection between the Host and the GS-C module requires only three wires (TxD, RxD and ground), the galvanic isolation can be implemented as per fig. 12 that uses only two optocouplers and two resistors, one protection diode and a +12 or +15V source.

A +12 or +15V source is normally available on the pin 6 and 8 of any RS232 connector. The source impedance is quite high (in the range of 220 to 600Ω) and for this reason the value of R2 must be greater than 1000Ω to avoid the source overload.

Figure 12. GS-C200 to Host galvanic isolation.



COMPLEX MOVEMENTS SYNCHRONIZATION

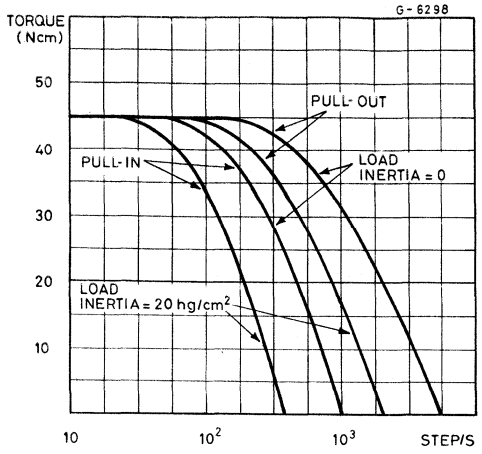
In many applications the synchronization of several movements is quite often required and the GS-C allows this function to be easily implemented either by using the Step Enable input or the User input/output pins. In fig.13A and fig.13B the block diagrams relative to the two solutions are reported.

The solution **A** is the simplest but it has some limitations, i.e. it can be used only when the whole system has to move synchronously. The solution **B** is more complex but also more flexible and it allows the program to control where and when the synchronization must be implemented.

THE START-STOP SPEED (S command) SELECTION

A typical Start-Stop curve (as shown on Fig. 14), shows that for a given driving voltage and phase current, the highest drive frequency allowed at the start (Pull-In Rate) is much lower than the one allowed for the stop (Pull-Out Rate) and that both are influenced by the load value. Of course the higher the current level the higher is the available torque, and the system can be started at a greater speed. A significant increase of the start-stop speed is obtained when the supply voltage is increased but in both cases the problem related to the mechanical resonance must be considered. It is advisable to maintain a significant safety margin against the system torque limit in order to avoid any problem due to the friction variation. A commonly accepted rule fixes the Start-Stop speed equal to the 50% of the maximum theoretical value reported on the motor data sheet; this takes into account friction, load inertia variations as well as motor parameter differences and power supply fluctuations.

Figure 14. Start-Stop Characteristic.



SLEW SPEED (T command) SELECTION

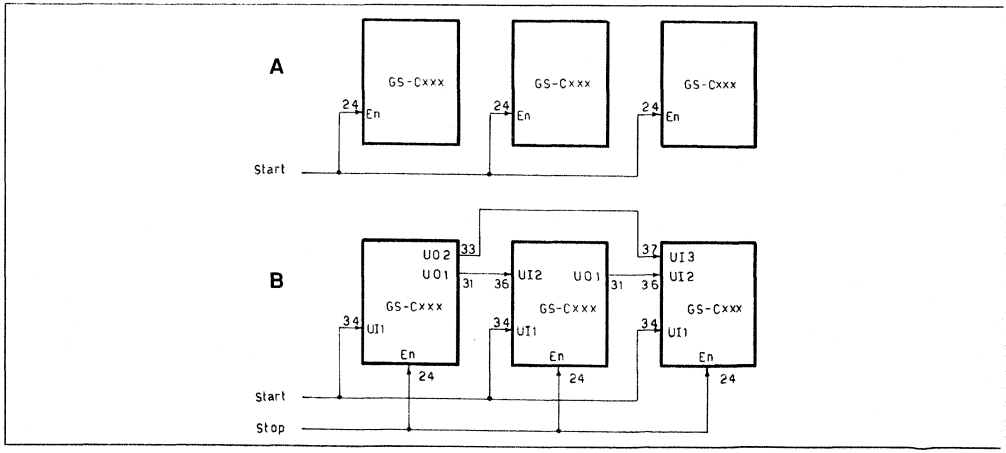
The Slew speed is roughly determined by the load and it can be evaluated by using the following relation:

$$\frac{F \cdot L}{6000 \cdot t} = \frac{T \cdot N}{10}$$

where

F = Strength in Pounds
T = Torque in Ounce/Inch

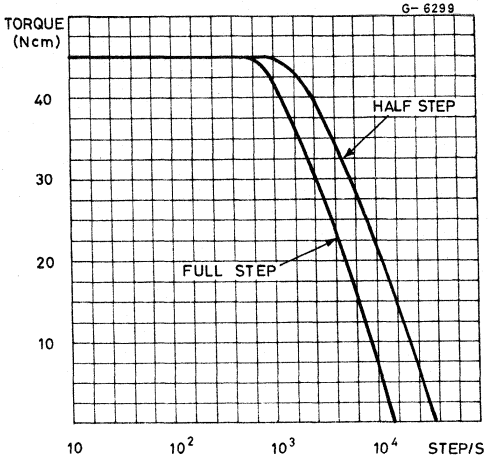
Figure 13. Complex Movements Synchronization



L = Length in Inches
N = Speed in turn/min.
t = Time in seconds

The Slew speed is also limited by the motor electrical and physical characteristics, as shown on Fig. 15 where the behaviour of the minimum available torque versus the driving frequency is reported.

Figure 15. Torque/Frequency Characteristic.

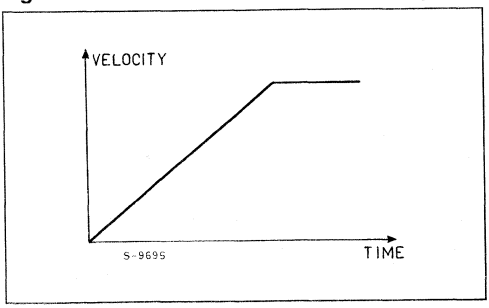


It can be noted that the torque decreases almost linearly starting from a certain frequency, and this frequency depends on the motor windings impedance and the rotor inertia.

RAMP LENGHT (R command) SELECTION

The acceleration and deceleration ramps are not likely to be calculated and they shall be optimized during the system debugging and testing phase. The testing may start with very conservative ramp gradients, i.e. very long ramps, that will be gradually shortened until the first positioning error is detected.

Figure 16. The GS-C200 Acceleration Ramp.



The acceleration and deceleration ramps generated by the GS-C have the trend shown in fig. 16.

It is important to note that, when the number of steps to be executed does not allow to reach the Slew speed, the GS-C moves to the target position performing a partial acceleration ramp linked to a shortened deceleration ramp. This represents the minimum time consuming way to reach the specified position.

CLOSED LOOP OPERATION

The stepper motor is a device normally driven in an open loop mode and there is no direct control between the cause and the effect. In adverse conditions an issued step may not be performed mechanically because the driving conditions do not match the required torque and speed. In addition, the resonance phenomenon, common to all the stepper motors, can also affect the correct positioning.

In some particular applications, when the load has a very large spread of values and the torque margin is limited, it is sometimes necessary to implement an external electronic circuitry to guarantee the correct system positioning

To this purpose three different methods can be adopted:

a) Digital encoding of the absolute position.

b) Recognition that a step has been executed by the usage of a slotted disk, two optocouplers and some logic.

c) The same as above by the usage of velocity coils and some logic.

The first solution is very expensive and the digitalized position value must be read by the computer through a parallel port by using a specifically written program. A further limitation arises from the fact that every shaft encoder provides just the information relative to the position but it does not take care if more than one turn has been performed by the motor shaft, and an external logic is also required to detect and save this condition.

The second solution is less expensive but it requires a tedious trimming of the mechanical positioning of the optical sources and detectors to be effective. The major drawback of this solution is its sensitivity to dust, and the whole position sensing system must be contained in a dust free box.

The last solution is probably the best under every point of view because it does not require any

In fig. 17 the block diagram of a closed loop system is reported.

If the step execution is recognized by a movement detector that uses either a slotted disk or the motor velocity coils, two logic signals (x,y) like those reported in fig. 18 are available.

It is possible, by using these two signals as inputs (x, y) of the very simple and inexpensive logic circuit reported in fig. 19, to detect the direction of rotation and the step execution. The output of the circuit is then used to condition the step enable input of the GS-C module allowing the step clock pulse to be issued only if the previous step has been executed.

Figure 17. Closed Loop System.

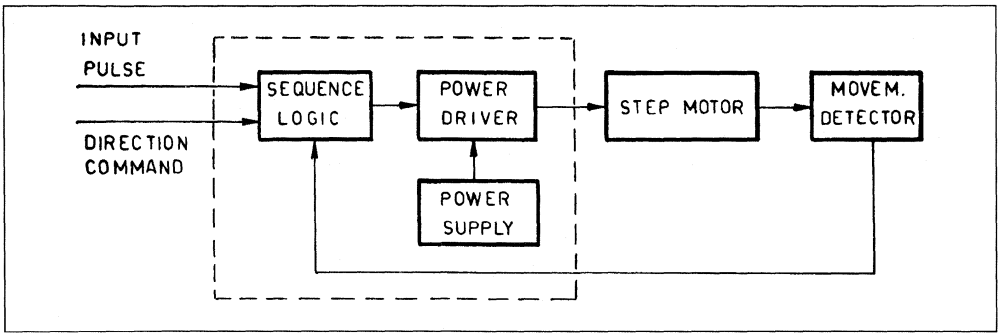


Figure 18. Signal Output of the Movement Detector.

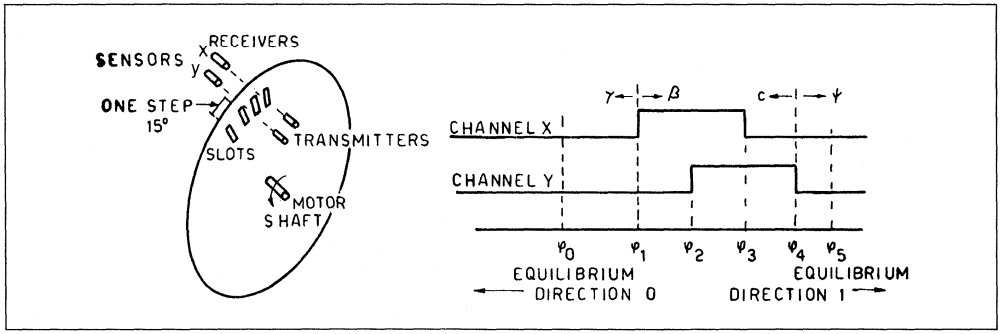
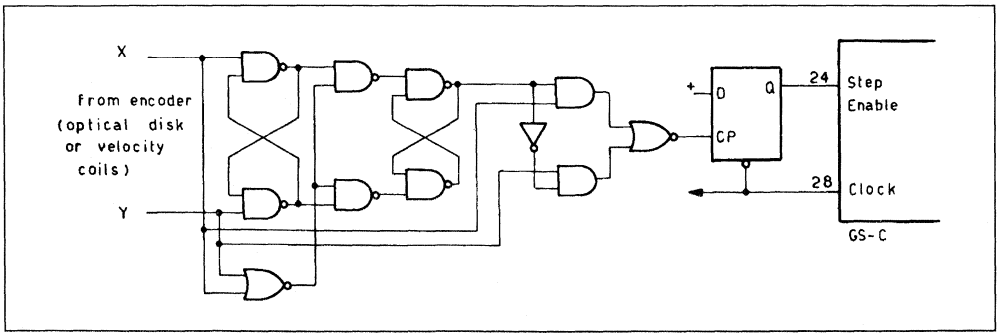


Figure 19. Suggested Logic to Close the Loop.



and the step execution. The output of the circuit is then used to condition the step enable input of the GS-C module allowing the step clock pulse to be issued only if the previous step has been executed.

ELECTRONIC DAMPING

Any stepper motor system when driven at very low stepping rates, has an oscillatory step response as shown in fig. 20.

This oscillatory behaviour is due to fact that the motor reaches the stall position after each excitation change through an acceleration and a successive deceleration. This causes the motor shaft to rotate with jumps instead of uniform motion.

Another consequence of this oscillatory single step response is that the long system settling time can cause mechanical stresses to the driven load.

A second tedious effect is the enhancement of the rotor oscillation when the driving step rate approaches the natural resonance frequency of the motor. If the step rate is lower than this frequency, the motor is behind the equilibrium position and the velocity is near to zero when the next excitation change occurs.

When the step rate is increased to a value close to the natural resonance frequency, an increase of the oscillations also occurs, and as soon as the oscillation amplitude exceeds the step amplitude, the corrispondence between the rotor position and the excitation sequence is lost and any subsequent rotor movement is erratic as shown in fig. 21.

A simple method to reduce the oscillations problem is to use the half step driving, but this also limits the maximum speed of the system.

Figure 21. Slow Speed Step Response.

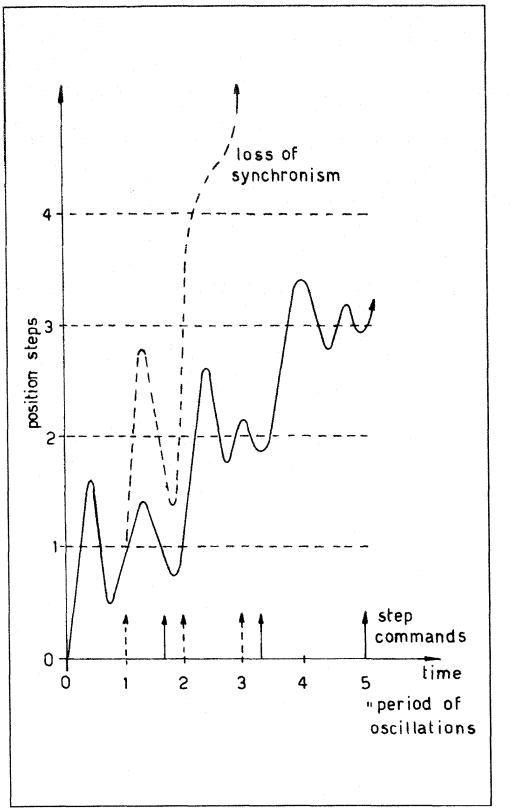
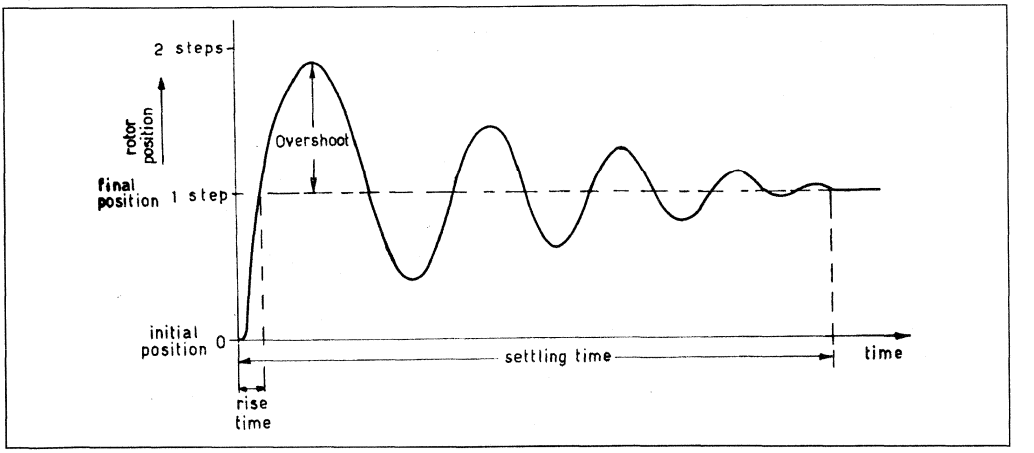


Figure 20. Typical Single Step Response.



When this limitation is not acceptable, other two basic techniques may be adopted to damp the system oscillations:

1. A mechanical damper
2. An electronic damping circuit.

The mechanical damping is obtained by the introduction of a viscous friction between the motor shaft and the load. The friction system must be elastic and it will recover the original relative angular shaft alignement to assure the correct final positioning.

The response time of the damping system must be quite fast, and it must be active just for rapid speed changes otherwise a severe limitation in the maximum speed will occur.

The electronic damping is obtained by the proper driving of the motor phases that are switched on and off in such a way to generated a negative torque to decelerate and stop the rotor smoothly. Let's assume the motor is moving from position 1 to the detent position 2, i.e. the phase A is switched OFF and the phase B is switched ON.

The rotor starts moving at t_0 instant (see fig. 22), and after a time t_1, the phase driving is reversed (phase A ON and phase B OFF) generating a braking torque that will allow the rotor to approach the final detent position at a very limited speed. Before the zero speed is reached, (t_2) it is necessary to switch back the phase driving to its original condition in order to stop the system at its target position.

Leaving the phase driving unchanged will cause the motor to stop a step earlier of the correct position because the motor, after the zero speed is reached, will accelerate in the reverse direction returning to the starting position.

The deceleration time as well the damping level is easily adjusted by changing the timing i.e. t_1 and t_2, but it can be quite complicate to compensate a system where large load variation occurs.

In fact, an heavy load variation causes a large variation of the single step response time of the system, and it could be that a system compensated in a no load condition will stop one step behind when fully loaded, while another compensated at full load will probably exibits erratic positioning at no load.

If the load condition is known it is possible to introduce a compensation circuit that can be conveniently driven by one or more User outputs. Fig. 22 shows the motor response to a single step pulse with electronic damping and the relative phase driving. This phase switching reversal method is also known as the bang-bang damping method, and it can be easily implemented by using the GS-C module.

The RAMP and MOV signals allow the user to detect when the last pulses are issued, and to generate, by a simple logic circuit, the delayed phase reversal commands necessary to implement the sequence of fig. 23.

The circuit uses a last pulse detector (G1), and on the falling edge of the A signal (synchronous to the last step command), a timing generator is triggered. The various delays can be trimmed to the values requested by the operating conditions, and the pulse sequence reported in figure 23 (A, B and C signals) in generated.

Figure 22. Single Step Response with Damping.

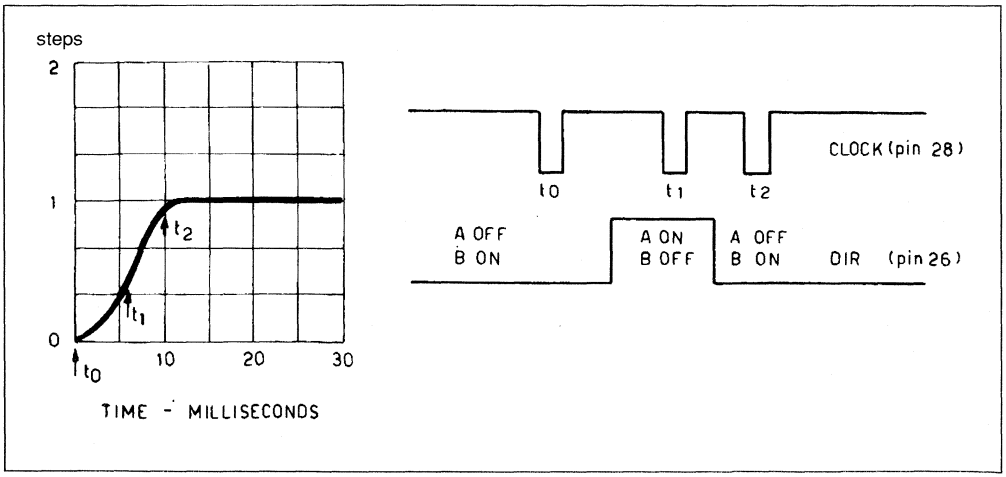
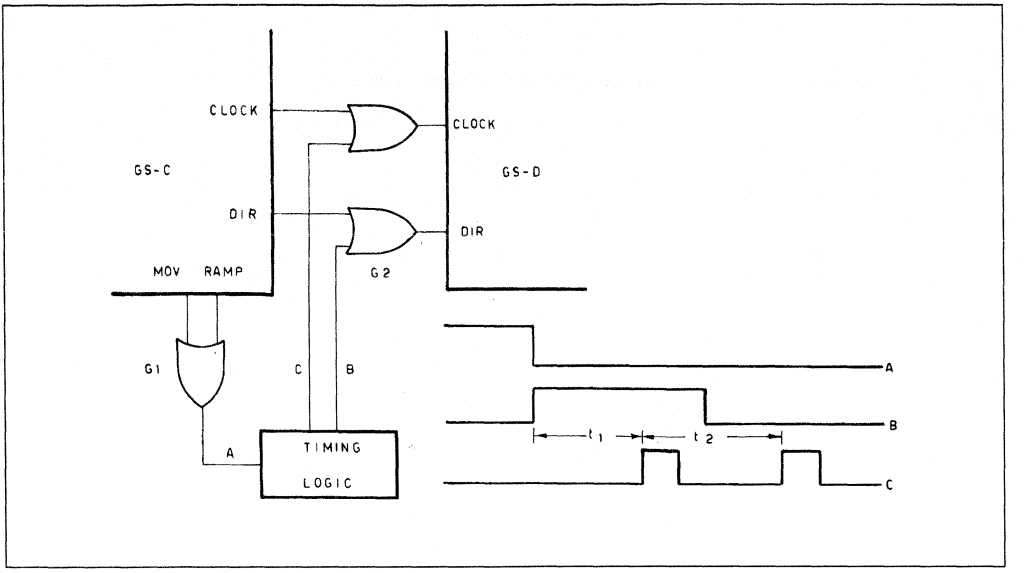


Figure 23. Practical Implementation of the Phase Reversal Damping with the GS-C Module.



SGS-THOMSON MICROELECTRONICS

GS-C200PROG

SOFTWARE PROGRAM FOR STEPPING MOTOR CONTROLLERS

The GS-C200PROG is a software package developed to speed up the knowledge of the GS-C200 and GS-C200S stepper motor intelligent controllers and to help the system motion designer in the program writing and application debugging phase.

This software package runs on every P.C. equipped with a RS-232 serial communication port and the advanced BASIC or GWBASIC interpreter.

The GS-C200PROG is released on a 5" floppy disk that contains six different programs:

FAST.BAS

FAST1.BAS

FASTC.BAS

FASTS.BAS

FAST1S.BAS

FASTCS.BAS

The first three programs are to be used with the GS-C200 controller while the last three ones are for the GS-C200S.

GS-C200PROG DESCRIPTION

The **FAST.BAS** and the **FASTS.BAS** programs are suitable for a black and white video terminal. They allow the complete control of the driven unit (GS-C modules) because they feedback to the user the status (free/busy), the current position and I/O level to ease the debugging phase.
The **FASTC.BAS** and the **FASTCS.BAS** are similar to the above two ones, but they are suitable for a color video terminal. The various screen colors address the programmer to easily find the various commands and to further simplify his/her job.
The **FAST1.BAS** and the **FAST1S.BAS** are equivalent to the first ones, but the status feedback capability is excluded. This allows the user to exactly evaluate the program execution time. In fact the status feedback uses some of the controller time to communicate to the Host the current status.

Programs Loading

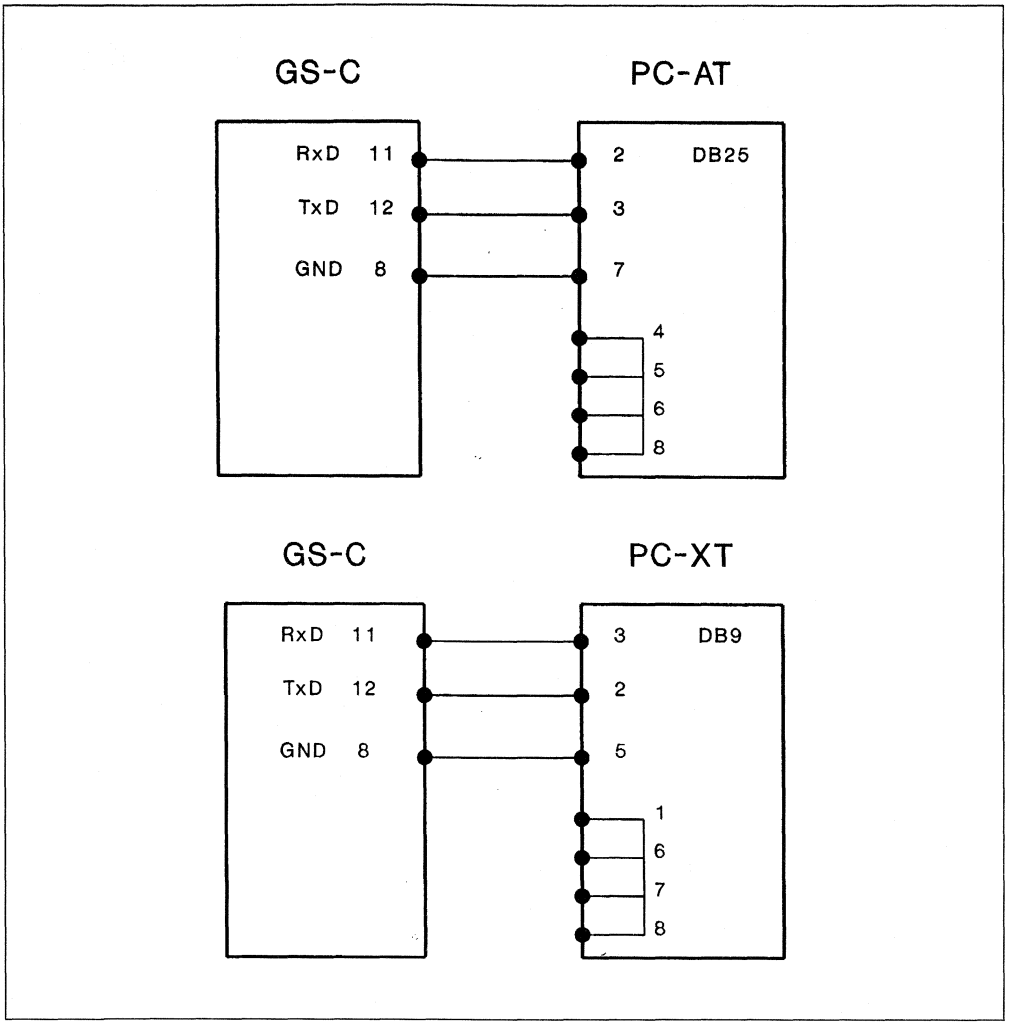
The **GS-C200PROG** must be used in conjunction with a GS-C200 or GS-C200S controller and a sequencer driver such as the GS-D200, GS-D200S, GS-D350M and GS-D550.

The various programs can be loaded by using the following operative sequence:

1) Connect the GS-C communication port to the RS232 port of the P.C. by using an appropriate cable.
2) Select the 4800 Baud communication speed by grounding BR1 and BR2 pins of the GS-C modules.
3) Verify the checksum character is excluded (pin 7 grounded).
4) Check the Selection pins are all open (point to point protocol selected).
5) Connect the GS-C to the Sequencer-Driver.
6) Switch on the P.C. and load the operating system.
7) Insert the GS-C200PROG disk in the floppy drive.
8) Load the advanced Basic interpreter.
9) Load the required FAST program.
10) Switch the motion sytem power on.
11) Run the program.

The cable to interconnect the GS-C to the P.C. must be wired in a different way if the P.C. is of the XT or the AT type. The cable connections are reported in fig. 1.

Figure 1. GS-C to P.C. Connecting Cable



When the used controller is the GS-C200, the programs to be loaded are **FAST.BAS** ot **FAST1.BAS** or **FASTC.BAS**.

The first video mask on the screen is as shown in fig. 2.

Figure 2. GS-C200PROG FAST.BAS Video Mask

```
**********************************************************
*                                                        *
*                      F. A. S. T.                       *
*                                                        *
*          First Advanced Stepper Training program       *
*                                                        *
*                                                        *
*                      Copyright 1988                    *
*                                                        *
*              SGS-THOMSON  Smemiconductors              *
*                                                        *
*                                                        *
*                   S.E.R.F.  Division                   *
*                                                        *
*                                                 V.3    *
**********************************************************

          < Caps lock > and type any key to continue :
```

By typing any key, the video mask of fig. 3 will appear on the screen.

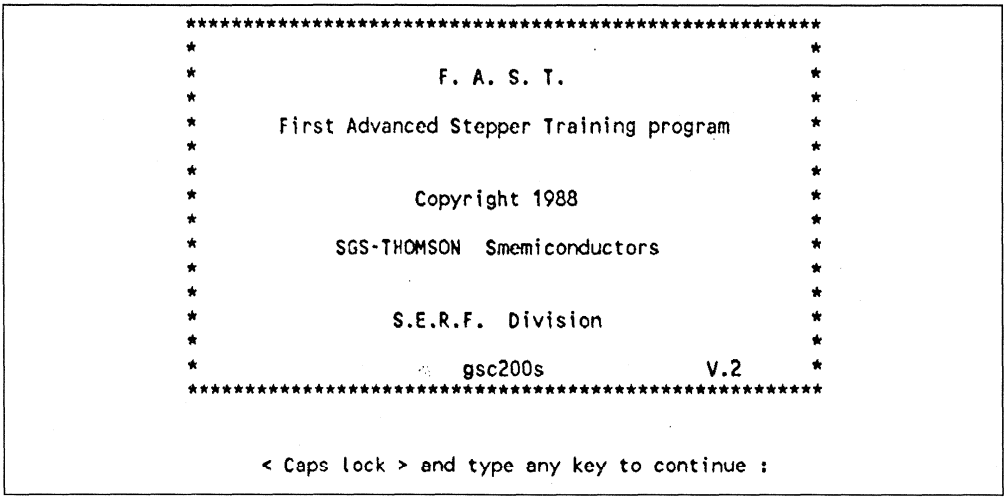
Figure 3. GS-C200PROG FAST.BAS Video Mask

```
                          STEPPER MOTOR COMMANDS
T (1-1000) = TOP SPEED                  D (1-255)  = DELAY
S (1-1000) = START SPEED                L (1-255)  = LOOP
R (1-999)  = RAMP                       A (1-3)    = ACTIVATE OUTPUT
V 91-20    = VERIFY                     C (1-3)    = CLEAR OUTPUT
H (+/-)    = HOME                       W (1-3)    = WAIT FOR INPUT
I (1-3)    = INITIALIZE                 U (1-3)    = UNTIL INPUT
F = FEEDBACK      P = PROGRAM           + (1-999999)  = INCREMENTAL +
Q = LISTING                             - (1-999999)  = INCREMENTAL -
K = KILL          E = EXECUTE           G (0-9999999) = ABSOLUTE
Z = SOFT HALT     J = EDITOR            G (+/-) = VELOCITY MODE
M = STORE PROG.   X = REC. FROM PROG.   G [+/-(1-3)] = VE.MODE TEST INP

       STATUS : FREE            POSITION : 0            I/O : 000 / 000

COMMAND :
```

The user can now start the commands entering or editing an already existing program.
For the meaning of various commands, see the GS-C200/GS-C200S data sheet.
When the used controller is the GS-C200S, the programs to be loaded are **FASTS.BAS** or **FAST1S.BAS** or **FASTCS.BAS**.

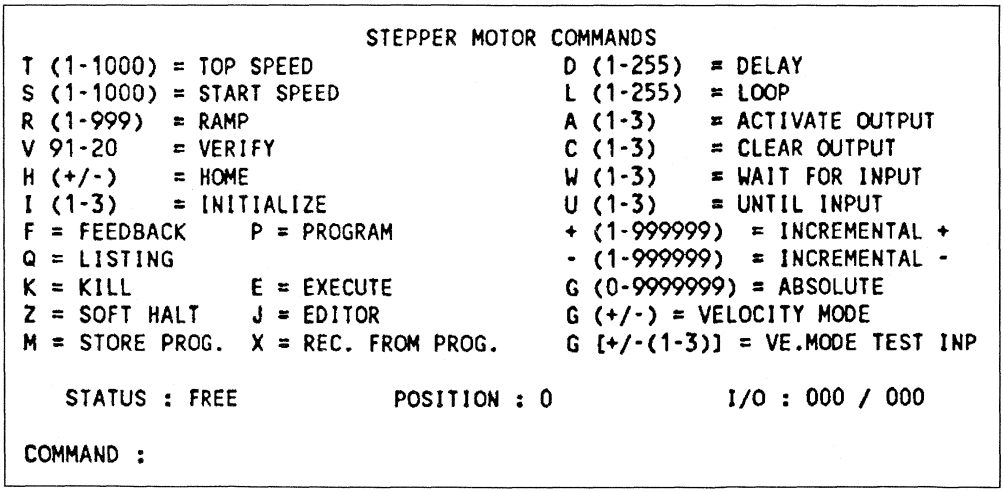
The first video mask on the screen is as shown in fig. 4.

Figure 4. GS-C200PROG FAST.BAS Video Mask



By typing any key, the video mask of fig. 5 will appear on the screen and the user can start the programming session

Figure 5. GS-C200PROG FAST.BAS video mask



Sometime, at the first run of the program, the following message can appear on the video screen:

Device I/O error

this warns the operator that the initialization of the comunication link has not been correctly done; to restart the operations it is sufficient to run the program again.

If the warning message is still present, probably there is an error in the Baud rate programming, or a mistake in the P.C. to GS-C connecting cable.

Programs Editing

The "Program editing" feature allows the user to manage the GS-C program as a file and this makes the field update of a program very cheap and easy.

To enter the Editor program the **J** key followed by a carriage return must be entered. The video mask that will appear is reported in fig. 6.

The blank mask can be filled in by the user. In case the user wants to modify a program already stored in the disk, the command **L** must be issued.

Figure 6. Editor Entry Mask

```
EDITOR MODE        command: X,Q,E     Cn,In,Dn,M,N     P,S,L     Help
-------------------------------------------------------------------------
 1                          21                          41
 2                          22                          42
 3                          23                          43
 4                          24                          44
 5                          25                          45
 6                          26                          46
 7                          27                          47
 8                          28                          48
 9                          29                          49
 10                         30                          50
 11                         31                          51
 12                         32                          52
 13                         33                          53
 14                         34                          54
 15                         35                          55
 16                         36                          56
 17                         37                          57
 18                         38                          58
 19                         39                          59
 20                         40                          60
```

The user may also want to retrieve a program stored in the GS-C200 or GS-C200S controller. In this case, the commands are a sequence of **X** and **Q** commands.

Fig. 7 shows an example of editor mask with program.

Figure 7. Editor Mask with Program

```
EDITOR MODE        command: X,Q,E     Cn,In,Dn,M,N     P,S,L     Help
-------------------------------------------------------------------------
1    R20                 21                              41
2    S1                  22                              42
3    T100                23                              43
4    +200                24                              44
5    D3                  25                              45
6    L0                  26                              46
7    +50                 27                              47
8    D3                  28                              48
9    L4                  29                              49
10   -200                30                              50
11   D3                  31                              51
12   C1                  32                              52
13   U1                  33                              53
14                       34                              54
15                       35                              55
16                       36                              56
17                       37                              57
18                       38                              58
19                       39                              59
20                       40                              60
```

The video screen can also be used to highlight the editor features. To achieve this, the **H** (help) command must be issued.
In this case, the editor mask with program and Help messages can have the form shown in fig. 8.

The programming session is ended by the issue of an "**M**" command.

Giving an "**E**" command the program is sent to GS-C200 (S) module and automatically executed.

To store a program written in Editor mode follow this procedure:

- type an "**E**" command
- wait for the end of program executed
- type an "**M**" command to return to main menu
- in main menu type an "**M**" command to store the written program.

Figure 8. Editor Mask with Program and Help Messages

```
EDITOR MODE        command: X,Q,E     Cn,In,Dn,M,N    P,S,L    Help
-------------------------------------------------------------------------------
1   R20                  21                          X=recall from NVRAM
2   S1                   22                          Q=listing
3   T100                 23                          E=send & execute
4   +200                 24
5   D3                   25                          Cn=change row n
6   L0                   26                          In=insert row n
7   +50                  27                          Dn=delete row n
8   D3                   28                          M=return to main
9   L4                   29                          N=new program
10  -200                 30
11  D3                   31                          P=print
12  C1                   32                          S=save file
13  U1                   33                          L=load file
14                       34
15                       35                          H to return
16                       36
17                       37                       57
18                       38                       58
19                       39                       59
20                       40                       60
```

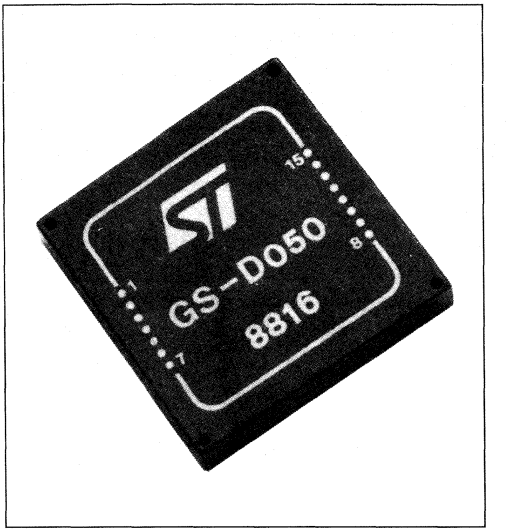
SGS-THOMSON MICROELECTRONICS

GS-D050

0.5A BIPOLAR STEPPER MOTOR DRIVE MODULE

FEATURES

- Inputs TTL/CMOS compatible
- Logic Inhibit/Enable
- Chopper regulation of motor bipolar current
- Programmable motor current (0.5 A max) (by steps or continuously)
- Wide voltage range (10-46 V)
- Full-step (wave and normal drive), Half-step, Quarter-step operations
- Overtemperature protection



DESCRIPTION

The GS-D050 is a driver for bipolar stepper motors that directly interfaces a microprocessor and two phase permanent magnet motors.

The motor current is controlled in a chopping mode up to 0.5 A. The small outline makes the GS-D050 ideal when space is a premium.

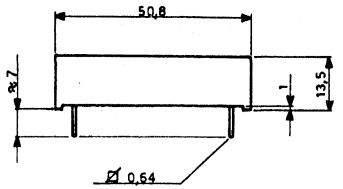
ABSOLUTE MAXIMUM RATINGS

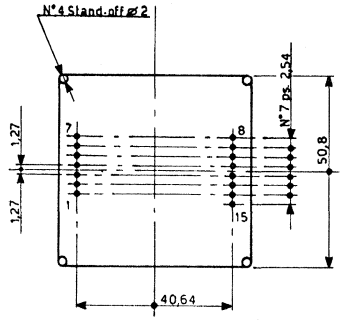
Symbol	Parameter	Value	Unit
V_S	Supply Voltage	46	V
V_{SS}	Logic Supply Voltage	7	V
V_i	Logic Input Voltage	6	V
I_O	Peak Output Current	1.2	A
V_{ref}	Reference Input Voltage	5	V
T_{stg}	Storage Temperature Range	−40 to +105	°C
T_{cop}	Operating Case Temperature Range	−20 to + 85	°C

THERMAL DATA

$R_{th(ca)}$	Case-ambient Thermal Resistance	Max	8.0	°C/W

MECHANICAL DATA (dimensions in mm)





Dimension in mm

Bottom view

PIN DESCRIPTION

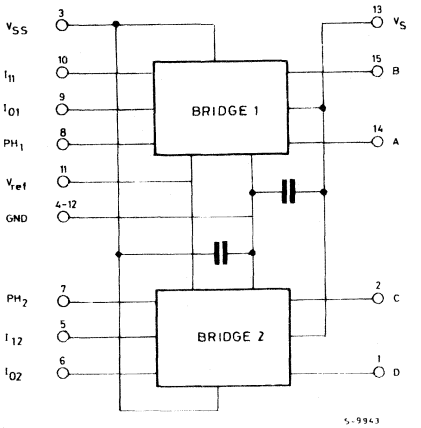
Pin	Function	Description
1	D	Bridge Output D. This output has a phase opposite to the driving signal PH2
2	C	Bridge Output C. This output has the same phase of the driving signal PH2.
3	V_{SS}	Logic Supply Voltage. Maximum applicable voltage is 7 V.
4	GND	See Pin 12
5	I12	Input pin for current level and operating mode selection (see pin 10 - I11 description)
6	IO2	Input pin for current level and operating mode selection (see pin 10 - I11 description)
7	PH2	Phase 2 Logic Input
8	PH1	Phase 1 Logic Input
9	IO1	Input pin for current level selection (see pin 10 - I11 description)
10	I11	Input pin used, together with IO1, to select the current level according to the following table.

I11/I12	IO1/IO2	Phase Current
0	0	Iph = 100 % Iset
0	1	Iph = 60 % Iset
1	0	Iph = 19% Iset
1	1	No Current

PIN DESCRIPTION (Cont'd)

Pin	Function	Description
11	Vref	Reference Input Voltage for the Chopper Comparators. The voltage applied to this pin settles the phase current to the desired value. A 5 V ref sets a 0.5 A phase current when full-step drive is selected.
12	GND	Ground Connection. Motor and logic supply voltage as well as the logic signals, must be referenced to this pin.
13	V2	Motor Unregulated Supply Voltage. Maximum Applicable Voltage is 46 V.
14	A	Bridge Output A. This output has the same phase of the driving signal PH1.
15	B	Bridge Output B. This output has a phase opposite to the driving PH1.

Equivalent Block Diagram of GS-D050



ELECTRICAL CHARACTERISTICS (T_A=25 °C unless otherwise specifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	Pin 13	10		46	V
V_{SS}	Supply Voltage	Pin 3	4.75	5	5.25	V
I_S	Quiescent Supply Current	Pin 13 V_S = 35V Iout = 0		15	30	mA
I_{SS}	Quiescent Supply Current	Pin 3. All Inputs High Iout = 0 V_{SS} = 5 V		15		mA
V_i	Input Voltage	Pin 5, 6, 7, 8, 9, 10 Low High	 2.0		0.8 V_{SS}	V V
I_i	Input Current	Pin 5, 6, 7, 8, 9, 10 Low High			0.4 10	mA µA
Vsat	Source Saturat. Voltage	Pin 1, 2, 14, 15 I_O = 0.5 A Conduction Period			2.1	V
Vsat	Source Saturat. Voltage	Pin 1, 2, 14, 15 Io = 0.5 A Recirculation Period			1.4	V
Vsat	Sink Saturat. Voltage	Pin 1, 2, 14, 15 Io = 0.5 A			1.4	V

MODULE OPERATION

The module consists of two identical sections each of them driving one winding of a bipolar permanent magnet stepper motor.

A brief description is given for one section.

An H bridge output stage (fig. 1) drives the winding of the motor by a constant current up to 0.5 A. The direction of the current depends on which diagonal of the H bridge is activated.

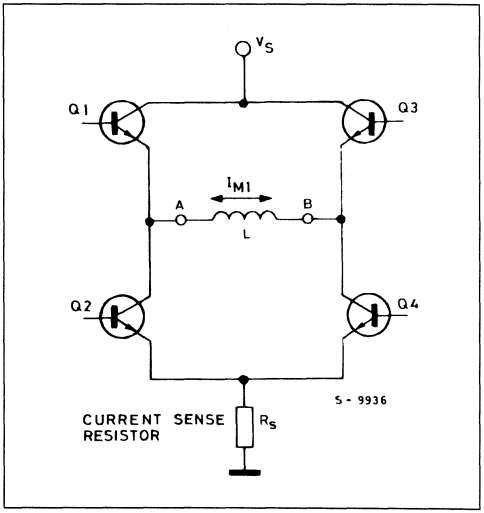
The input signal PH1 selects the diagonal. (See block diagram). When PH1 is high the two transistors Q_1 and Q_4 are switched ON and the current is sourced by the A pin and sinked by the B pin. When PH1 is low, Q_3 and Q_2 are switched ON. At switch ON the current through the winding increases almost linearly according to the equation :

$$\frac{dI_{M1}}{dt} = \frac{V_S}{L}$$

being L the inductance of the winding.

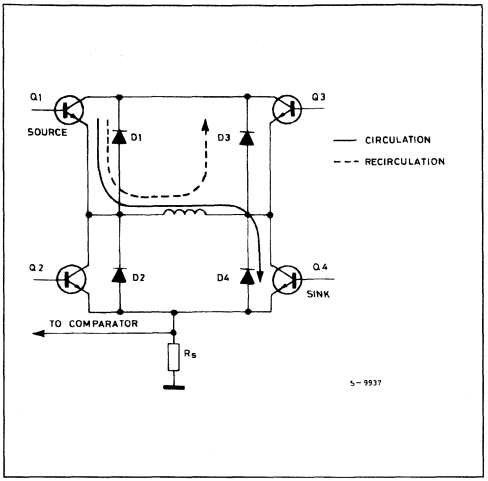
This current is sensed by a current sense resistor R_S and the voltage drop is compared to a reference voltage.

Figure 1. Output Bridge Circuit.



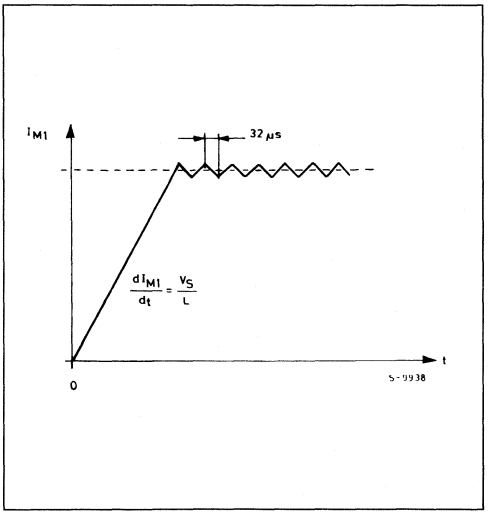
When the voltage drop is higher than reference the sink transistor (for example Q_4) is switched off and the current decays through the source transistor and the recirculating diode D3 (fig. 2).

Figure 2. Current Paths During Current Level Control.



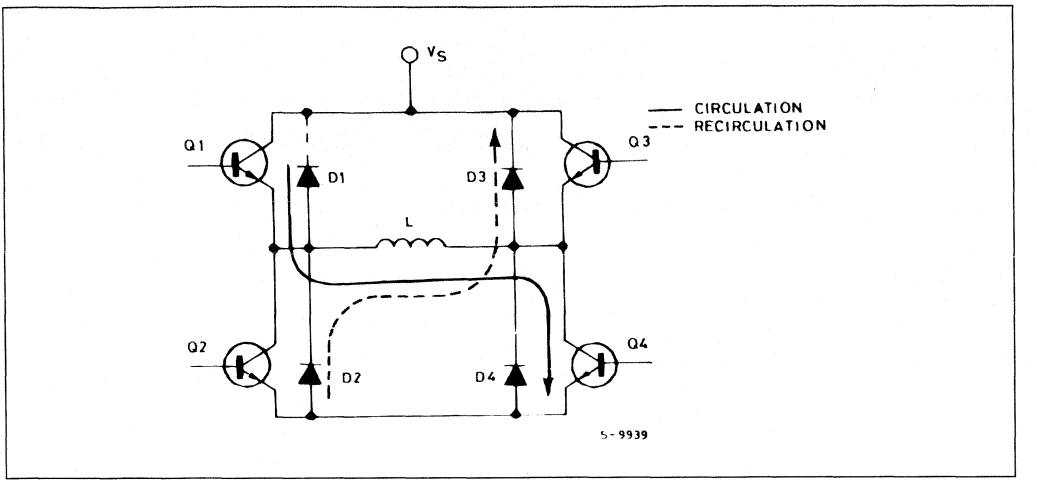
The module contains a monostable circuit that keeps OFF Q_4 for a fixed period of time (t_{OFF} = 32 µs). After t_{OFF}, Q_4 is switched on again and the cycle is repeated as long as PH1 signal is high (fig 3).

Figure 3. Output Current Waveform



When the signal PH1 changes state (from high to low), both Q_1 and Q_4 are switched OFF and Q_2 and Q_3 are switched ON. The current recirculates through D2 and D3 until it decays to zero and then it reverses the direction (fig. 4).

Figure 4. Current Paths During Phase Reversal.



The current phase reversal is therefore obtained by a four quadrant operation while the current level control is by a two quadrant operation. The current decay by a four quadrant is faster being the total voltage applied to the winding almost equal to supply voltage.

The decay time during chopping control of the current level is internally fixed (t_{OFF}), the applied voltage to the inductance is also fixed (about 3 V) and, therefore, the amplitude of current decay or the current ripple depends exclusively on the value of L.

The level of the maximum current is fixed and controlled by a set of voltage dividers and comparators. Four current levels can be digitally selected according to the status of I_{11} and I_{01} (See block diagram and fig. 5).

When $I_{11} = I_{01} = 1$ the H-bridge is disactivated and no current can circulate.

For $I_{11} = 0$; $I_{01} = 0$ the comparator 1 is enabled. The maximum current is allowed to flow through the bridge and the value of the current is given by

$$I_M = \frac{0.042 V_{ref}}{R_S} = 100\%$$

$R_S = 0.47\ \Omega$ is internally fixed. For $V_{ref} = 5$ V the maximum allowed current is 0.45 A.

For $I_{11} = 0$; $I_{01} = 1$ the comparator 2 is enabled and the current is reduced to 60% of the maximum value.

For $I_{11} = 1$; $I_{01} = 0$ the comparator 3 is enabled and the current is reduced to 19%. When in Wave or Half Step mode, the signals I_{11} and I_{01} are used also for the correct timing. The following paragraphs show the mode operation of the GS-D050 making reference to the schematic of fig. 6. The current is considered positive when flowing from A to B or from C to D.

Figure 5. Current Level Setting.

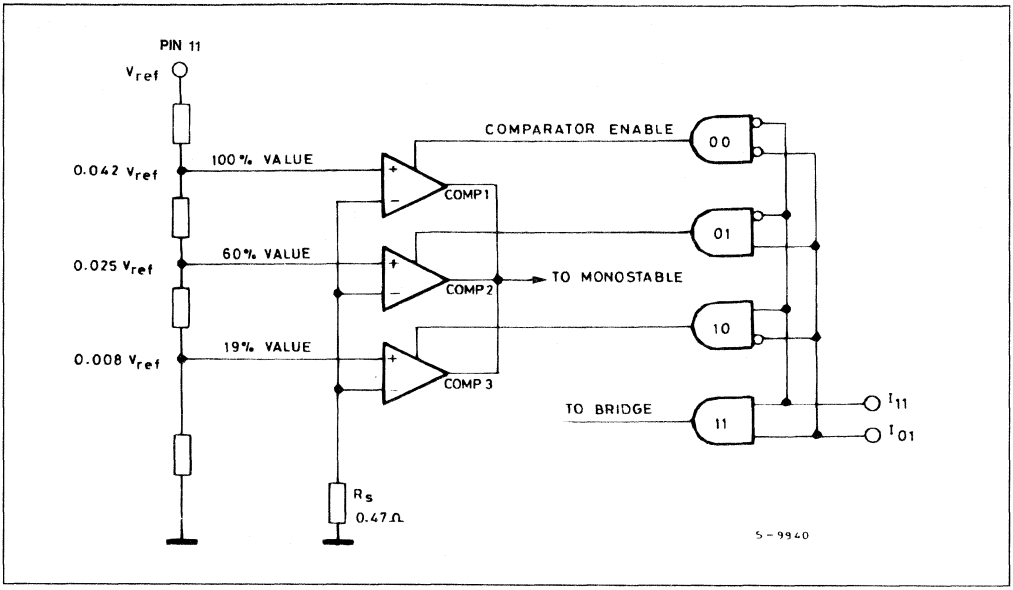
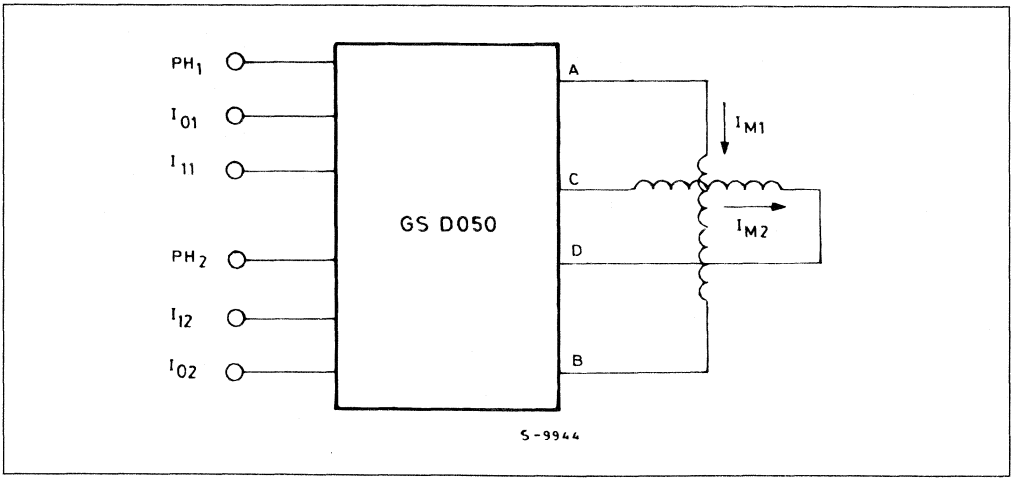


Figure 6. Basic GS-D050 Inputs and Outputs.



ONE PHASE ON or WAVE CURRENT

Only one winding is energized at any given time according to the sequence (for FWD direction)

AB ; CD ; BA ; DC ;

(BA means a negative current flowing from B to A).

Fig. 7 and 8 show the timing of the input signals and of the output currents.

Figure 7. Wave Drive FWD Direction.

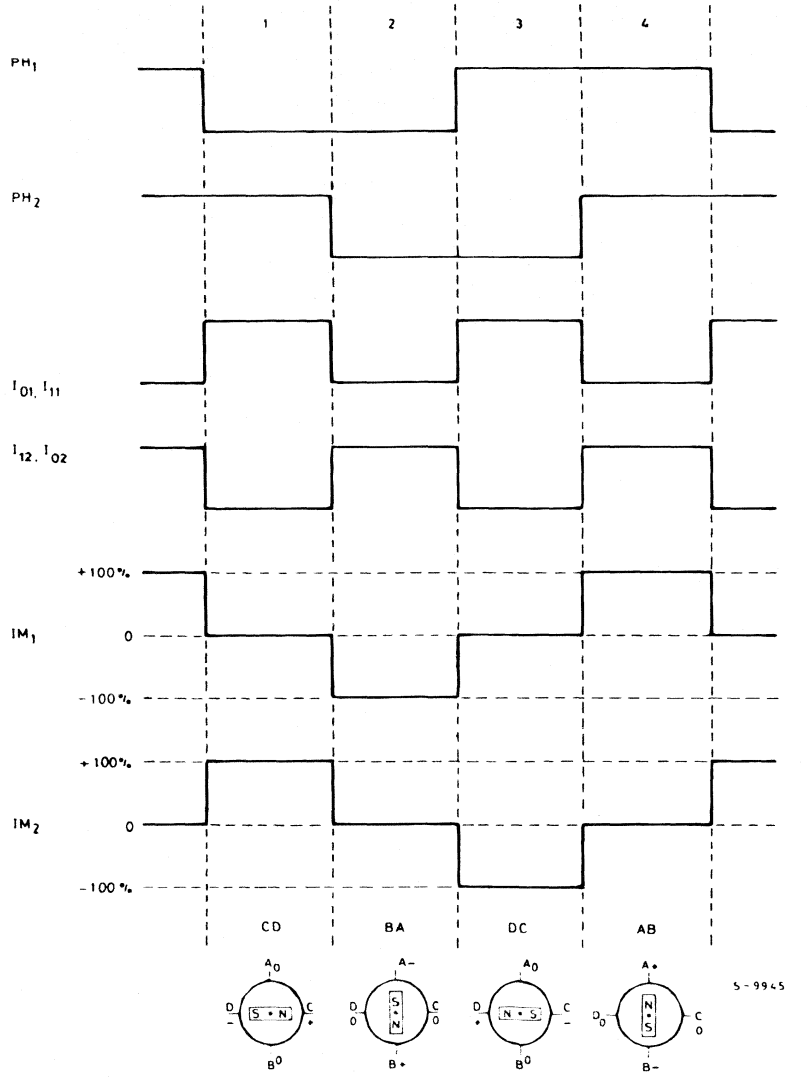
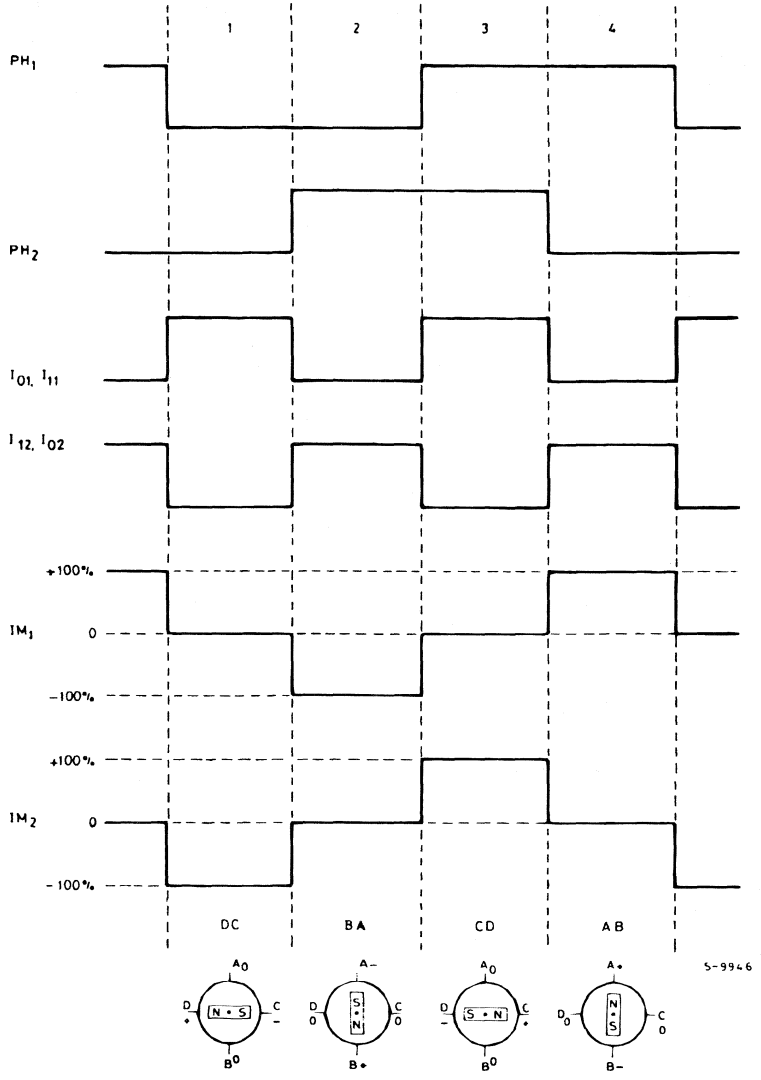


Figure 8. Wave Drive REV Direction.



TWO-PHASE-ON or NORMAL DRIVE

Two windings are energized at any given time according to the sequence (FWD direction).

AB & CD ; CD & BA ; BA & DC ; DC & AB

In this case I_{01}, I_{11} signals are used just for current level set.

Fig. 9 and 10 show the timing or various signals.

Figure 9. Two-Phase-on FWD Direction.

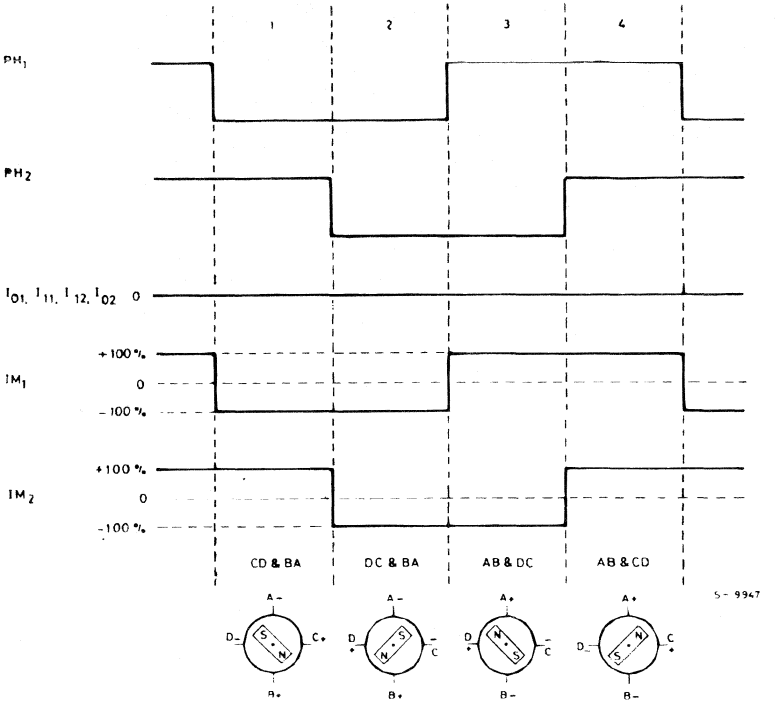
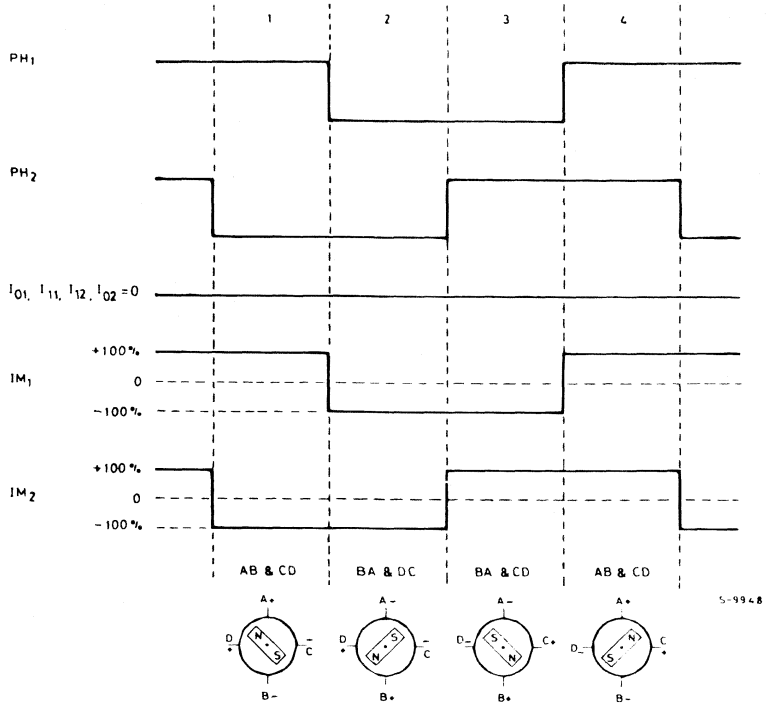


Figure 10. Two-Phase-on REV Direction.



HALF STEP DRIVE

By this mode one winding or two windings are alternatively energized. Eight steps are required for a complete revolution of the rotor.

For FWD direction the sequence is :

AB ; AB & CD ; CD & BA ; BA & DC ; DC ; DC & AB

Fig. 11 and 12 show the timing of various signals.

Figure 11. Half Step FWD Direction.

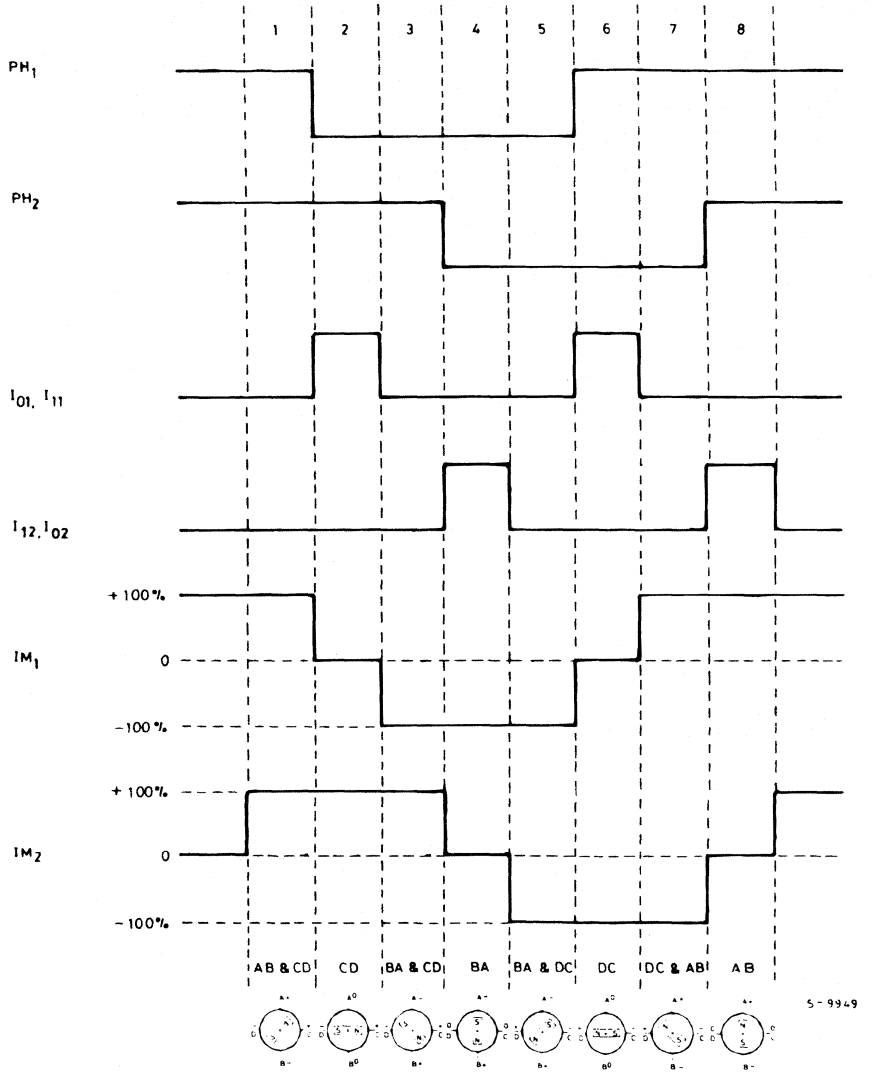


Figure 12. Half Step REV Direction.

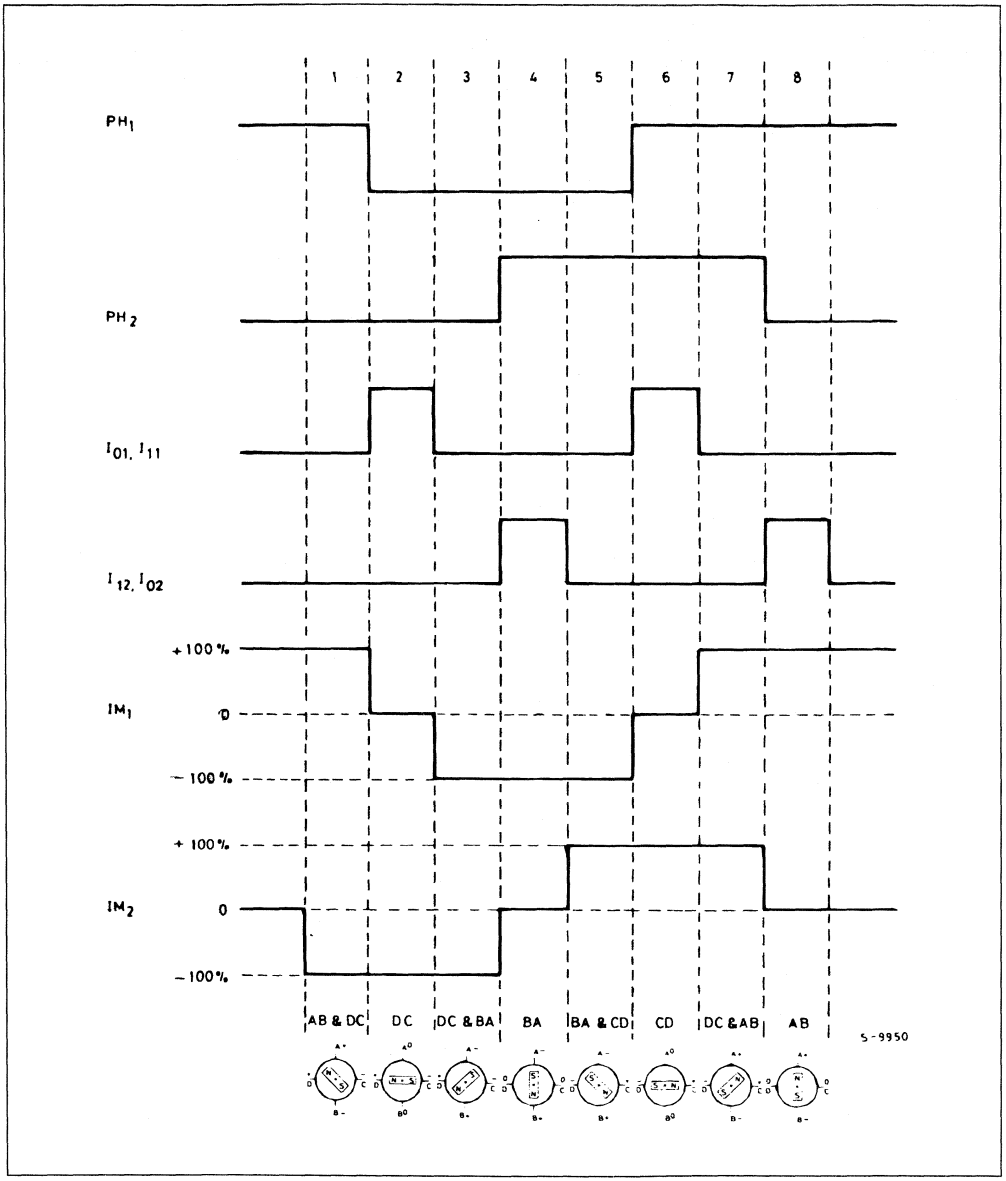


Figure 13. Quarter Step FWD Direction.

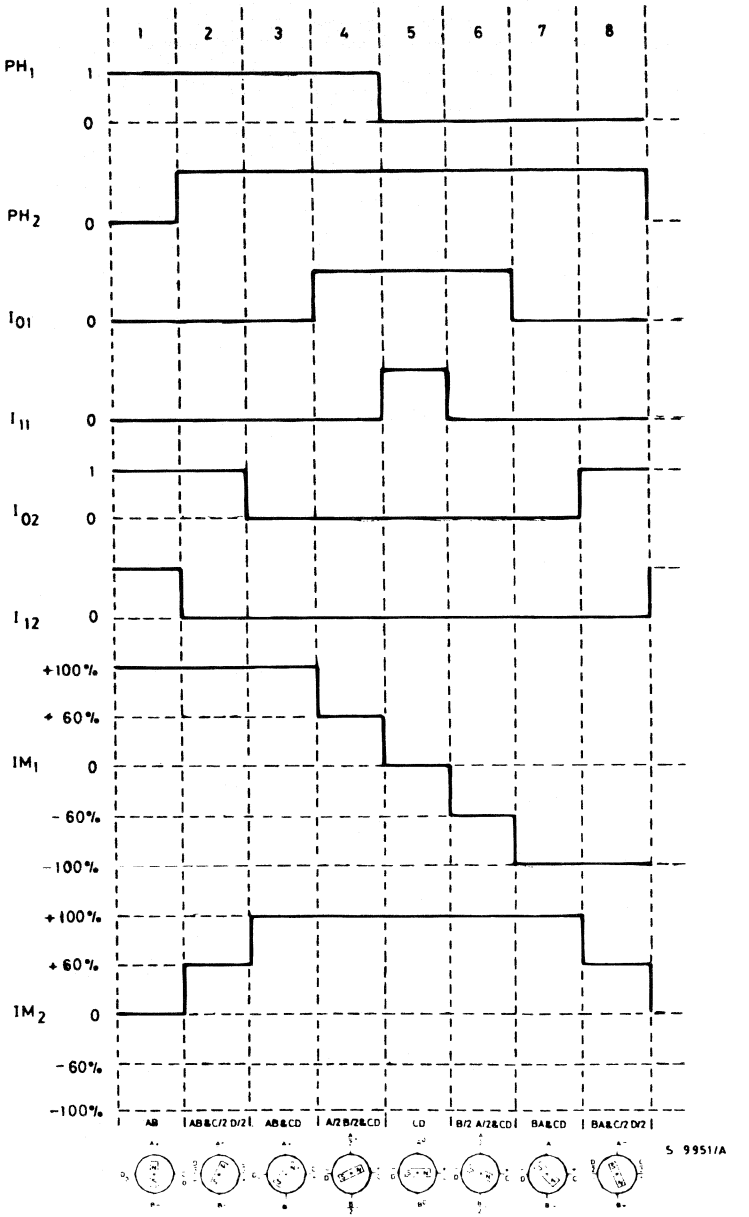
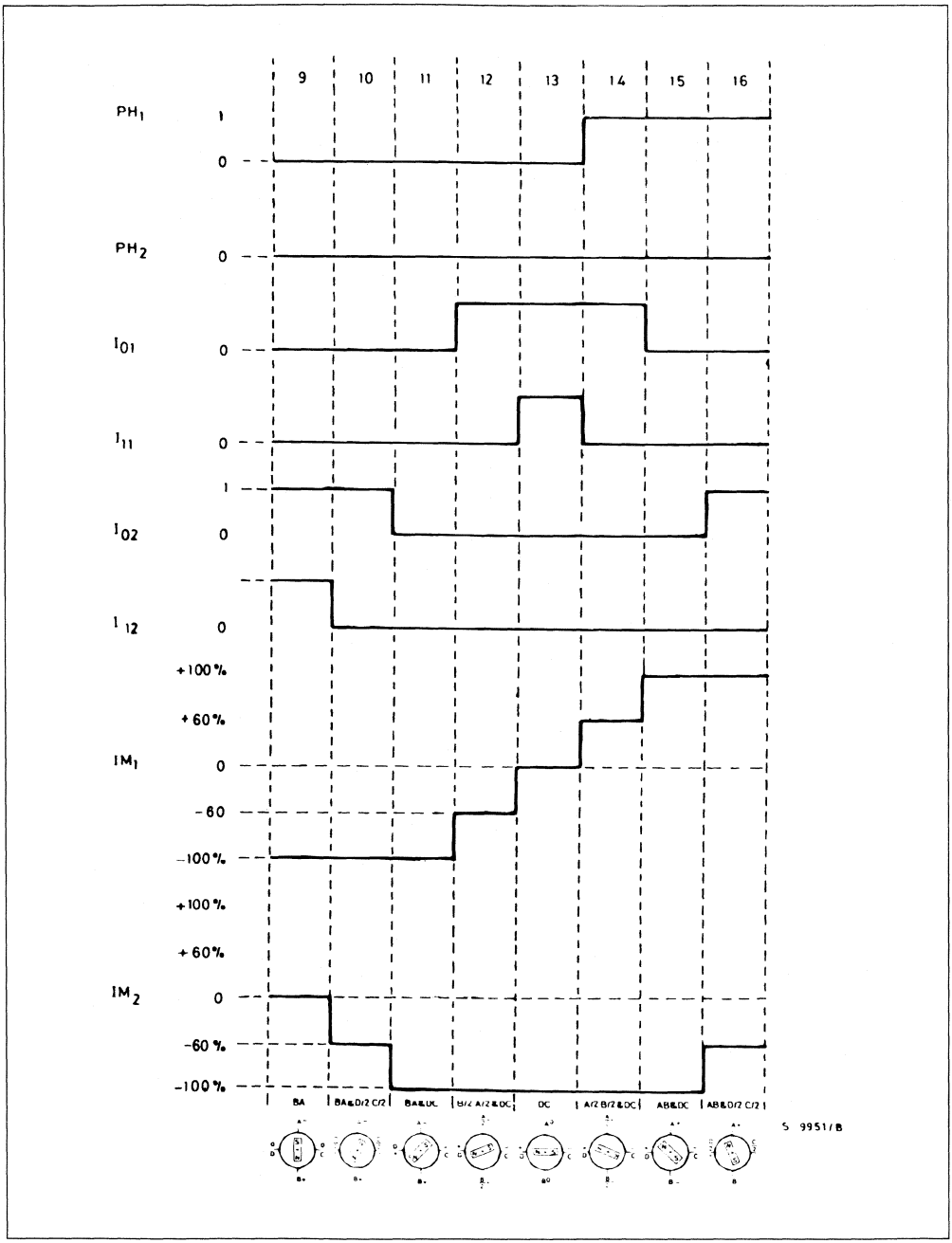


Figure 13. Quarter Step FWD Direction. (Continued)



For wave, normal, half step, the driving can be made at any current level : for simplicity the previous diagrams refer to a condition where 100 % of the motor current is used, as set by the equation.

$$I_H = \frac{0.042\ V_{ref}}{R_S}$$

In half step mode it is advisable to reduce the current level to 60 % of the maximum when two windings are energized and to use the maximum value when one winding is energized : this allows a less irregular torque.

This operation can be simply performed by selecting the proper status of I_{01} and I_{02}.

QUARTER STEP DRIVE

It is preferable to perform the quarter step drive at full power to have a more regular torque.

The extra quarter steps are added to the half step sequence by putting one winding at half current according to the sequence.

$$AB\ ;\ AB\ \&\ \frac{CD}{2}\ ;\ AB\ \&\ CD\ ;\ \frac{AB}{2}\ \&\ CD\ ;\ CD\ ;$$

$$CD\ \&\ \frac{BA}{2}\ ;\ CD\ \&\ BA\ ;\ \frac{CD}{2}\ \&\ BA\ ;\ BA\ ;$$

$$BA\ \&\ \frac{DC}{2}\ ;\ BA\ \&\ DC\ ;\ \frac{BA}{2}\ \&\ DC\ ;\ DC\ ;$$

$$DC\ \&\ \frac{AB}{2}\ ;\ DC\ \&\ AB\ ;\ \frac{DC}{2}\ \&\ AB.$$

The timing for forward direction is shown on fig. 13. 16 steps are required for one complete revolution.

APPLICATION CIRCUIT

A typical application is shown on fig. 14 for a maximum winding current of about 0.5 A.

As shown, no external component is needed to drive the motor.

Signals I_{01}, I_{11}, I_{02}, I_{12} may be used to inhibit the module when they are permanently kept at high level. If they are left open, the GS-D050 treats them as at high logic level.

The case of the GS-D050 is electrically connected to ground : radiated EMI caused by chopping operation is therefore shielded by the case itself.

To reduce further EMI a low pass filter can be inserted across the outputs of the GS-D050 as shown on fig. 15.

L, C, components should be selected according to

$$L \cong \frac{L_M}{10} \qquad C = \frac{4 \cdot 10^{-10}}{L}$$

The module is protected against thermal overload.

If by any reasons (very high ambient temperature or high power dissipation or both) the junction temperatures of active components inside the GS-D050 reach 150° C the module automatically reduces the output power and the power dissipation.

Even if the module controls the maximum output current, a short circuit of the outputs can damage the device.

Figure 14. GS-D050 Basic Application Circuit.

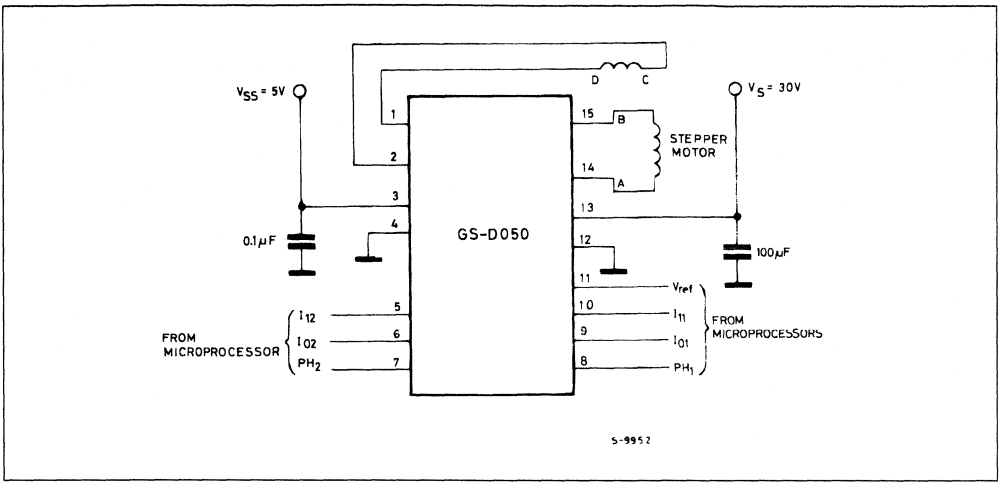
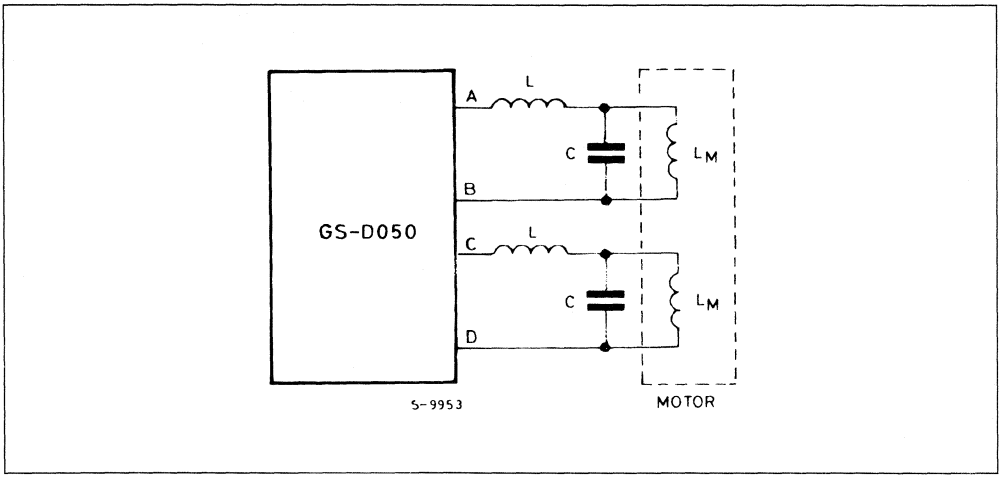


Figure 15. Circuit for EMI Reduction.



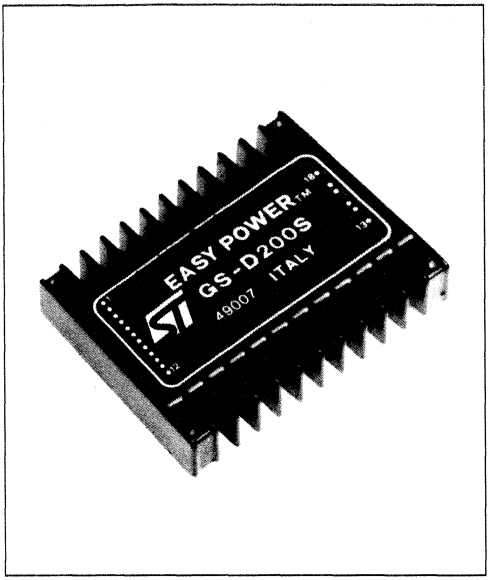
SGS-THOMSON MICROELECTRONICS

GS-D200
GS-D200S

2/2.5A BIPOLAR STEPPER MOTOR DRIVE MODULES

FEATURES

- Wide supply voltage range
- Full/Half step drive capability
- Logic signals TTL/CMOS compatible
- Programmable motor phase current and chopper frequency
- Selectable Slow/Fast current decay
- Synchronization for multimotor applications
- Remote shut-down
- Home position indication



DESCRIPTION

The **GS-D200** and the **GS-D200S** are drive modules that directly interface a microprocessor to a two phase, bipolar, permanent magnet stepper motors.
The phase current is chopper controlled, and the internal phase sequence generation reduces the burden of the controller and it simplifies software development.
The **GS-D200** uses bipolar power outputs while the **GS-D200S** has powermos outputs to significantly reduce both commutation and conduction losses.
A further benefit offered by the **GS-D200S** is the complete protection of the outputs against any type of shorts.

SELECTION CHART

Type Ordering Number	Phase Current (A)	Voltage Drop (V)	Supply Voltage (V)
GS-D200	1.0 nom. (0.5 to 2.0)	4.1 max.	10 to 46 5.0±5%
GS-D200S	2.0 nom. (0.5 to 2.5)	2.5 max.	12 to 40 5.0±5%

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_S	DC Input Voltage (pin 18)	GS-D200 GS-D200S	48 42	V V
V_{SS}	DC Input Voltage (pin 12)		7	V
T_{stg}	Storage Temperature Range		–40 to +105	°C
T_{cop}	Operating Case Temperature Range		–20 to +85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter	Test Conditions		Value			Unit
				Min	Typ	Max	
I_S	Quiescient Supply Current	Pin 18				20	mA
I_{SS}	Quiescent Supply Current	Pin 12 V_{SS}=5V			60		mA
V_i	Input Voltage	Pin 3,4,6,7,10,11	Low High	 2		0.8 V_{SS}	V V
I_i	Input Current	Pin 3,4,6,7,10,11	V_i=Low V_i=High			0.6 10	mA µA
Vsat	Source/Sink Saturation Voltage(GS-D200)	Pin 14,15,16,17	I_O=1A			1.8	V
Vsat	Source/Sink Saturation Voltage(GS-D200S)	Pin 14,15,16,17	I_O=2A			1.8	V
IoL	Current Limit Intervention	GS-D200S		5			A
fc	Chopper Frequency				17		kHz
tclk	Stepckl Width	Pin 6 (See fig. 1)		0.5			µs
ts	Set Up Time	"		1			µs
th	Hold Time	"		1			µs
tr	Reset Width	"		1			µs
trclk	Reset to Clock Set Up Time	"		1			µs

Figure 1: Signals Timing

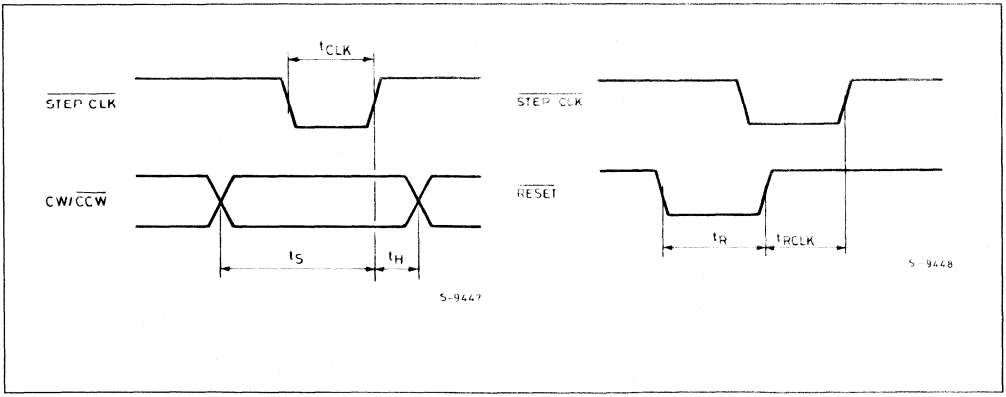


Figure 2: GS-D200 and GS-D200S Block Diagram

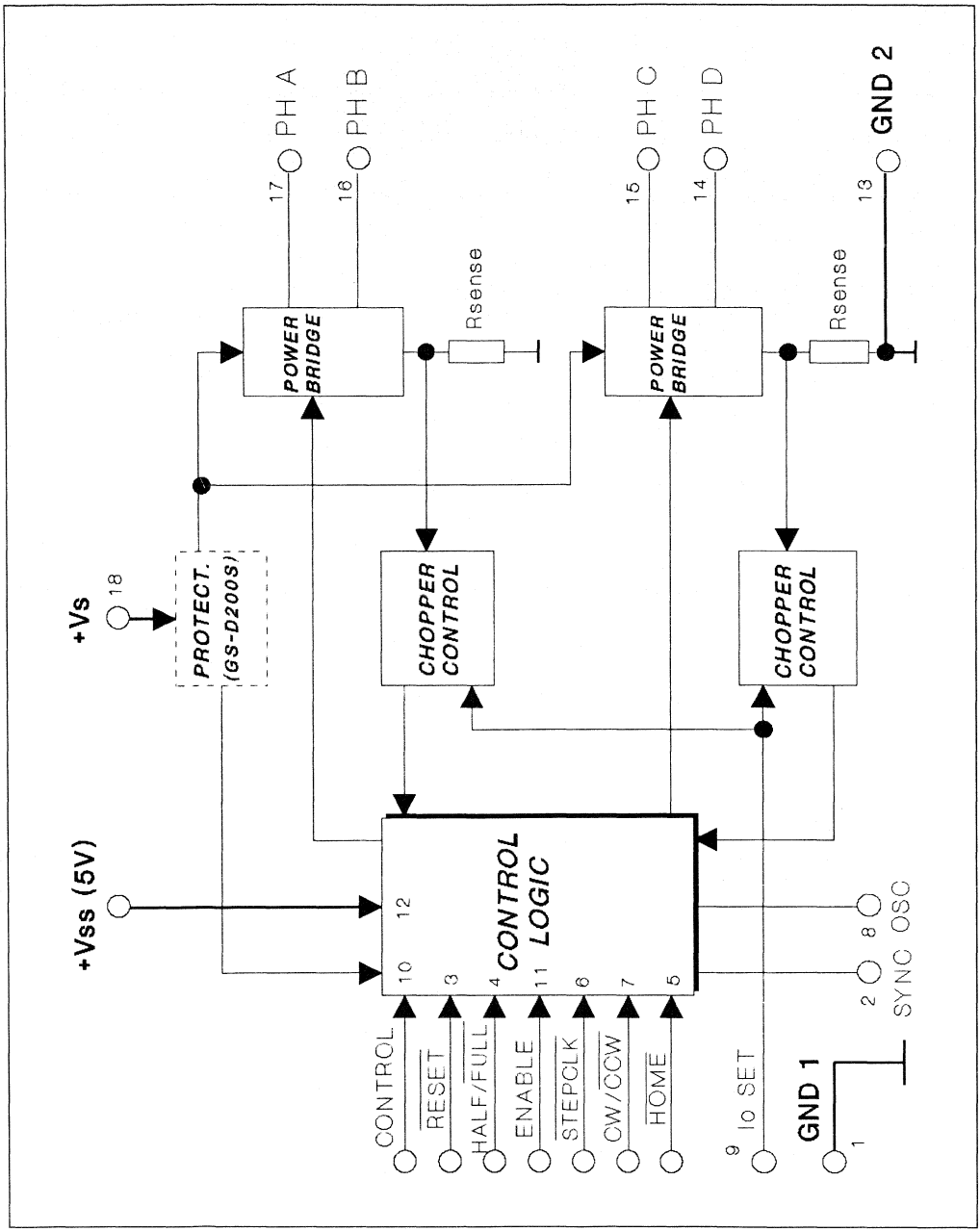


Figure 3: GS-D Modules Typical Application

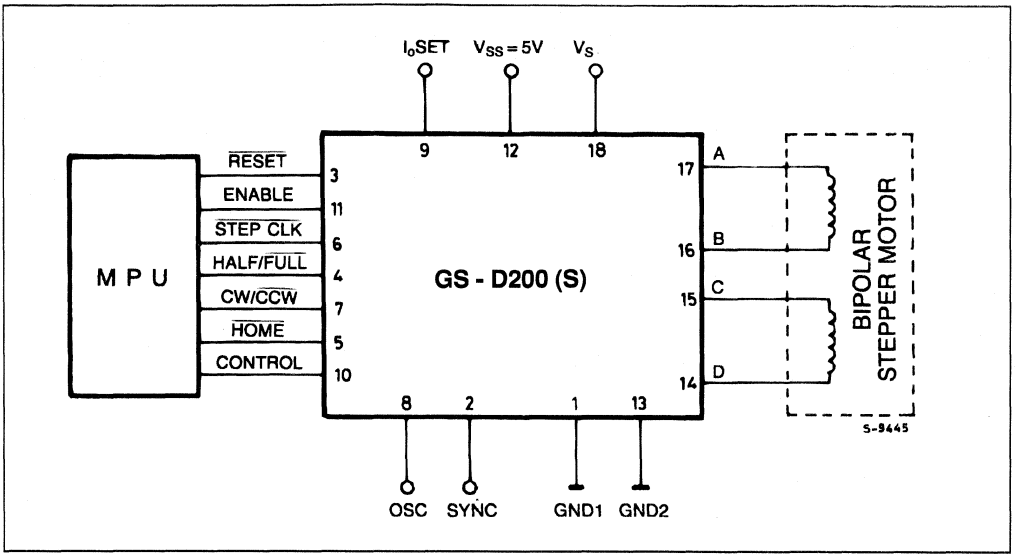
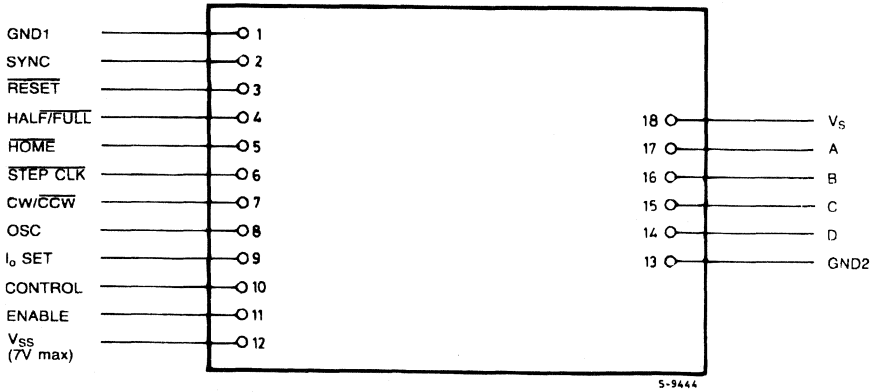


Figure 4: GS-D200 and GS-D200S Connection Diagram (Top view)



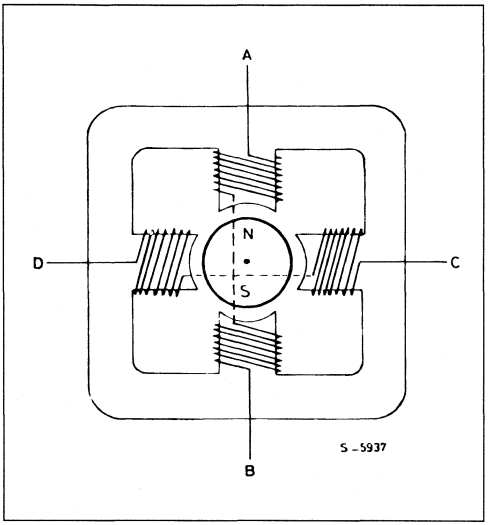
PIN DESCRIPTION

Pin	Function	Description
1	GND1	Return path for the logic signals and 5V supply.
2	Sync	Chopper oscillator output. Several modules can be synchronized by connecting together all Sync pins. This pin can be used as the input for an external clock source.
3	$\overline{\text{Reset}}$	Asynchronous reset input. An active low pulse on this input preset the internal logic to the initial state (ABCD=0101).
4	Half/$\overline{\text{Full}}$	Half/Full step selection input. When high or unconnected the half step operation is selected.
5	$\overline{\text{Home}}$	When low this output indicates that the internal counter is in its initial state (ABCD=0101). This signal should be ANDed with the output of a mechanical switch to be used as a system Home indication.
6	$\overline{\text{Stepclk}}$	The motor is moved one step on the rising edge of this signal.
7	CW/$\overline{\text{CCW}}$	Direction control input. When high or unconnected clockwise rotation is selected. Physical direction of motor rotation depends also on windings connection.
8	Oscillator	The chopper oscillator timing, internally fixed at 17kHz, can be modified by connecting a resistor between this pin and V_{SS} or a capacitor between this pin and Gnd1. The oscillator input must be grounded when the unit is externally synchronized.
9	Ioset	Phase current setting input. A resistor connected between this pin and Gnd1 or V_{SS}, allows the factory setted phase current value (1A for GS-D200 and 2A for GS-D200S) to be changed.
10	Control	Logic input that allows the phase current decay mode selection. When high or unconnected the slow decay is selected.
11	Enable	Module enable input. When low this input floats the outputs enabling the manual positioning of the motor. Must be LOW during power-up and down sequence, HIGH during normal operation.
12	V_{SS}	5V supply input. Maximum voltage must not exceed 7V.
13	GND2	Return path for the power section.
14	D	D output.
15	C	C output.
16	B	B output.
17	A	A output.
18	V_S	Module and motor supply voltage. Maximum voltage must not exceed the specified values.

BIPOLAR STEPPER MOTOR BASICS

Simplified to the bare essentials, a bipolar permanent magnet motor consists of a rotating-permanent magnet surrounded by stator poles carrying the windings (fig. 5).

Figure 5: Simplified Bipolar Two Phase Motor



Bidirectional drive current is imposed on windings A-B and C-D and the motor is stepped by commutating the voltage applied to the windings in sequence. For a motor of this type there are three possible drive sequences.

One-Phase-on or Wave Drive

Only one winding is energized at any given time according to the sequence :

AB - CD - BA - DC

(BA means that the current is flowing from B to A).

Fig. 6 shows the sequence for a clockwise rotation and the corresponding rotor position.

Two-Phase-on or Normal Drive

This mode gives the highest torque since two windings are energized at any given time according to the sequence (for clockwise rotation).

AB & CD ; CD & BA ; BA & DC ; DC & AB

Fig. 7 shows the sequence and the corresponding position of the rotor.

Half Step Drive

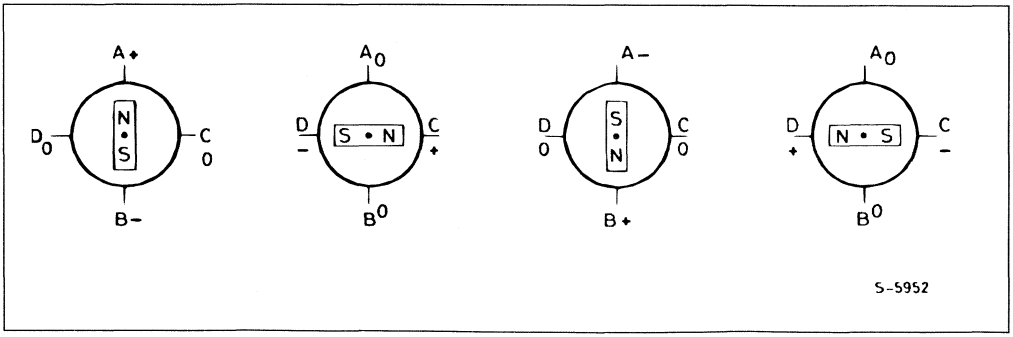
This sequence halves the effective step angle of the motor but gives a less regular torque being one winding or two windings alternatively energized. Eight steps are required for a complete revolution of the rotor.
The sequence is:

AB ; AB & CD ; CD ; CD & BA ; BA ; BA & DC ; DC ; DC & AB

as shown in fig. 8.

By the configurations of fig. 6, 7, 8 the motor would have a step angle of 90 ° (or 45 ° in half step). Real motors have multiple poles pairs to reduce the step angle to a few degrees but the number of windings (two) and the drive sequence are unchanged.

Figure 6: One-Phase-on (Wave Mode) Drive



SGS-THOMSON MICROELECTRONICS

Figure 7: Two-Phase-on (Normal Mode) Drive

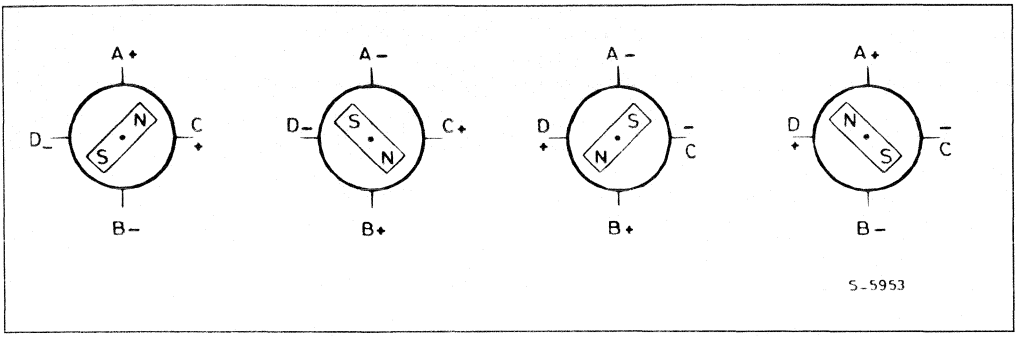
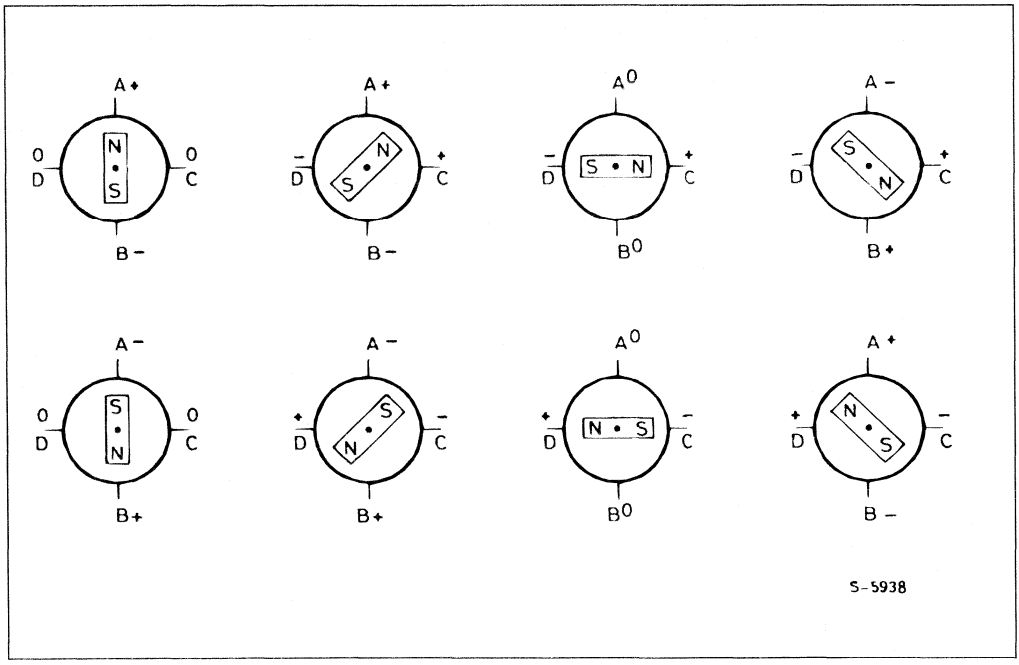


Figure 8: Half Step Sequence



PHASE SEQUENCE GENERATION INSIDE THE GS-D200/GS-D200S

The modules contains a three bit counter plus some combinational logic which generate suitable phase sequences for half step, wave and normal full step drive. This 3 bit counter generates a basic eight-step Gray code master sequence as shown in fig. 9. To select this sequence, that corresponds to half step mode, the HALF/FULL input (pin 4) must be kept high or unconnected.

The full step mode (normal and wave drive) are both obtained from the eight step master sequence by skipping alternate states. This is achieved by forcing the step clock to bypass the first stage of the 3 bit counter. The least significant bit of this counter is not affected and therefore the generated sequence depends on the state of the counter when full step mode is selected by forcing pin 4 (HALF/FULL) low. If full step is selected when the counter is at any odd-numbered state, the two-phase-on (normal mode) is implemented (see fig. 10).

On the contrary, if the full mode is selected when the counter is at an even-numbered state, the one-phase-on (wave drive) is implemented (see fig. 11).

Figure 9: The Eight Step Master Sequence corresponding to Half Step Mode.

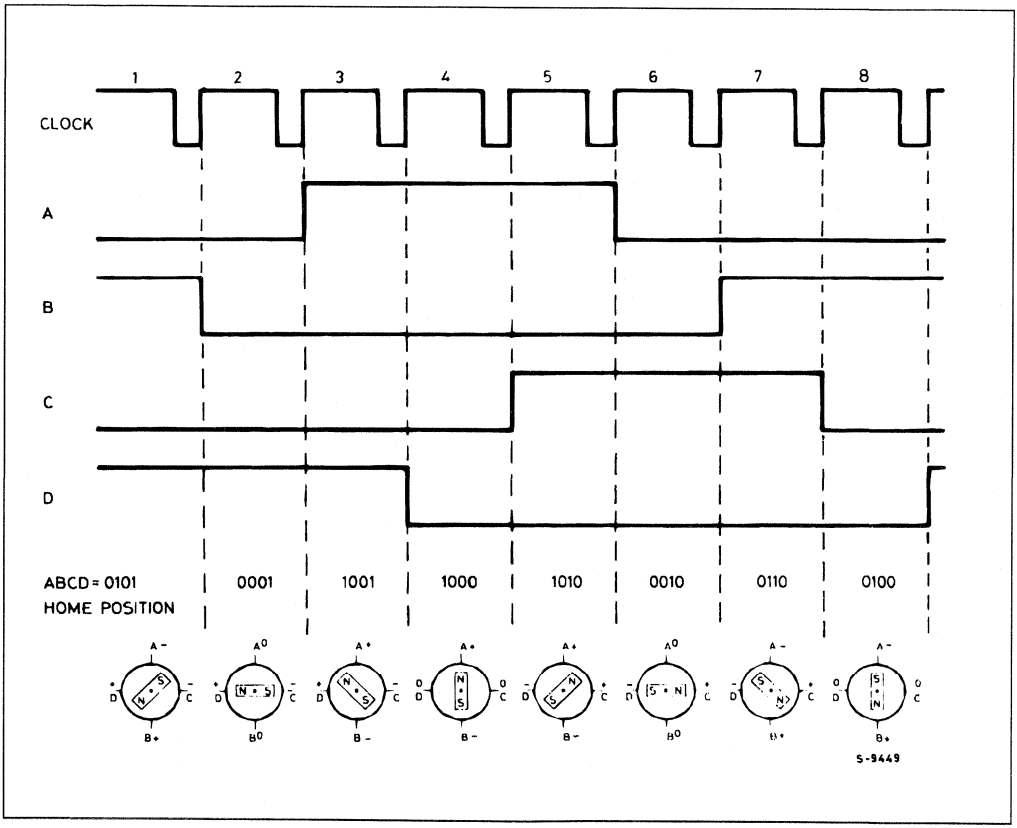


Figure 10: Two-Phase-on (Normal Mode) Drive

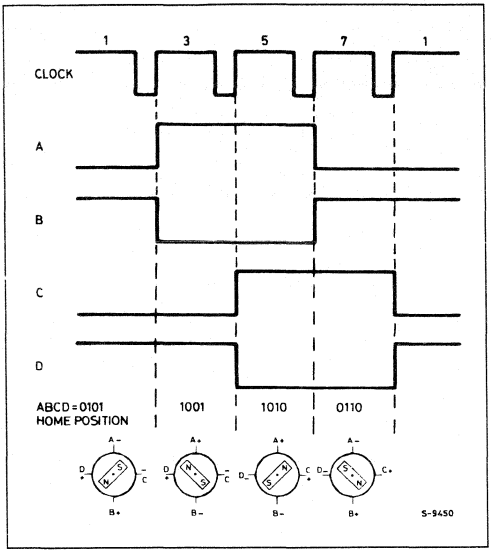
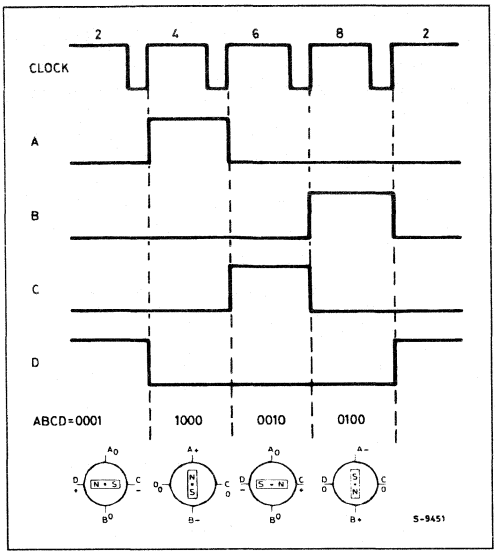


Figure 11: One-Phase-on (Wave Mode) Drive



RESET, ENABLE AND HOME SIGNALS

The $\overline{\text{RESET}}$ is an asynchronous reset input which restores the module to the home position (state 1 : ABCD = 0101). Reset is active when low.

The $\overline{\text{HOME}}$ output signals this condition and it is intended to be ANDed with the output of a mechanical home position sensor.

The ENABLE input is used to start up the module after the system initialization. ENABLE is active when high or unconnected.

MOTOR CURRENT REGULATION

The two bipolar winding currents are controlled by two internal choppers in a PWM mode to obtain good speed and torque characteristics.
An internal oscillator supplies pulses at the chopper frequency to both choppers.

When the outputs are enabled, the current through the windings raises until a peak value set by I_{oset} and R_{sense} (see the equivalent block diagram) is reached. At this moment the outputs are disabled and the current decays until the next oscillator pulse arrives.

The decay time of the current can be selected by the CONTROL input (pin 10). If the CONTROL input is kept high or open the decay is slow, as shown in fig. 12, where the equivalent power stage of GS-D200, the voltages on A and B are shown as well as the current waveform on winding AB.

When the CONTROL input is forced low, the decay is fast as shown in fig. 13.

The CONTROL input is provided on GS-D200 and GS-D200S to allow maximum flexibility in application.

If the modules must drive a large motor that does not store much energy in the windings, the chopper frequency must be decreased: this is easily obtained by connecting an external capacitor between OSC pin and GND1.

In these conditions a fast decay (CONTROL LOW) would impose a low average current and the torque could be inadequate. By selecting CONTROL HIGH, the average current is increased thanks to the slow decay.

When the GS-D200S is used in the fast-decay mode it is recommended to connect external fast recovery, low drop diodes between each phase output and the supply return (GND). The slow-decay should be the preferred operating recirculation mode because of the lower power dissipation and low noise operations.

Figure 12: Chopper Control with Slow Decay

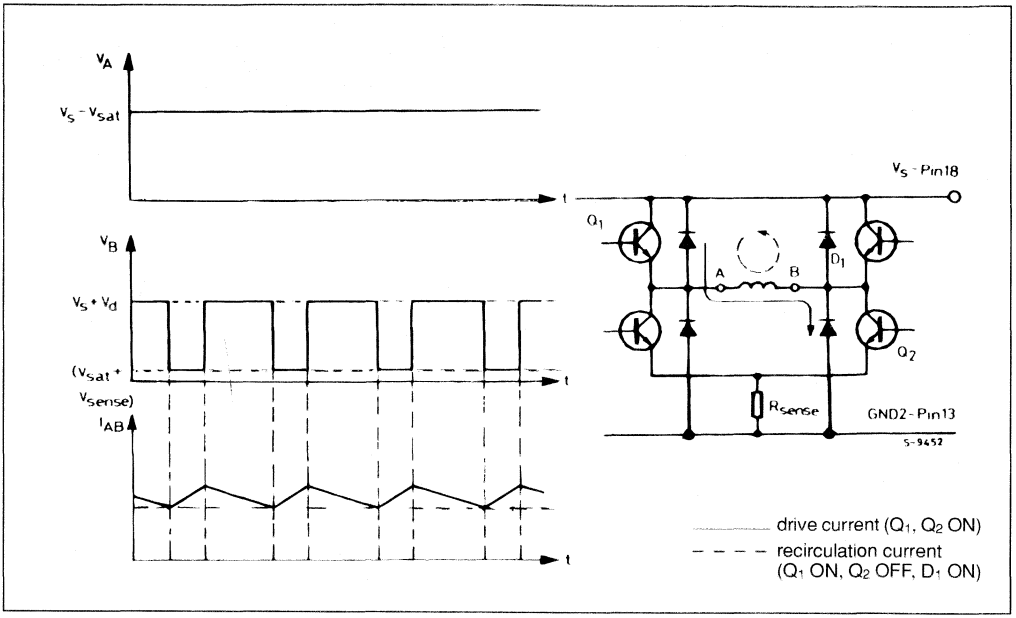
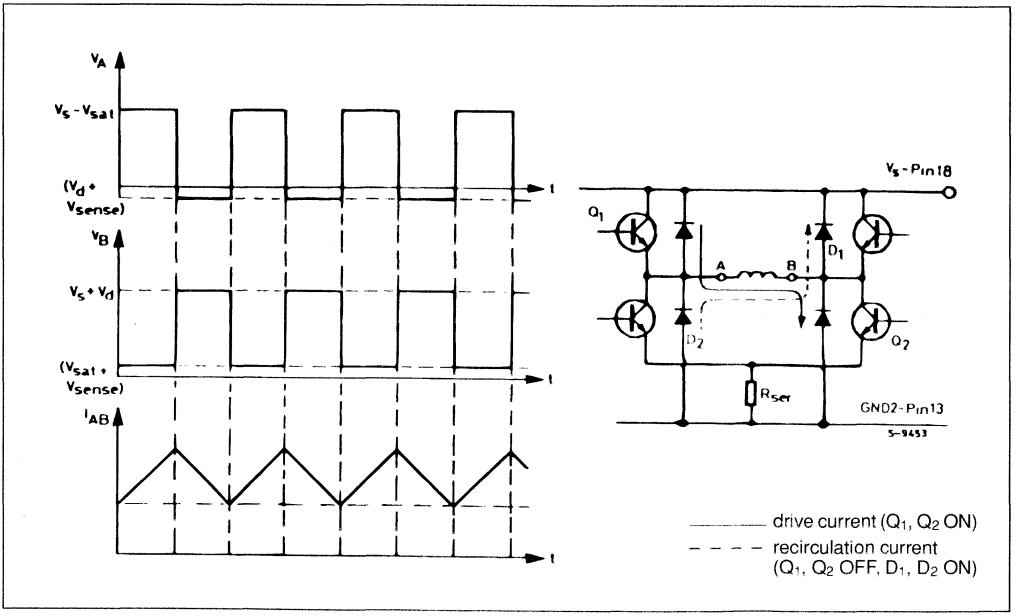


Figure 13: Chopper Control with Fast Decay



USER NOTES

Supply Voltage

The recommended operating maximum supply voltage must include the ripple voltage for the V_S rail, and a 5V±5% for the V_{SS} line is required.
The two supply voltages must to be correctly sequenced to avoid any possible erroneous positioning of the power stages. The correct power-up and power-down sequences are:

Power-up
1) V_{SS} (5V) is applied with Enable = Low
2) V_S (the motor supply voltage) is applied
3) Enable is brougth High

Power-down
1) Enable is brougth Low
2) V_S is switched off
3) V_{SS} is switched off.

Case Grounding

The module case is internally connected to pin 1 and 13. To obtain additional effective EMI shield, the PCB area below the module can be used as an effective sixth side shield.

Thermal Characteristics

The case-to-ambient thermal resistance of the GS-D modules is 5°C/W. This produces a 50°C temperature increase of the module surface for 10W of internal dissipation.
According to ambient temperature and/or to power dissipation, an additional heatsink or forced ventilation may be required. (See derating curves).

Supply Line Impedance

The module has an internal capacitor connected accross the supply pins (18 and 13) to assure the circuit stability. This capacitor cannot handle high values of current ripple, and would be permanently damaged if the primary energy source impedance is not adequate.
The use of a low ESR, high ripple current 470µF capacitor located as close to the module as possible is recommended. Suitable units are the SPRAGUE type 672D, the SPRAGUE 678D, the RIFA type PEG 126 or any equivalent unit. When space is a limitation, a 22µF ceramic multilayer capacitor connected across the module input pins must be used.

Module Protections

The GS-D200 outputs are protected against occasional and permanent short-circuits of the output pin to the supply voltage. The GS-D200S outputs are also protected against short circuits to ground and to another output. When the current exceeds the maximum value, the output is automatically disabled.

The GS-D200S protection is of the latching type, i.e. when an overload condition is detected the unit outputs are disabled. To restart the operations it is necessary to disable the unit (pin 11=Low) or to switch off the supply voltage for at least 100ms.

Motor Connection

The motor is normally quite far from the module and long cables are needed for connection. The use of a twisted pair cable with appropriate cross section for each motor phase is recommended to minimize DC losses and RFI problems.

Unused Inputs

All the GS-D200 and GS-D200S logic inputs have an internal pull-up, and they are high when unconnected.

Phase Current Programming

The output current of the GS-D200 is factory set to 1A while the GS-D200S has a standard 2A value. The phase current value can be changed by connecting an appropriate resistor between pin 9 and ground or V_{SS} (see fig. 14). In the first case the phase current will decrease, in the latter it will increase.
The maximum phase current must be limited to 2A for the GS-D200 and 2.5A for the GS-D200S to avoid permanent damage to the module.

GS-D200 phase current programming:

$$I>1A \qquad Ri = \frac{10 - I}{0.993 \cdot I - 1} = k\Omega \qquad Ri \geq 8.2\ k\Omega$$

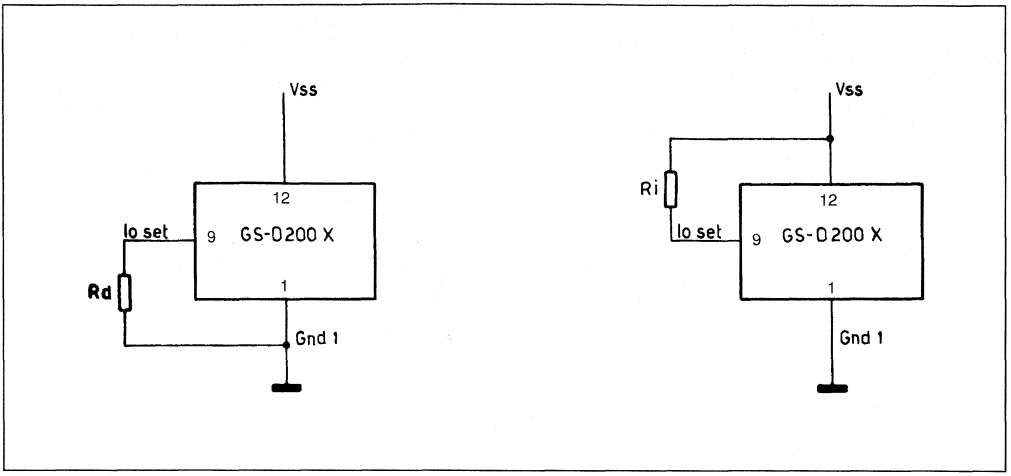
$$I<1A \qquad Rd = \frac{I}{1 - 0.993 \cdot I} = k\Omega$$

GS-D200S phase current programming:

$$I>2A \qquad Ri = \frac{10 - 0.33 \cdot I}{0.473 \cdot I - 1} = k\Omega \qquad Ri \geq 50\ k\Omega$$

$$I<2A \qquad Rd = \frac{I}{3.03 - 1.43 \cdot I} = k\Omega$$

Figure 14: GS-D200 and GS-D200S Phase Current Programming



Chopper Frequency Programming

The chopper frequency is internally set to 17kHz, and it can be changed by addition of external components as follows. To increase the chopper frequency a resistor must be connected between Oscillator (pin 8) and V_{SS} (pin 12, see fig. 15).
The resistor value is calculated according to the formula:

$$Rf = \frac{306}{fc - 17} = k\Omega \qquad \text{where } fc = kHz \quad Rf \geq 18k\Omega$$

To decrease the chopper frequency a capacitor must be connected between Oscillator (pin 8) and Gnd1 (pin 1). The capacitor value is calculated according to the formula:

$$Cf = \frac{80.5 - 4.7fc}{fc} = nF \quad \text{where } fc = kHz$$

Figure 15: Chopper Frequency Programming

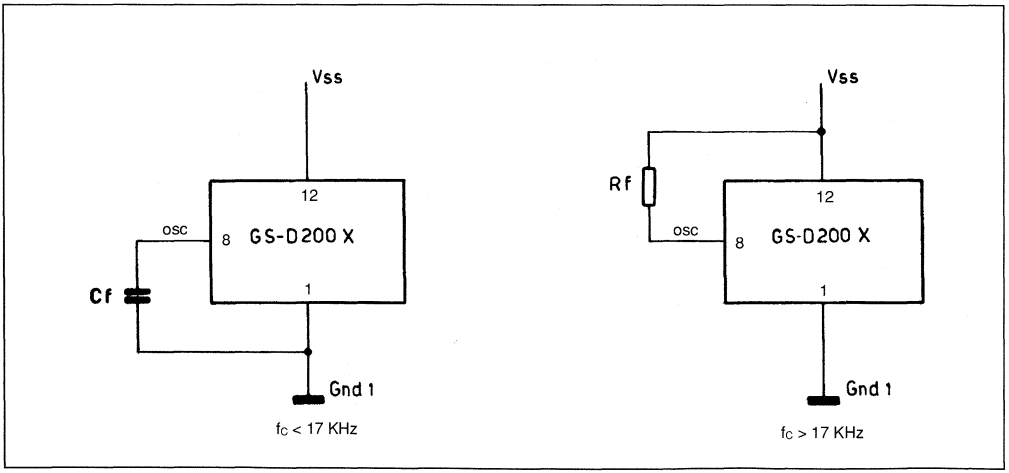


Figure 16: GS-D200 Free Air Derating Curve

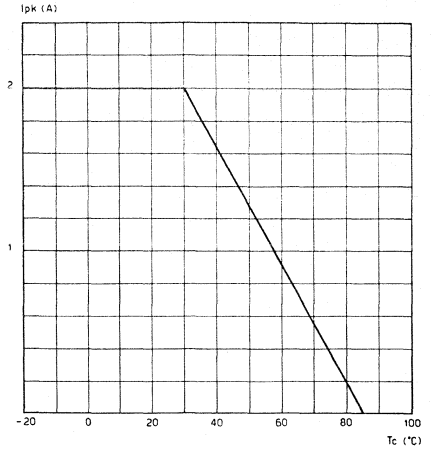
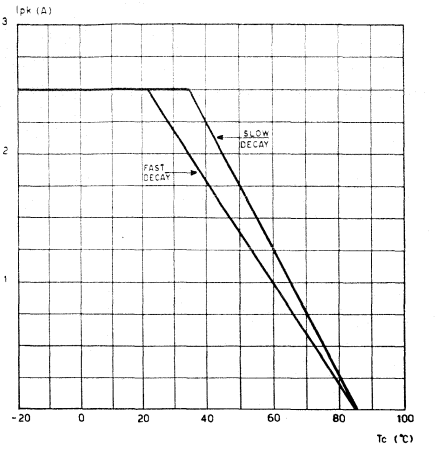


Figure 17: GS-D200S Free Air Derating Curve



MULTI MODULES APPLICATION

In complex systems, many motors must be controlled and driven. In such a case more than one GS-D200 or GS-D200 S must be used.
To avoid chopper frequencies noise and beats, all the modules should be synchronized.
If all the motors are relatively small, the fast decay may be used, the chopper frequency does not need any adjustement and fig. 18 shows how to synchronize several modules.

When at least one motor is relatively large a lower chopper frequency and a slow decay may be required: In such a case the overall system chopper frequency is determined by the largest motor in the system as shown in fig. 19.

Figure 18: Multimotor Synchronization. Small Motor and Fast Current Decay

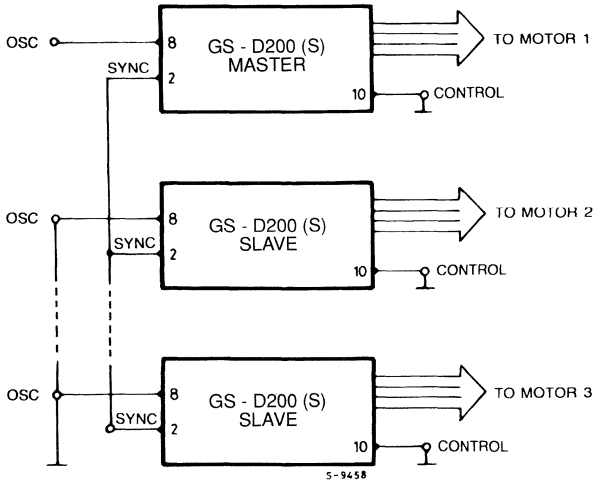
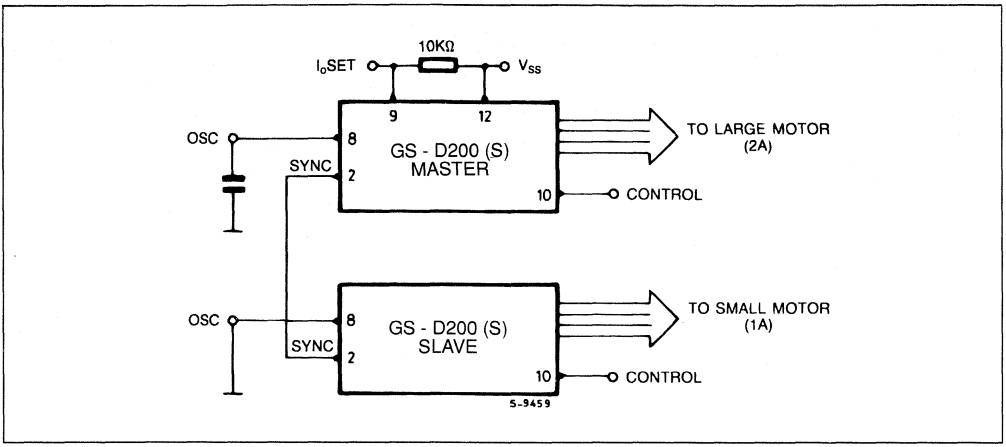


Figure 19: Multimotor Synchronization. Large and Small Motor. Slow Current Decay



THERMAL OPERATING CONDITIONS

In many cases the modules do not require any additional cooling because the dimensions and the shape of the metal box are studied to offer the minimum possible thermal resistance case-to-ambient for a given volume.

It should be remembered that these modules are a power device and, depending on ambient temperature, an additional heath-sink or forced ventilation or both may be required to keep the unit within safe temperature range. ($T_{case_{max}} < 85$ °C during operation).

The concept of maximum operating ambient temperature is totally meaningless when dealing with power components because the maximum operating ambient temperature depends on how a power device is used.

What can be unambiguously defined is the case temperature of the module.

To calculate the maximum case temperature of the module in a particular applicative environment the designer must know the following data:

– Input voltage

– Motor phase current

– Motor phase resistance

– Maximum ambient temperature

From these data it is easy to determine whether an additional heath-sink is required or not, and the relevant size i.e. the thermal resistance.

The step by step calculation is shown for the following example (GS-D200).

V_{in} = 40 V, I_{phase} = 1 A, R_{ph} Phase resistance = =10Ω, max. T_A = 50 °C

- Calculate the power dissipated from the indexer logic and the level shifter (see electrical characteristics):

$$P_{logic} = (5\ V \cdot 60\ mA) + (40\ V \cdot 20\ mA) = 1.1\ W$$

- Calculate the average voltage across the winding resistance:

$$V_{out} = (R_{ph} \cdot I_{out}) = 10\Omega \cdot 1\ A = 10\ V$$

- Calculate the required ON duty cycle (D.C.) of the output stage to obtain the average voltage (this D.C. is automatically adjusted by the GS-D200):

$$D.C. = \frac{V_{out}}{V_{in}} = \frac{10}{40} = 0.25$$

- Calculate the power dissipation of the GS-D200 output power stage. The power dissipation depends on two main factors:

– the selected operating mode (FAST or SLOW DECAY)

– the selected drive sequence (WAVE, NORMAL, HALF STEP)

FAST DECAY. For this mode of operation, the internal voltage drop is $Vsat_{source} + Vsat_{sink}$ during the ON period i.e. for 25 % of the time.
During the recirculation period (75 % of the time), the current recirculates on two internal diodes that have a voltage drop V_d = 1 V, and the internal sense resistor (0.5 Ω). For this example, by assuming maximum values for conservative calculations, the power dissipation during one cycle is:

$$P_{pw} = 1.1 \cdot [2\ V_{sat} \cdot I_{ph} \cdot D.C. + 2\ V_d \cdot I_{ph} \cdot (1 - D.C.) + 0.5 \cdot I_{ph}]$$

$P_{pw} = 1.1 \cdot [2 \cdot 1.8 \cdot 1 \cdot 0.25 + 2 \cdot 1 \cdot 1 \cdot 0.75 + 0.5 \cdot 1]$

$P_{pw} = 1.1 \cdot [0.9 + 1.5 + 0.5] = 3.19$ W

The factor 1.1 takes into account the power dissipation during the switching transient.

SLOW DECAY. The power dissipation during the ON period is the same. The RECIRCULATION is made internally through a power transistor ($V_{sat-sink}$) and a diode. The power dissipation is, therefore:

$P_{pw} = 1.1 \cdot [2\ V_{sat} \cdot I_{ph} \cdot D.C. + (V_{sat} + V_d) \cdot I_{ph} \cdot (1 - D.C.)]$

$P_{pw} = 1.1 \cdot [2 \cdot 1.8 \cdot 1 \cdot 0.25 + (1.8 + 1) \cdot 1 \cdot 0.75]$

$P_{pw} = 1.1 \cdot [0.9 + 2.1] = 3.3$ W

WAVE MODE. When operating in this mode the power dissipation is given by values of FAST and SLOW DECAY mode, because one phase is energized at any given time.

NORMAL MODE. At any given time, two windings are always energized. The power dissipation of the power output stage is therefore multiplied by a factor 2.

HALF STEP. The power sequence, one-phase-on, two-phase-on forces the power dissipation to be 1.5 times higher than in WAVE MODE when the motor is running. In stall condition the worst case for power dissipation is with two-phase-on i.e. a power dissipation as in NORMAL MODE.

The following table summarizes the power dissipations of the output power stage of the GS-D200 when running for this example:

	Wave	Normal	Half Step
Fast Decay	3.19 W	6.38 W	6.38 W
Slow Decay	3.30 W	6.60 W	6.60 W

- Calculate the total power dissipation for the GS-D200 :

$P_{tot} = P_{logic} + P_{pw}$

In this example, for slow decay and normal mode

$P_{tot} = 1.1 + 6.6 = 7.7$ W

- The case temperature can now be calculated:

$T_{case} = T_{amb} + (P_{tot} \cdot R_{th}) = 55 + (7.7 \cdot 5) = 93.5$ °C

- If the calculated case temperature exceeds the maximum allowed case temperature, as in this example, an external heat-sink is required and the thermal resistance can be calculated according to:

$$R_{th_{tot}} = \frac{T_{cmax} - T_{amb}}{P_{tot}} = \frac{85 - 55}{7.7} = 3.9\ °C$$

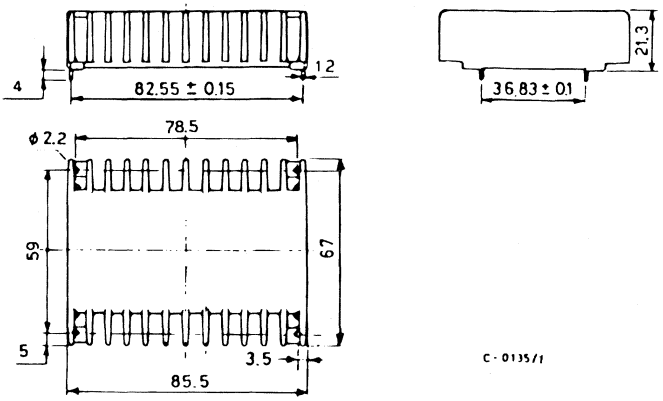
and then

$$R_{th_{hs}} = \frac{R_{th} \cdot R_{th_{tot}}}{R_{th} - R_{th_{tot}}} = \frac{5 \cdot 3.9}{5 - 3.9} = 17.7°C$$

The following table gives the thermal resistance of some commercially available heath-sinks that fit on the GS-D200 module.

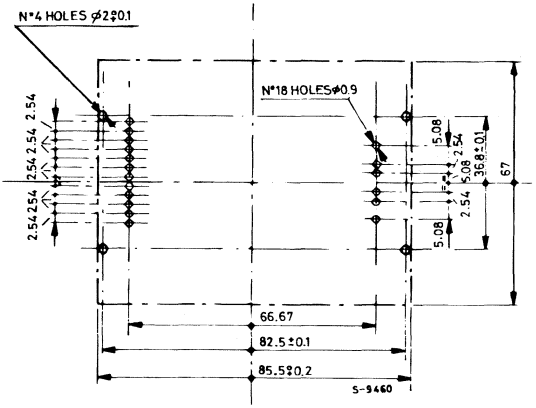
Manufacturer	Part Number	R_{th} (°C/W)	Mounting
Thermalloy	6177	3	Horizontal
Thermalloy	6152	4	Vertical
Thermalloy	6111	10	Vertical
Fischer	SK18	3	Vertical
Assman	V5440	4	Vertical
Assman	V5382	4	Horizontal

MECHANICAL DATA



Dimensions in mm

MOTHER BOARD LAYOUT



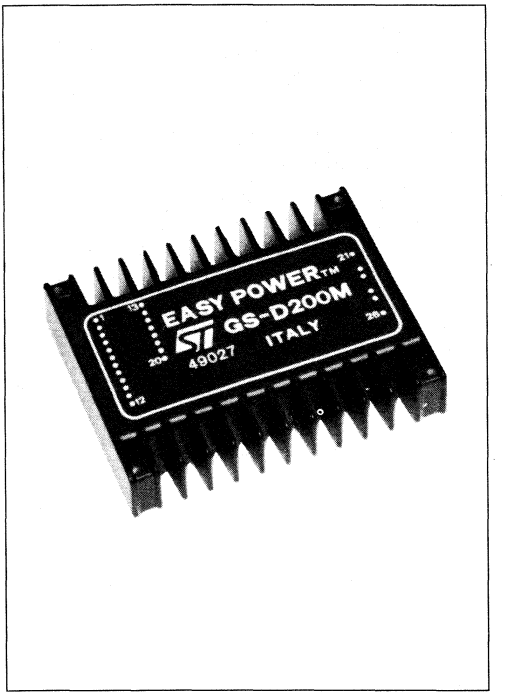
SGS-THOMSON MICROELECTRONICS

GS-D200M

2.5A MICROSTEP DRIVE MODULE FOR STEPPER MOTORS

FEATURES

- Wide supply voltage range (12 to 40V)
- High peak phase current (2.5Apk)
- 1/128 phase current resolution
- Logic signals TTL/CMOS compatible
- Direct interface to microprocessors
- Chopping regulation of the phase current
- Programmable peak motor phase current
- Remote inhibit/enable
- Thermal protection



DESCRIPTION

The GS-D200M is a module specifically designed to drive bipolar stepper motors in the microstep mode.
The unit interfaces the microprocessor as a parallel port and two phase, bipolar, permanent magnet stepper motor.
The phase current (up to 2.5Apk) is controlled in a chopping mode by using a mixed recirculation method that allows the best overall system performance.
The microstep per step rate is determined by the microprocessors software according to the application requirement: the maximum resolution of the phase current is 1/128 of the peak value.
The two phases of the motor are driven by two internal and separate H-bridges made of powerfets to minimize the commutation and conduction losses.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
V_{SS}	DC Supply Voltage	7	V
T_{stg}	Storage Temperature Range	–40 to +105	°C
T_{cop}	Operating Case Temperature Range	–20 to +85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
V_S	DC Supply Voltage		12		40	V
V_{SS}	DC Logic Supply Voltage		4.75	5	5.25	V
I_S	Quiescent Supply Current			20		mA
I_{SS}	Quiescent Supply Current	V_{SS} = 5V		60		mA
I_{ph}	Phase Peak Current				2.5	A
V_{dr}	Voltage Drop	I_{ph} = 2A			2.5	V
V_i	Logic Input Voltage	Low High	2		0.8 V_{SS}	V
V_o	Logic Output Voltage	Low High	2		0.8 V_{SS}	V
t_{off}	Recirculation Time			32		µs
D_s	Select and Data to Strobe Set Up Time		100			ns
D_h	Select and Data to Strobe Hold Time		600			ns
S_{tpw}	Strobe Pulse Width		700			ns
C_{srt}	Data Uptdating Frequency				400	kHz
R_{th}	Case to Ambient Thermal Resistance			5		°C/W

Figure 1. Signals Timing

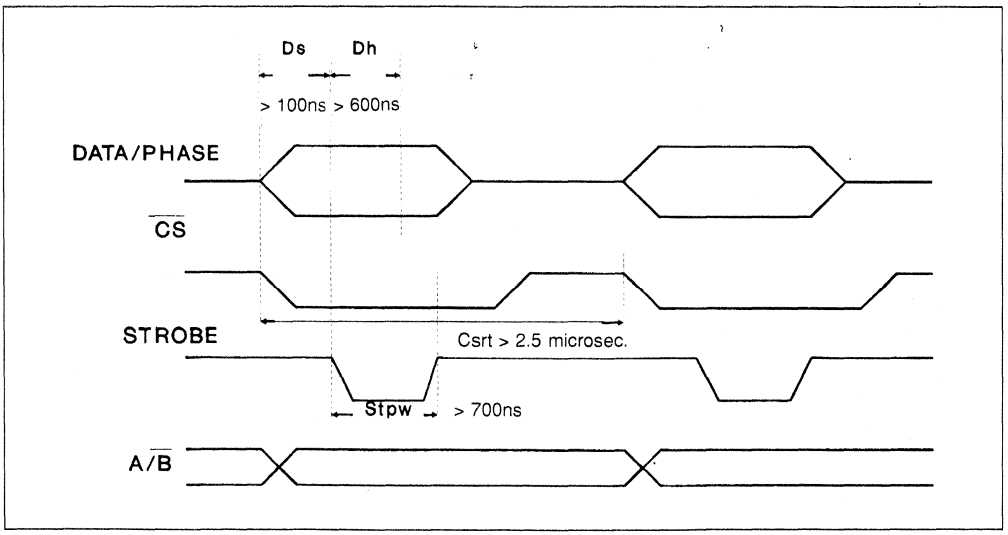


Figure 2. GS-D200M Equivalent Block Diagram

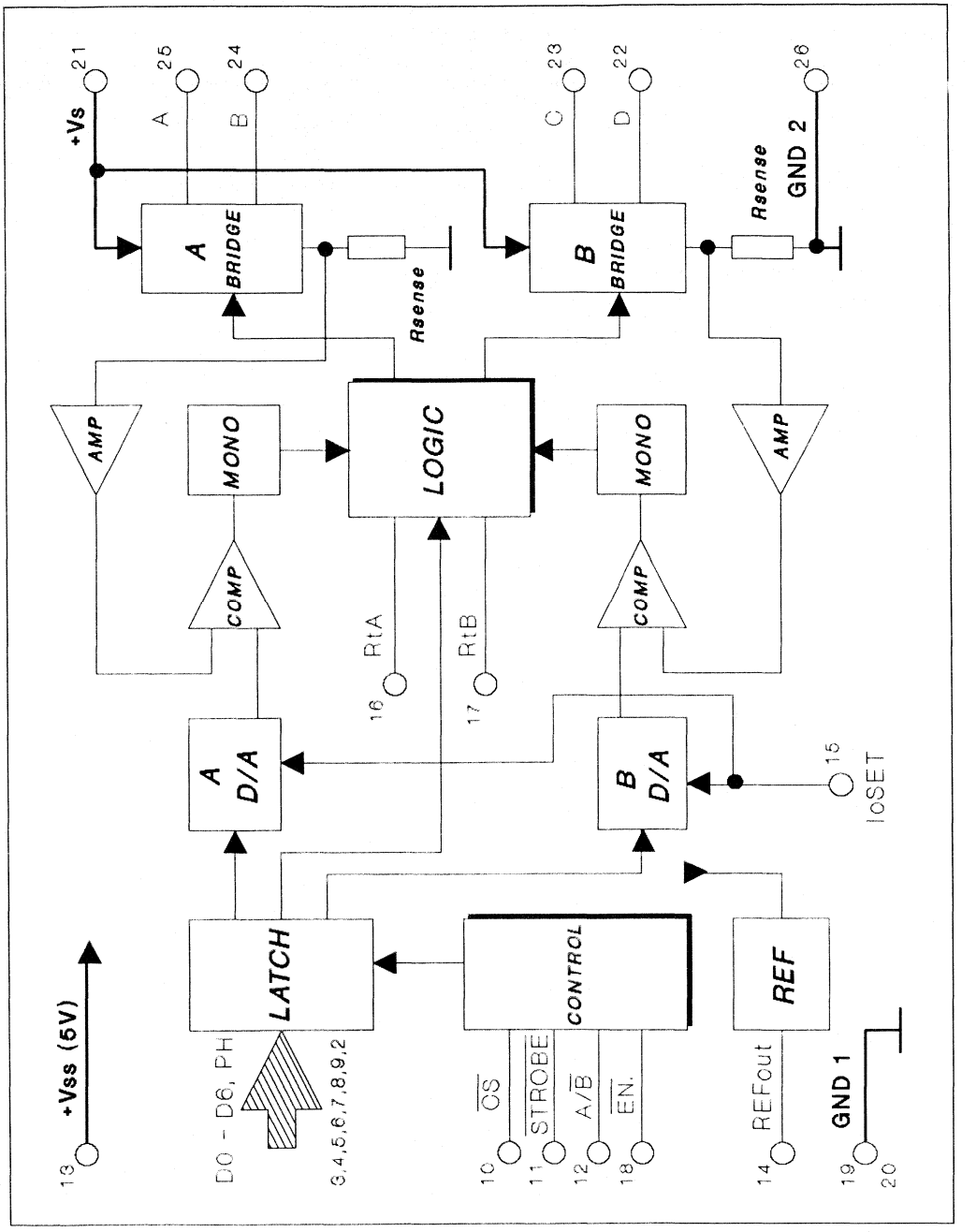
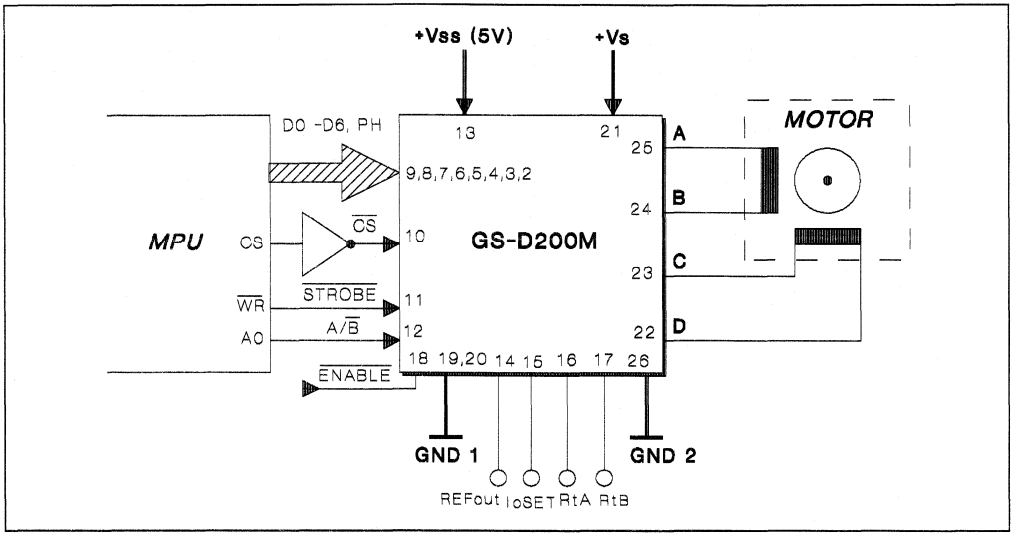


Figure 3. Interfacing the GS-D200M to a Microprocessor and to Stepper Motor.



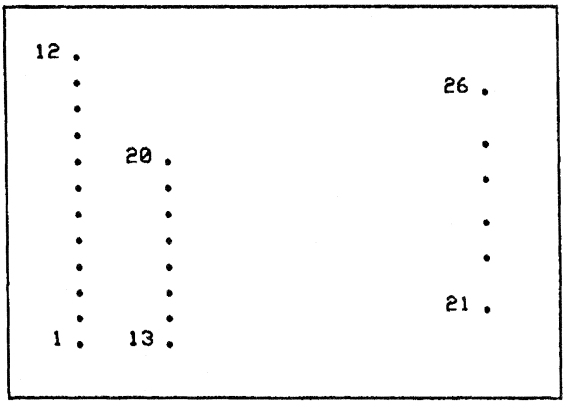
PIN DESCRIPTION

Pin	Function	Description
1	Vss	5V supply input. Maximum voltage must not exceed 7V.
2	Phase	Phase logic information. This input, normally connected to bit7 of the data bus, determines the direction of conduction for the addressed power driver.
3	D6	Data inputs. The value present on these inputs is stored into the addressed DAC latch during the high-to-low transition of the STROBE input.
4	D5	
5	D4	
6	D3	
7	D2	
8	D1	
9	D0	
10	CS	Chip select input. Data can be stored into DAC latches only when CS is low.
11	STROBE	Latches strobe command. The data present on the bus is transferred to the addressed DAC latch on the high-to-low transition of this input.
12	A/B	DAC latch selection input. When high the A DAC is addressed.
13	Vss	5V supply input. Maximum voltage must not exceed 7V.
14	REFout	Reference output. A 2.5V reference voltage is available on this pin for phase current setting.
15	Ioset	Current setting input. A resistor connected between pin 14 and this pin sets the phase current peak value.
16	RtA	Phase A ripple current setting resistor.

PIN DESCRIPTION (Cont'd)

17	RtB	Phase B ripple current setting resistor.
18	DISABLE	Power driver disable logic input. When high or unconnected causes the output power stages to float.
19	GND	Return path for the logic.
20	GND	Return path for the logic.
21	Vs	Module and motor supply voltage. Maximum voltage must not exceed 40V.
22	D	D output. A motor winding is connected between D and C outputs.
23	C	C output. A motor winding is connected between C and D outputs.
24	B	B output. A motor winding is connected between B and A outputs.
25	A	A output. A motor winding is connected between A and B outputs.
26	GND1	Ground path for the motor current.

Figure 4. Connection Diagram (Bottom view)



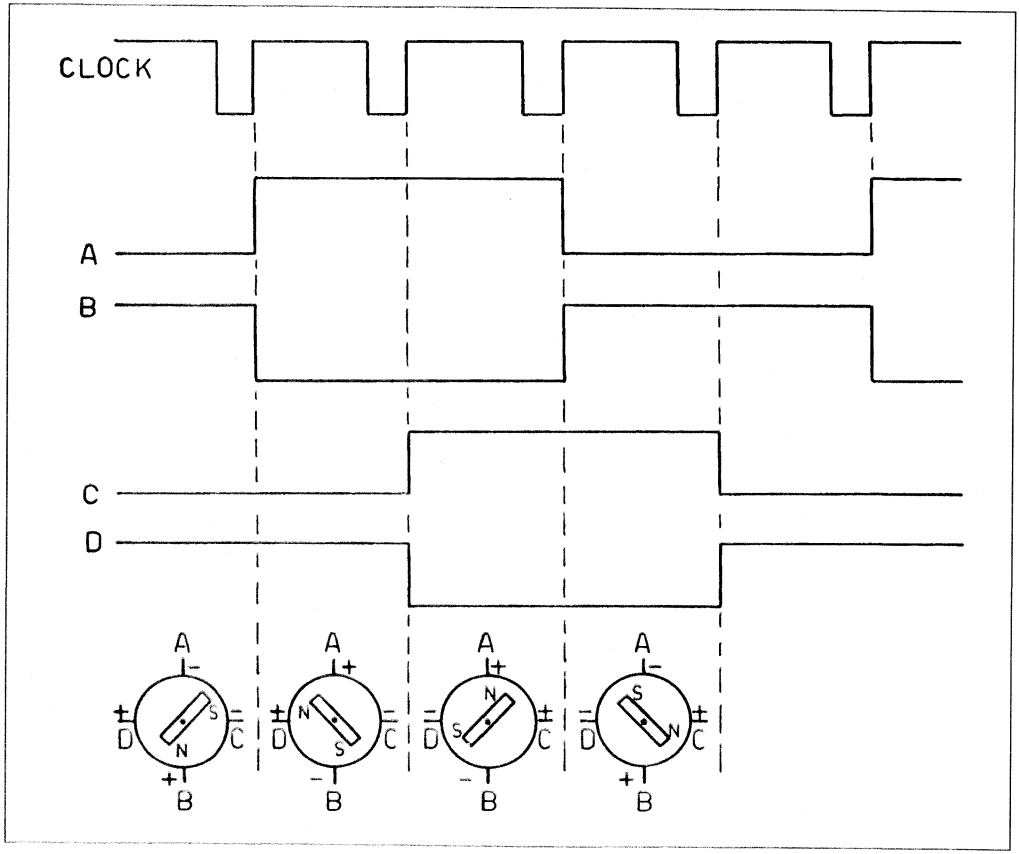
MICROSTEPPING BASICS

Stepping motors have the advantage to be usable in an open-loop system's architecture that controls speed and positioning.
However, they exibit also two major limitations on achievable resolution and mechanical resonance.
The microstepping mode of operation can pratically eliminate these two limitations.

Resolution Improvement Through Microstepping

Basically, microstepping is achieving finer electrical resolution than is offered by conventional full-step and half-step driving.
A typical and simplified two-phase-on (normal mode) drive of a stepping motor is shown in fig. 5.

Figure 5. Two-Phase-on (Normal mode) Drive.



SGS-THOMSON MICROELECTRONICS

Figure 6. Phase Current for Four Full Step.

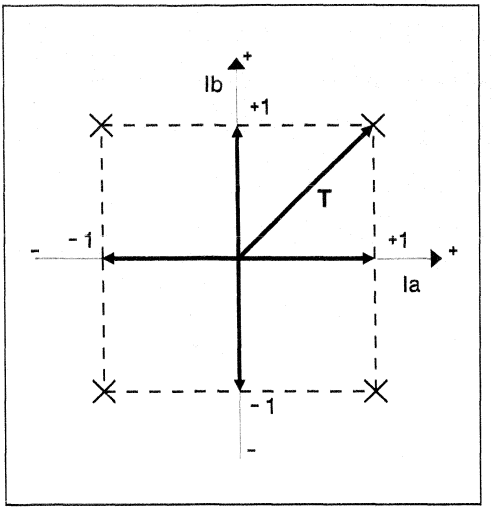
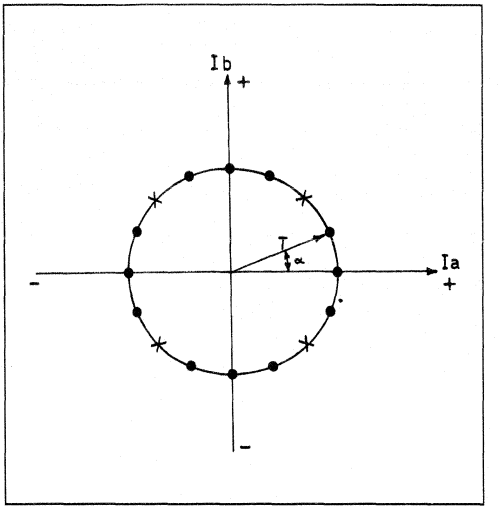


Figure 7. Microstepping



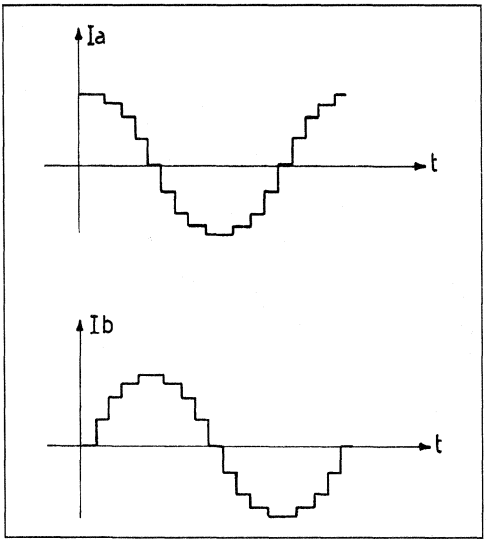
A full cycle (360 electrical degrees) of the driving signals generate exactly four full steps (one torque cycle).
One full step is, therefore, equivalent to 90° of electrical signal.
This is equivalent to have two windings with current I_a and I_b mechanically placed at 90° along x, y, axis as shown in fig. 6. The two currents have discrete values: 0, +1, −1.

The torque T is proportional to the current in the motor winding and the resultant torque is the vector sum of the individual torques produced by phase a and phase b current. The motion direction is determined by the direction of the current flow.
From fig. 6, it is evident that to reduce the mechanical step angle, the torque vector should have more than the 4 position indicated by the crosses.
The ideal situation would be for the resultant torque vector to fall in a unit circle for all positions as shown in fig. 7.

This would occur if the winding current rather than square waves as shown in fig. 5 are orthogonal functions, such as sine and cosine.

In fig. 7 four microsteps/step are shown. The correspondent phase currents are shown in fig. 8.

Figure 8. Phase Current Profile for 4 microsteps/step



Substantially, the microstepping mode is obtained by subdividing each full step into a fixed number of microsteps; this, in turns, is obtained by driving the motor winding with intermediate current levels.

The higher the number of intermediate levels, the closer the torque vector will follow the unity circle of fig. 7. However, the mechanical characteristics of the motor in response to these intermediate levels will make useless a very high number of levels: in the GS-D200M, the maximum number of microsteps/step is fixed at 128.
Real motors have multiple poles pairs to reduce the step angle to a few mechanical degrees for a full step.
Most steppers have resolution of 200 steps/revolution i.e. 1.8° per full step.
The finer electrical resolution obtained by 128 microsteps/step is more than adequate for practical application.

Mechanical Resonance Improvement

Microstepping can help smooth out the mechanical motion of a stepper motor.
Large pulse drive waveforms encountered in full step mode create mechanical forces that may translate into mechanical resonances in a positioning system.

These resonances are also depending on load characteristics and they are difficult to control because of low damping capability of stepper motors. Resonance may cause loss of synchronization i.e. the motor can skip or gain a step.
Microstepping reduces large current transients and it is beneficial in reducing or eliminating the resonance problem.

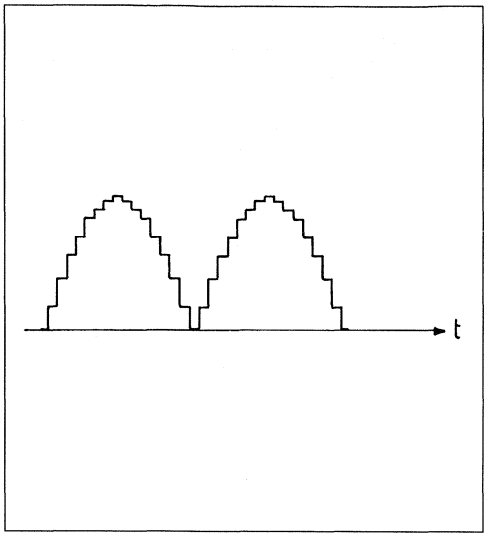
GS-D200M DESCRIPTION

The block diagram of the module is shown in fig. 1. The GS-D200M implements all the functions needed to achieve intelligent power drive of a stepper motor in a microstep mode.

The two functions, sine and cosine, are digitized, stored in a look-up-table of the external microprocessor and supplied to the module.
The magnitude only of the two signals is sufficient since the software can take into account the sign i.e. the direction.
The typical waveform has the form of a rectified sine wave as shown in fig. 9.

The current waveform can also be modified, via software, to take into account motor resonance and damping.

Figure 9. Digitized, Rectified Sine Wave



The GS-D200M includes two data latches that can be easily interfaced to a microprocessor, either to an I/O port or directly on the data bus of the system. Using these two latches, the microprocessor can indipendently set both the level and the direction of the current flow in each winding of the stepper motor.

In the 8 bit word of the microprocessor, 7 bits can be used to digitize the sine, cosine functions so achieving 128 levels while the Most Significant Bit can be used as a sign bit (direction).
The 7 bits are indicated as D0.....D6 while the MSB is named phase (Ph).

Three additional pins are present on the GS-D200M for the micro data processing. The data of the microprocessor can be stored into the latches just when the Chip Select pin (CS) is low. The data transfer into the selected modules occurs during the high-to-low transition of the STROBE pin.
The proper latch inside the GS-D200M is selected by the A/B pin: when high the A latch is addressed.
The conversion of the digital information in the latch into an analog signal that sets the current level is performed by a couple of 7-bit D/A converters.
The two analog signals, after proper conditioning for current control, drive two H-powerfet bridges that can directly interface the two motor windings.

CURRENT CONTROL INSIDE THE GS-D200M.

The peak current delivered by the H-bridges can be programmed externally up to 2.5Apk max.
To this purpose a resistor must be connected between the pins REF_{out} and I_{oset}. This resistor fixes the current to voltage conversion of the two D/A converters that employ a current switch approach to reach a setting time of less than 2µs.
The value of the current programming resistor is given by:

$$R_i = (3.2/Ipk - 1)\ k\Omega.$$

where Ipk = phase peak current.

The minimum value of Ri is 280Ω that corresponds to the maximum current of 2.5Apk.
The phase current level control of the GS-D200M is achieved by a chopping mode.
The Pulse Width Modulation (PWM) that could be used to achieve a chopping mode can exhibit some stability problems if the switching duty-cycle exceeds 50%.
For this reason the GS-D200M uses Frequency Modulation switching control.
This techniques uses fixed off duration from the moment the output current exceeds the reference level established by the D/A converters.

Referring to the block diagram of fig. 2, the phase current of each bridge is sensed by R_{sense}, amplified and fed to one input of a comparator, being the other input connected to the D/A output.
When the phase current exceeds the level fixed by the D/A, a monostable pulse generator is triggered by the comparator and it disables the H-bridge for a time duration of 32µs that is fixed inside the module. During the off-time the current decays. At the end of the off-time, a new cycle is started, the H-bridge is enabled again and the phase current starts to rise again according to the L/R time constant of the motor winding. The on-time depends on the supply voltage, the L/R constant and the Electromotive force of the motor.
Therefore the total time (on+off) is never constant and the switching frequency is self adapting to the dynamic behaviour requested by microstepping.

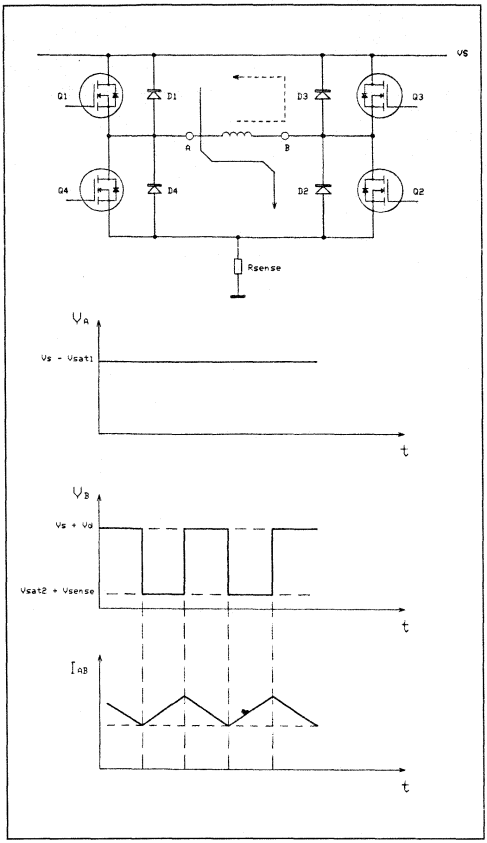
The amount of current decay during the fixed off-time depends on the method used to recirculate the current: slow or fast.

The method for slow decay is shown in fig. 10. During the on-time both Q1 and Q2 are on. The total voltage V_{AB} applied to the winding is:

$$(V_S - V_{sat1}) - (V_{sat2} + V_{sense})$$

where V_S = supply voltage, V_{sat1} = saturation voltage of Q1, V_{sat2} = saturation voltage of Q2, V_{sense} = voltage drop on the sensing resistor.
The current flow is indicated by the solid line of fig. 10.

Figure 10. Chopper Control with Slow Decay



If, during the off-time, Q2 is switched off, the current stored in the winding will flow through D_3 (see dotted line of fig. 10) and V_B will raise the V_S+V_d being V_d the voltage drop of D_3.
The total voltage applied to the winding during the off-time is, therefore, $V_{sat1}+V_d$ and the current decay is slow. The method for fast decay is shown in fig. 11.

During the on-time both Q1 and Q2 are ON as in the previous case.
During the off-time both Q1 and Q2 are switched OFF and the current flows through D_4 and D_3 (dotted line of fig. 11).
During the off-time the voltage applied to the winding is:

$$(V_S + V_d) - (V_d + V_{sense})$$

Figure 11. Chopper Control with Fast Decay

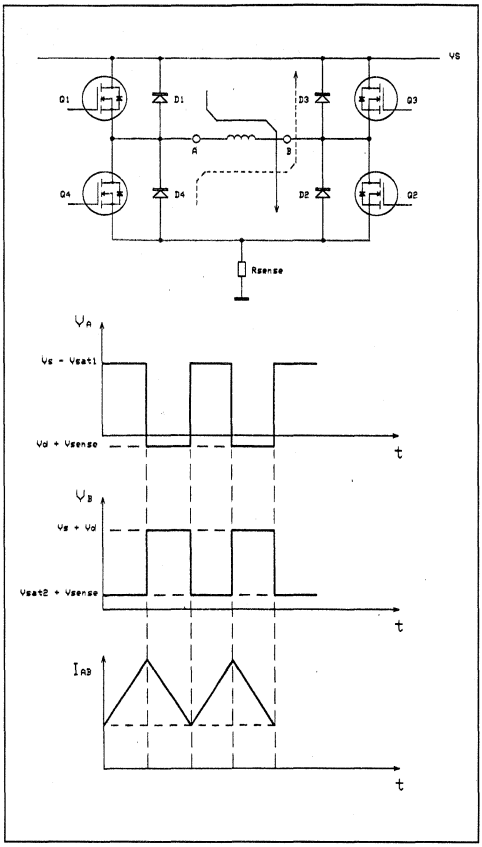
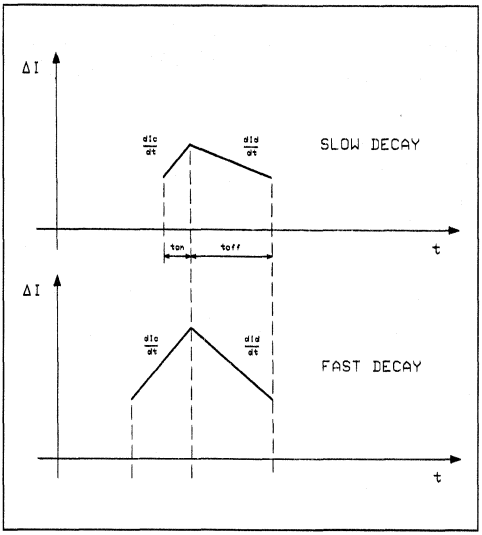


Figure 12. On-time for Slow and Fast Decay



If the V_d and V_{sense} are negligible compared to V_S, the slope of the current decay is practically equal to the slope of the current rise during the on-time.
The decay can be very fast depending on the value of V_S, R, L and EMF.
Both methods (slow, fast decays) have advantages and disadvantages.
The disadvantage of the fast decay is a higher ripple current due to the chopping action.
The disadvantage of slow decay is the reduced on-time.
In steady state conditions, the amount of decay during off-time is equal to the amount of current rise during the on-time.
Fig. 12 shows a qualitative behaviour of the ripple current in the two cases.
During the off-time the slope dI_d/dt are different because of the different voltage applied to the winding during recirculation.

During the on-time the slope dI_c/dt is the same on both the cases. Being the ripple lower in the slow decay, it takes a shorter time during the on-phase to reach the peak current.

In some application where there is a low back EMF, as it will occur when trying to hold a position and V_{emf} becomes zero, or high supply voltage, the minimum achievable on-time for a slow decay can set a current level that is above the desired current set by the D/A converter.

For a given minimum average phase current I_m, the dutycycle (t_{on}/t = D) is given by the following formula:

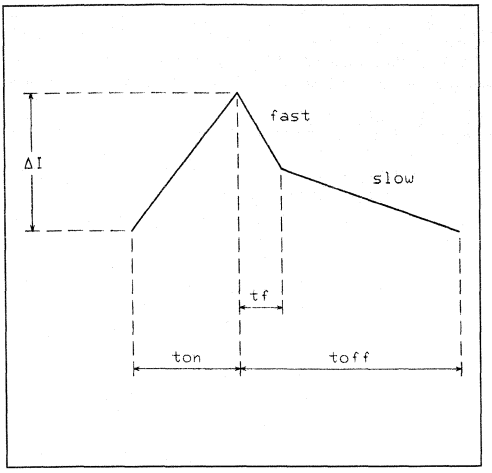
$$I_m = \frac{(V_S - V_{sat1})\,D + (D-1)\,V_d - V_{emf} - V_{sat2} - V_{rsense}}{R_{motor} + R_{sense}}$$

If I_m is very low, D may be prevented to be very low by various delays, etc.
To overcome these problems and to add flexibility to the GS-D200M a mixed decay (recirculation) method as been adopted.

During the off-time, initially a fast decay is imposed on the phase current. The off-time is then completed by a slow decay.
The ripple current behaviour is shown in fig. 13.

An internal monostable is triggered when the current reaches the peak current.
This monostable switches off both Q1 and Q2 (see fig. 11) so forcing a fast decay for a time t_f.

Figure 13. Mixed Decay Method



After t_f, Q1 is turned on again to complete the off-time in a slow mode.

The fast decay time t_f can be programmed by two resistor connected between the R_{tA} and R_{tB} pins to V_{SS} (+5V).
The value of these resistors is given by:

$$R_{tA}, R_{tB} = \left(\frac{t_f}{0.7} - 0.1\right) k\Omega$$

where t_f is in microseconds.

The GS-D200M User is therefore free to select the proper current ripple value that best fits to his/her needs.

USER NOTES

GS-D200M - DAC Operation

GS-D200M has two internal DACs used to set the current in phase AB and in phase CD. The internal DACs are named A and B:

- DAC A set the current in phase CD (pins 23,22)
- DAC B set the current in phase AB (pins 25,24).

To load a digital word, present on D0 - D6 inputs, on DAC A you have to:

- set D0 - D6 inputs, on DAC A (D0 is LSB)
- set input A/B to logic level high
- set CS input to logic level low
- give a STROBE signal.

The digital word set the current at a value given by the relation:

$$Iout = Ipk \times \frac{N}{127}$$

where N is the digital value (0 to 127) and Ipk is the maximum current set by means the resistor Ri with the relation:

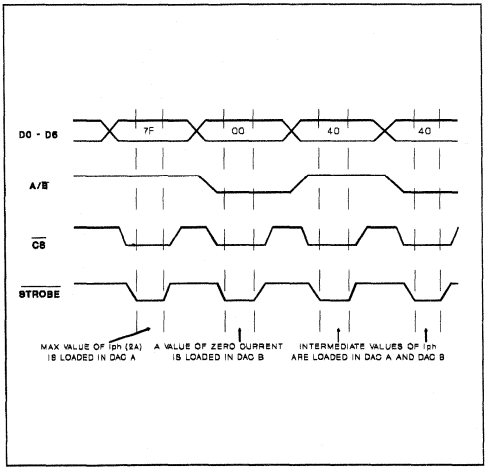
$$Ri = \frac{3.2}{Ipk} - 1 (k\Omega)$$

This means:

- if D0 -D6 are all zeros the phase current is 0 (zero)
- if D0 - D6 are all ones the phase current is the maximum value set by Ri
- other combinations on D0 - D6 give a phase current proportional to the digital value.

Example: Iph= 2A, Ri= 0.6kΩ

Figure 14.

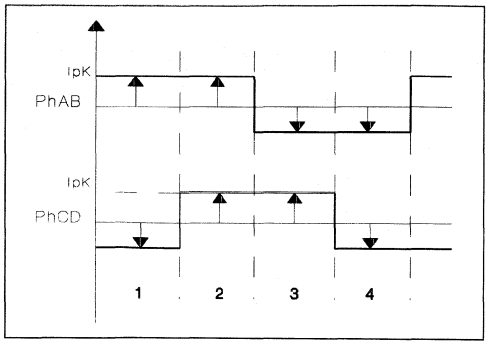


Phase Input (pin 2)

This pin is used to set the direction of the current in the addressed power driver. Usually this pin is connected to the data bus pin named D7. When this input is at logical high level, the current flows from B to A (phase AB) and from C to D (phase CD); when it is at logical low level the current flows from A to B (phase AB) and from D to C (phase CD).

Example: suppose to simulate a full-step moving. The current waveforms present on the phase outputs are:

Figure 15.



The arrows show the direction of the current in the phases:

- when phase (D7) = 1

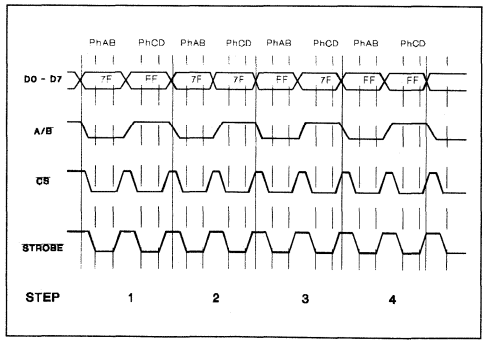
- when phase (D7) = 0

As you can see, the current changes from the maximum value in one way to the maximum value in the opposite way: so the digital inputs D0-D6 will be always at logic level high (7F).

The sequence the user has to load to have the full step mode is:

step	Ph AB			Ph CD		
	D7	D6-D0	D7-D0	D7	D6-D0	D7-D0
1	0	7F	7F	1	7F	FF
2	0	7F	7F	0	7F	7F
3	1	7F	7F	0	7F	7F
4	1	7F	7F	1	7F	FF

Figure 16.



GS-D200M Inhibit/Enable

One pin (DISABLE) is provided to put the two H-bridges in a floating mode.
To operate the GS-D200M this pin must be pulled down.

Supply Voltage

The recommended operating maximum supply voltage V_S is 40V inclusive of the ripple voltage, while for V_{SS} the voltage is 5V±5%.
The two supply voltages must be correctly sequenced to avoid erroneous conditions of the power stages.

The power-up and power-down sequences are:

Power-up
1) V_{SS} (5V) is applied with Disable = High
2) V_S (the motor supply voltage) is applied
3) After 50 ms (power-on reset time) the phase current level can be programmed to the proper level
4) Disable input is brougth low.

Power-down
1) Disable is brougth High
2) V_S is switched off
3) V_{SS} is switched off.

Case Grounding

The module case is internally connected to pin 19, 20 and 26. To obtain an effective EMI shield, the PCB area below the module can be used as a sixth side shield.

Thermal Characteristics

The case-to-ambient thermal resistance of the module is 5°C/W. This produces a 50°C temperature increase of the module surface for a 10W of internal power dissipation. According to ambient temperature and/or to power dissipation, an additional heatsink or forced ventilation may be required.

Supply Line Impedance

The module has an internal capacitor connected accross the supply pins to assure the circuit stability. This capacitor cannot handle large values of high frequency ripple current, and it is permanently damaged if the primary voltage source impedance is not adequate.

The use of a low ESR, high ripple current 470µF capacitor located as close to the module as possible is recommended. Suitable units are the SPRAGUE type 672D, the SPRAGE 678D, the RIFA type PEG 126 or any equivalent unit.
When space is a limit, a 22µF ceramic multilayer capacitor connected across the module input pins must be used.

Module Protection

The GS-D200M outputs are protected against occasional and permanent short circuits of the output pins to the supply voltage.
The thermal protection is activated when, for any reason, the internal junction temperature reaches 150°C. The unit restarts to operate as soon as the junction temperature falls below 130°C.

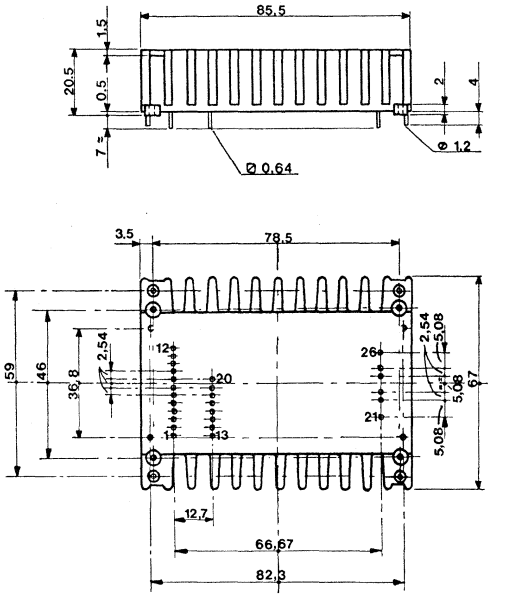
Motor Connection

The motor is usually quite far from the module and long cables are needed to connect the two. The use of a twisted pair cable with appropriate cross section for each motor phase is recommended to minimize DC losses and RFI problems.

Unused Inputs

All the GS-D200M logic inputs, excluding the data-bus, have a resistive pull-up, and they are in a high logic state when unconnected.

CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm

Bottom view

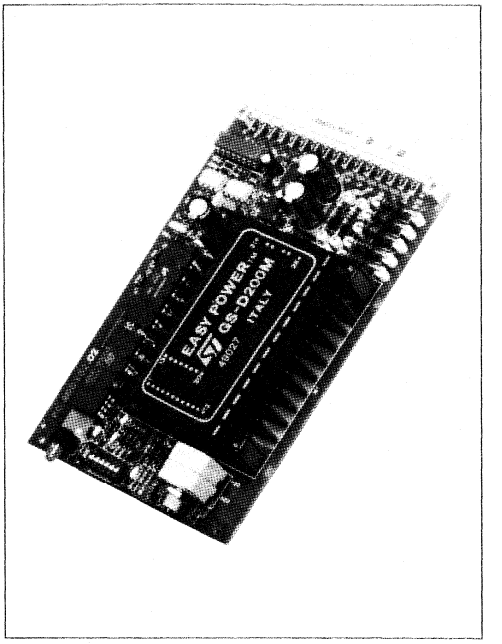
SGS-THOMSON MICROELECTRONICS

GS-D250M

2.5A MICROSTEP DRIVE BOARD FOR STEPPER MOTORS

FEATURES

- 2.5A/phase peak current
- 5, 10, 25, 45, 90, 100, 127, microsteps/step selection
- Full step selection possibility
- User programmable phase current
- User programmable phase current ripple
- Automatic ripple reduction at rest
- 4/8 wires motor drive
- Step clock in excess of 140kHz
- Single unregulated supply voltage
- TTL, 12V, 24V programmable input level
- Input signal galvanic isolation
- Thermal protection



DESCRIPTION

The GS-D250M is a single-Europe board for microstepping drive of 4/8 wires stepping motors.
Thanks to a very large number of embedded functions, the interfaces to the external environment are reduced to a minimum: just three commands are needed as inputs (step clock, direction, enable) and the outputs can drive directly the stepping motor windings.
The availability of user's selectable hardware allows a very high flexibility to meet all possible application needs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
I_I	Logic Input Current	30	mA
I_O	Logic Output Current	10	mA
T_{stg}	Storage Temperature Range	-20 to +85	°C
Thop	Max Operating Heatsink Temperature (GS-D200M)*	+85	°C

* Thermal protection intervention @ T_h 90°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit
V_S	DC Supply Voltage		12		40	V
I_i	Logic Input Current **			10		mA
V_o	Logic Output Voltage (TTL compatible)	Low High	 2	 2	0.8 5	V
I_{ph}	Phase Peak Current*			0.5	2.5	Apk
f_c	Clock Pulse Frequency				140	kHz
V_{is}	Isolation Voltage		500			Vdc

Note: The unit requires an input filtering capacitor 4700µF/50V, whit low ESRand located as close as possible to the board

* Output shorts protection phase-to-phase and phase-to-supply

** TTL, 12V, 24V Programmable input voltage level.

Figure 1. Signals Timing

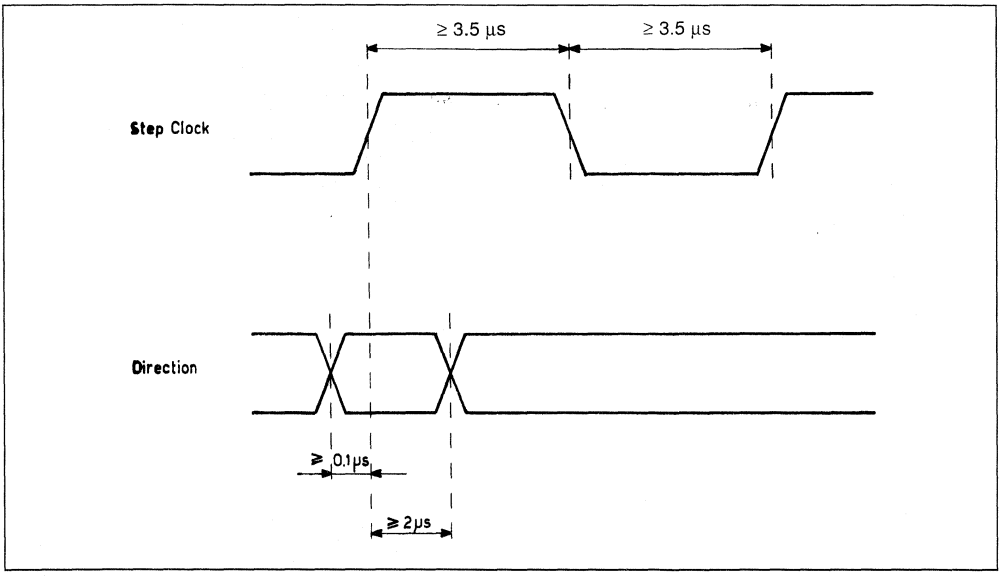
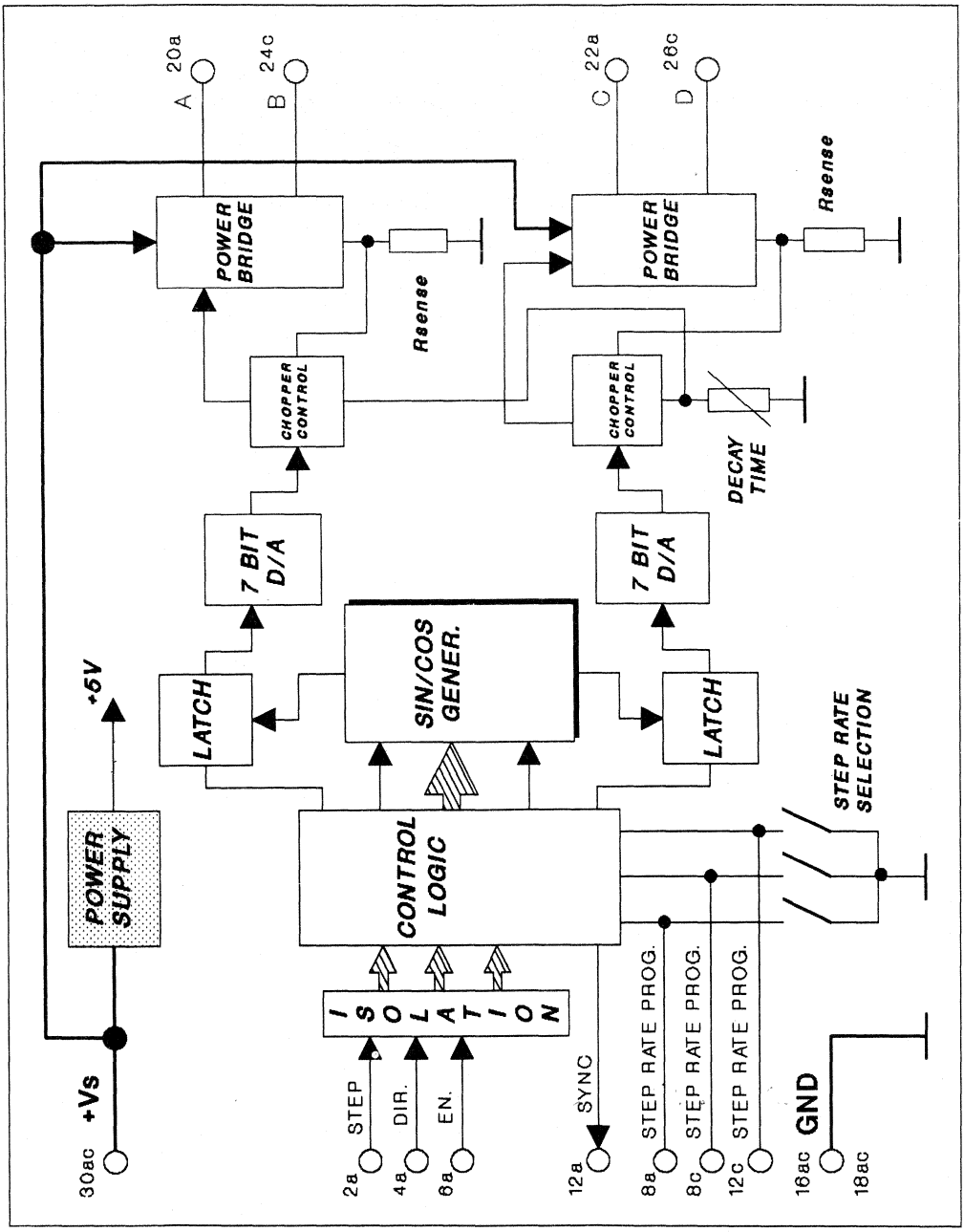
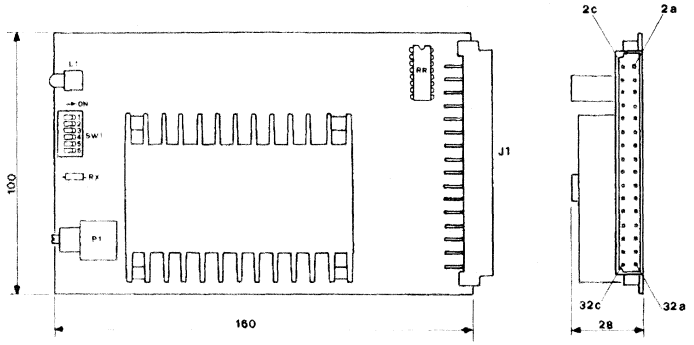


Figure 2. GS-D250M Block Diagram



CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm

GS-D250M BUS CONNECTOR PINS DESCRIPTION

The GS-D250M uses a 32 pins (16+16) DIN 41612 - VG95324 male connector

Row a	Pin	Row c
Step pulse input	2	Step pulse return
Direction input	4	Direction return
Disable input	6	Disable return
Microsteps/step programming	8	Microsteps/step programming
Not used	10	Not used
Sync Output	12	Microsteps/step programming
Not used	14	Not used
Supply ground	16	Supply ground
Supply ground	18	Supply ground
Phase A output	20	Not used
Phase C output	22	Not used
Not used	24	Phase B output
Not used	26	Phase D output
Not used	28	Not used
Supply voltage	30	Supply voltage
Not used	32	Not used

GS-D250M hardware available commands.

SW1, SW2, SW3	Microsteps/step programming
SW4	Selection of step clock transition
SW5	Direction polarity selection
SW6	Current ripple reduction at rest
Rx	Maximum peak current setting
P1	Phase current ripple programming
RR	Resistor array for logic level setting

GS-D250M DESCRIPTION

The GS-D250M single-Europe board has been designed by taking into account the maximum semplicity and flexibility in use.
It is based around the GS-D200M (microstep drive module, see the relevant data sheet) and it implements all the functions needed for a microstepping signal generation, so reducing the burden of external microprocessors, and the power stage to drive the stepper motor windings.
In its simplest application, the GS-D250M needs just three commands inputs: step clock, direction, disable.
Because this extreme semplicity could prevent the adaptability to different types of application, hardware selectable options are offered to the user to best program the board to his/her needs.
The various functions are described in the following.

Supply Voltage

The supply voltage can have any value between 12V and 40V maximum. No well regulated DC voltage is needed.
The supply voltage must be connected between pins 30a, 30c (positive rail) and 16a, 16c, 18a, 18c (negative rail).
The GS-D250M is permanently damaged by a supply voltage larger than 42V. The recommended maximum supply voltage is 40V.

During the phase current control by chopping method, the phase current is returned to supply voltage at each fast recirculation period. These current pulses can bring the supply voltage well above the recommended 40V max if the output impedance of the power supply feeding the GS-D250M is not adequately low.
A 1000μF/50V capacitor with low ESR at high frequency should be connected as close as possible to the supply voltage pins to provide a low impedance path for the recirculating current pulses.

An internal step-down switch mode regulator provides the 5V/± 5% requested by the internal logic blocks and it provides an automatic reset at POWER ON.
The POWER ON is indicated by on LED available of the front edge of the board.

Microstep Programming

The microsteps/step can be programmed by the user.
The digitized sine and cosine functions required for a microstepping control are stored in Lock-Up-Table inside the board. The user has two options to select the adequate number of microsteps/step.

Microstep programming by hardware

Three switches (SW1, SW2, SW3) are available on the front edge of the board.
The following table defines the microsteps/step rate.

SW1	SW2	SW3	Microsteps/step
OFF	OFF	OFF	127
ON	OFF	OFF	100
OFF	ON	OFF	90
ON	ON	OFF	45
OFF	OFF	ON	25
ON	OFF	ON	10
OFF	ON	ON	5
ON	ON	ON	1

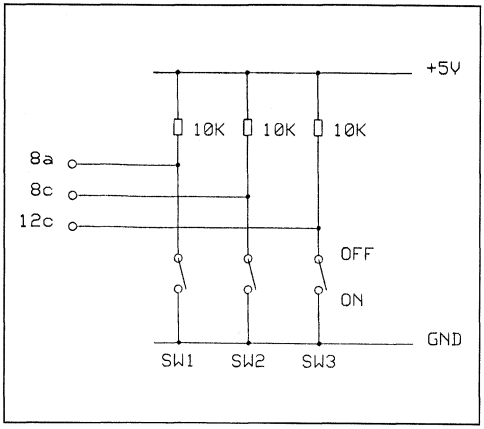
The last condition defines a full step operation of the board.
The switches are in the OFF condition when the knob is pulled versus the board edge.

Microstep programming by microprocessor software

The microsteps/step rate can also be changed on-the-fly by using the three logic inputs available on the bus connector (pin 8a, 8c, 12c).
These pins correspond, respectively, to SW1, SW2, SW3.
If the selection is performed remotely, the switches SW1, SW2, SW3 must be in the OFF position.

Fig. 3 clarifies the interaction between internal switches and external command signals.

Figure 3. Remote Microstepping Programming



The remote change from one rate to another cannot be implemented asynchronously by it must be forced only when the phase currents are respectively at 45 and 135 electrical degrees.
This state is signaled by the SYNC pin (12a).
The correct sequence for on-the-fly change of the microsteps/step is as follows:

- read the active edge of the step clock after a delay of 3µs
- read the status level of the SYNC pin (high or low)
- if the status level has changed after 3µs, program the new microsteps/step
- new microsteps/step rate programming must be completed before the arrival of the next step clock command to assure the correct system synchronization.

Setting of the Active Step Clock Transition

The step clock applied between pins 2a and 2c can be active i.e. advancing the motor by one step on the rising or falling edge of the clock pulse.
The user can select the proper transition condition by setting the SW4 switch according to the following table:

SW4	TRANSITION
ON	Low-to-high active step clock transition
OFF	High-to-low active step clock transition.

Setting of the Direction Polarity

The rotation direction signal must be applied between pin 4a and 4c. To add flexibility to the GS-D250M board the proper direction signal is combined with the position of an internal switch (SW5) according to the following table:

DIR SIGNAL	SW5	ROTATION
HIGH	ON	CCW
HIGH	OFF	CW
LOW	ON	CW
LOW	OFF	CCW

Phase Current Programming

The GS-D250M can be used to drive 4 wires motors or 8 wires motors. The phase peak current level can be programmed by a resistor according to the following formula:

$$Rx = \frac{3.2}{I_{pk}} - 1 \quad (k\Omega)$$

where I_{pk} is expressed in Amperes.
The factory setting is for a peak current of 1.6A.
The user can replace R_x (located close to the front edge of the board) by a new resistor according to the desired current level. The minimum value of R_x is 270Ω that corresponds to I_{pk} = 2.5A.

Phase Current Ripple Programming

The phase current control is performed by a chopping method with fixed off-time (about 32µs).
Therefore the chopping uses Frequency Modulation to keep the phase current at a desired level.
Being the off-time fixed, the amount of current decay i.e. of current ripple depends on the supply voltage, the back EMF, the L/R constant of the motor and on the method used for current recirculation (fast or slow, see the GS-D200M data sheet).

The GS-D250M board uses a mixed recirculation method:
fast recirculation for a time t_f, slow recirculation for the remaining period ($t_{off} - t_f$) of the off-time.
The time t_f and, therefore, the amount of phase current ripple can be adjusted by the proper setting of the potentiometer P1 provided on the front edge of the board.

Current ripple programming allows the optimization of the electromechanical characteristics of the system and the reduction of power dissipation inside the motor.

To further improve the performance of the GS-D250M board, the current ripple can be automatically reduced at rest.

The user can select this option by setting the switch SW6 in the ON position. When SW6 is OFF this feature is eliminated and normal operation restored.

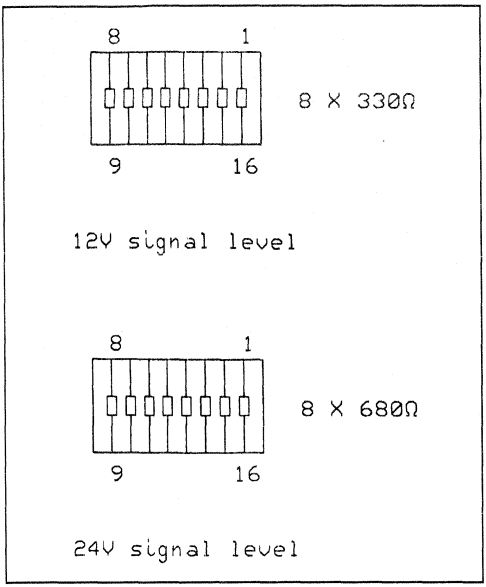
Input Commands

In the most straightforward application the GS-D250M board needs just three commands: step clock, direction, disable.
The module is disable when pin 6a is at high level.
To reduce the noise sensitivity, the three signals are applied to the board through internal optocouplers.
The pins 8a, 8c, 12c (optional commands for remote microsteps/step programming) are not galvanically isolated.
The signal level can have TTL compatibility (factory setted) or voltage levels of 12V or 24V, by changing the resistor array RR as shown in fig. 4.

Environmental Data

The GS-D250M board uses powerfet transistors in the two H-bridges that drive the motor windings.
This allows reduced conduction and switching power dissipation inside the GS-D200M.
Nevertheless, according to the application and to the ambient temperature, the GS-D200M case temperature can eventually increase to above 85°C. In such a case, cooling by forced ventilation is needed.

Figure 4. Input Signal Level Programming



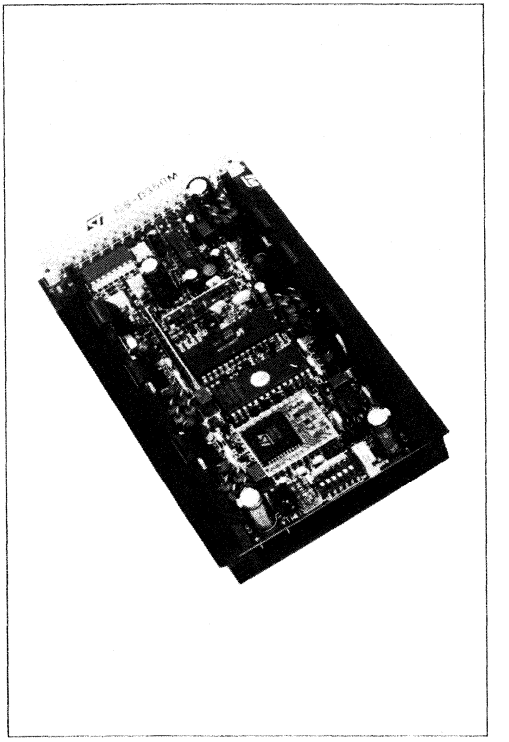
SGS-THOMSON MICROELECTRONICS

GS-D350M

5.6A MICROSTEP DRIVE BOARD FOR STEPPER MOTOR

FEATURES

- 5.6A/phase peak current
- 5, 10, 25, 45, 90, 100, 127 microsteps/step
- Full step operation
- User selectable phase current
- Automatic two quadrant chopping at rest
- Programmable phase current ripple
- 4/8 wires motors drive
- Galvanic isolation
- Full output protection against short circuits
- Thermal, under and overvoltage protection
- Step clock in excess of 140kHz
- Isolated Fault output



DESCRIPTION

The GS-D350M is a member of the SGS-THOMSON family of stepper motor drive modules and boards. It drives the 4/8 wires motor in a microstep mode thus assuring smooth and resonance free operations. On top of that it offers an unusually large number of features that allow a complete control of the electromechanical characteristics of the motion system to obtain optimum performance.
The powermos output stages offer both low conduction and commutation losses for increased efficiency: this, combined with an exclusive protection scheme, results in an extremely rugged unit suitable for harsh environment operation.
The GS-D350M single-Europe board is the simplest and most cost effective solution to any stepper motor drive requirements, thanks to the high number of embedded extra features.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
I_{ph}	Output Current per Bridge	3.3	Apk
I_{dis}	Supply Bus Discharge Current	4	A
I_i	Logic Input Current	30	mA
I_o	Logic Output Current	10	mA
V_{is}	Logic to Supply Isolation Voltage	500	V
T_{stg}	Storage Temperature Range	-20 to +85	°C
T_{hop}	Max Operating Heatsink Temperature*	+85	°C

* Thermal protection intervention @ Th > 90°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit
V_S	DC Supply Voltage		18		40	V
I_{ph}	Phase Current per Output*		0.5		2.8	A
I_i	Logic Input Current**			10		mA
V_o	Logic Output Voltage (TTL compatible)	Low High	2		0.8 5	V
fc	Clock pulse frequency				140	kHz

* Output shorts protection phase-to-phase, phase-to-supply and phase-to-ground.
** TTL, 12V, 24V Programmable input voltage level.

Note: The unit requires an input filtering capacitor 4700µF/50V, with low ESR and located as close as possible to the board.

Figure 1. Signals Timing

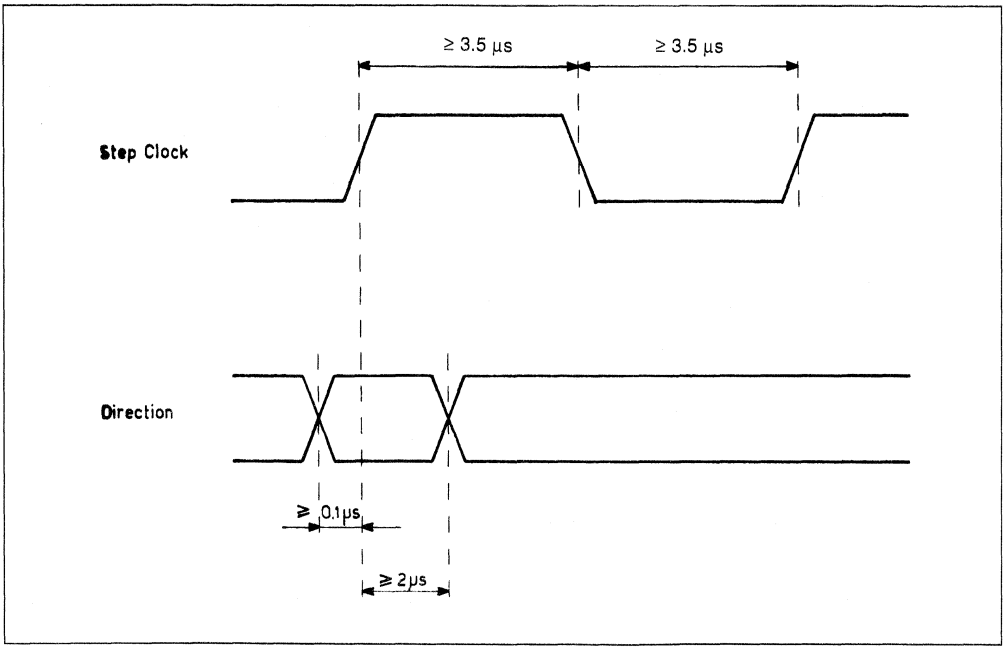
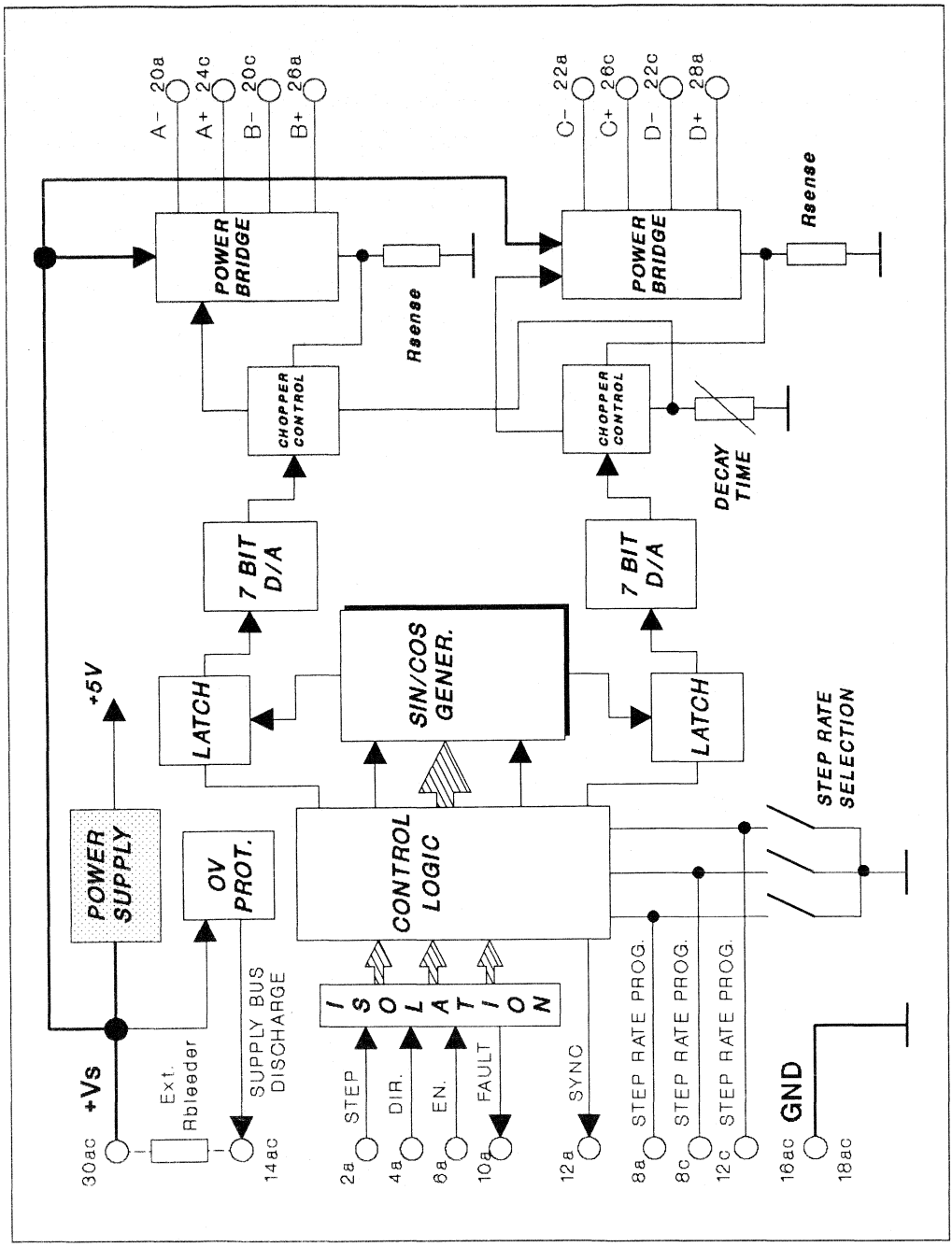
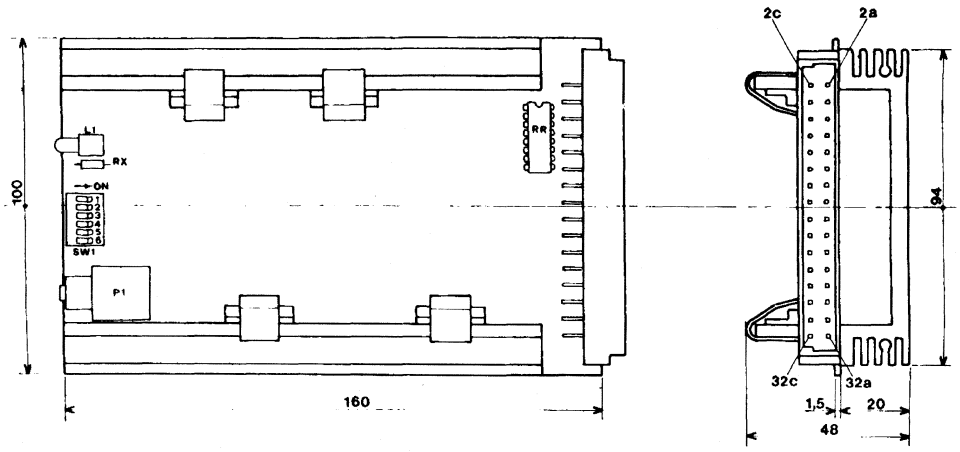


Figure 2. GS-D350M Block Diagram



CONNECTION DIAGRAM AND MECHANICAL DATA



Dimension in mm

GS-D350M Hardware available commands

SW1, SW2, SW3	Microsteps/step programming
SW4	Step clock transition selection
SW5	Direction polarity selection
SW6	Current ripple reduction at rest
R_X	Maximum peak current setting
P1	Phase current ripple programming
RR	Resistor array for logic level setting

GS-D350M BUS CONNECTOR PINS DESCRIPTION

The GS-D350M uses a 32 pins (16+16) DIN 41612-VG95324 male connector.

Pin	Function
2a	Step clock input: this is a logic input that performs the step function, i.e. on every transition of this input the motor is moved one step in the proper direction. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
2c	Return path for the Step clock input.
4a	Direction input; the logic state applied to this pin decides the rotation direction of the motor shaft. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
4c	Return path for the Direction input.
6a	Enable input; a logic high level applied to this input causes the power driver outputs to float. This condition allows the manual positioning of the system. Care must be used when this input is activated because the detention torque is lost. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
6c	Return path for the Enable input.
8a	Microsteps/step rate remote programming
8c	Microsteps/step rate remote programming
10a	Fault logic output. This isolated output is at a low logic level whenever an anomalous condition is detected. The output is open collector, i.e. a pull-up resistor is required.
10c	Fault output return path. Must be connected to the driven logic ground.
12a	Synchronization signal for Microsteps/step logic programming.
12c	Microsteps/step rate remote programming.
14a-c	Supply bus discharge output; this output is activated when an overvoltage condition is detected. A resistive load connected between this pin and the supply bus can be used to sink power to limit the maximum supply voltage to safe conditions.
16a-c	Power supply ground
18a-c	Power supply ground
20a	Phase A– output.
20c	Phase B– output.
22a	Phase C– output.
22c	Phase D– output.
24c	Phase A+ output.
26a	Phase B+ output.
26c	Phase C+ output.
28a	Phase D+ output.
30a-c	Module supply voltage; hazardous voltages may be present on these pins.

GS-D350M DESCRIPTION

The GS-D350M is a complete subsystem to drive stepper motors either in full step or microstep mode. A very large number of auxiliary functions has been included to allow extreme simplicity and flexibility in use.

Particular care has been devoted to protections, so that the GS-D350M can be safely used in very harsh environments. In addition to the obvious function to drive the motor phases in a chopping mode, the following functions have been implemented:

- Sine/cosine generation
- Selection of seven different microsteps/step rates
- Selection of full step drive
- Programming of peak phase current to optimize the torque
- Automatic phase current ripple reduction at rest
- Full protection against short circuits between phase-to-phase, phase-to-ground and phase-to-supply
- Thermal, undervoltage, overvoltage protection
- Galvanic isolation of input signals and of fault indication output
- On board auxiliary voltages generation.

As a result, the GS-D350M can provide up to 5.6A per phase and, in its simplest application, just three command signals are required: step clock, direction, enable.

SUPPLY VOLTAGE

A single, unregulated supply voltage is requested to operate the board.

THE POWER SUPPLY MUST BE TURNED OFF WHEN PLUGGING OR UNPLUGGING THE BOARD.

The supply pins are: 30a, 30c positive rail
16a, 16c, 18a, 18c ground rail.

The other supply voltages needed by the board are internally generated by a high efficiency step-down switch mode regulator that provides also the subsystem reset at power on. The supply voltage range is between 18V and 42V: it is recommended to operate the board at a maximum voltage of 40V. If an undervoltage condition is detected (Vs < 18V) the GS-D350M is automtically disabled and an LED is activated.

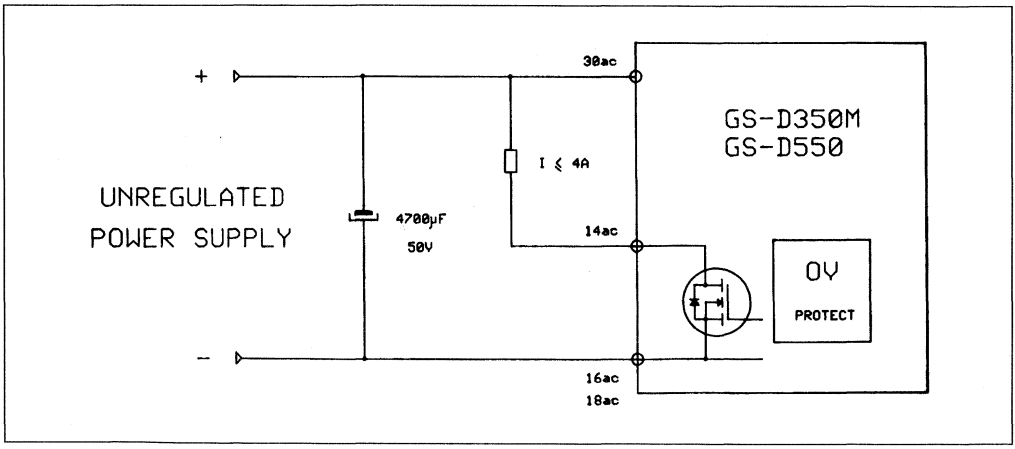
If a voltage above 42V is applied to the board, the following features are activated:

- An LED is turned on.
- An automatic overvoltage active clamping is turned on.

The active clamping system is implemented as shown in fig. 3.
The active overvoltage clamping is mainly intended to clamp transient overvoltages.

In case of permanent overvoltage, excessive power dissipation can occur. Therefore, if the supply voltage is derived from a rectified and filtered secondary winding of a main transformer, this voltage at no load and at maximum main AC voltage must be lower than 42V (50/60 Hz ripple included). Overvoltages may occur during fast deceleration because of transient spikes on the AC main supply during very fast deceleration cycles and when the output bridges are in the fast decay recirculation mode.

Figure 3. Active Overvoltage Clamping



During this mode, the phase current pulses are returned to the supply voltage: if the supply voltage impedance is not adequately low, the current pulse can raise the voltage well above the nominal level.

To avoid that the overvoltage clamping is activated at a chopping mode switching frequency, a 4700µF/50V capacitor must be connected as close as possible to the supply pins.
The ESR of the capacitor at the switching frequency (about 20÷30 kHz) must be very low.

The power rating of the external bleeder resistor can range from 10 to 50W depending on AC main supply condition (overvoltage transients frequency). The resistor must be of a low inductance type to allow fast discharge of the bus voltage.

This value varies according to the operating conditions, but in first approximation it can be calculated according to the following formula:

$$R_{bleeder} \geq \frac{V_S}{4} [\Omega]$$

This is the minimum usable value.

MICROSTEP PROGRAMMING

The number of microsteps per step is field programmable. The digitized sine and cosine functions, required by a microstepping control, are stored in a Lock-Up-Table inside the GS-D350M.

Two options are provided for the proper microsteps/step rate selection.

Microstep Programming by Hardware

Three switches (SW1, SW2, SW3) are available on the front edge of the board.

The microsteps/step rate is defined by the following table.

SW1	SW2	SW3	MICROSTEPS/STEP
OFF	OFF	OFF	127
ON	OFF	OFF	100
OFF	ON	OFF	90
ON	ON	OFF	45
OFF	OFF	ON	25
ON	OFF	ON	10
OFF	ON	ON	5
ON	ON	ON	1

The switches are in OFF condition when the knob is pulled versus the board edge. The last condition (ON, ON, ON) defines a full step operation.

Microstep Programming by Host Computer

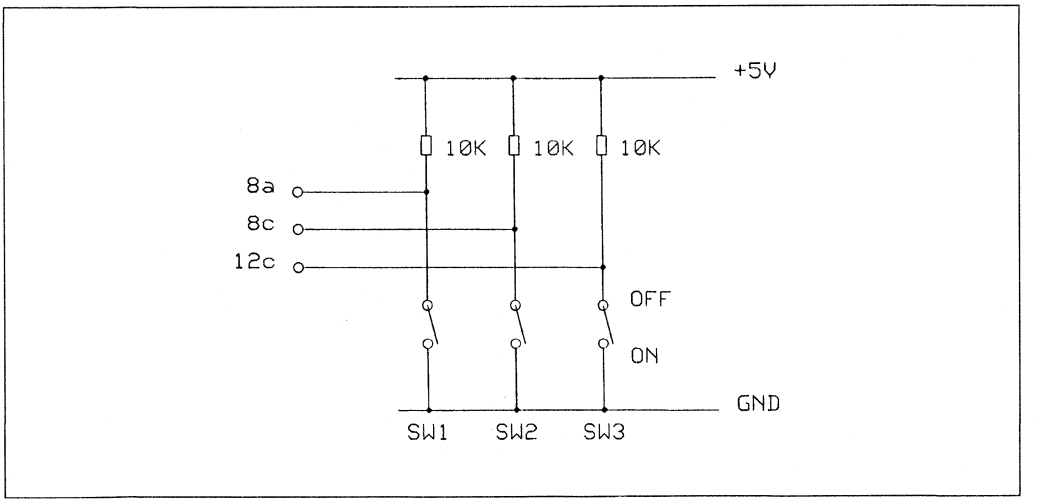
The microsteps/step rate can also be changed on-the-fly by using the three logic inputs available on the bus connector (8a, 8c, 12c) that correspond, respectively, to SW1, SW2, SW3.

This mode of operation may be requested during the motor operation to obtain, as an example, smooth start up and maximum top speed to reduce the time-to-move.

The interaction between logic signals and hardware switches is shown in fig. 4.

To operate the logic pins of the bus, the three internal switches must be in the OFF state (state 1).

Figure 4. Remote Microstepping Programming



The remote programming of the microsteps/step rate cannot be implemented asynchronously: it must be made only when the phase currents are at 45 and 135 electrical degrees.

This state is signaled by the SYNC pin (12a) and it must be read by the host computer after 3µs from the active edge of the step clock. The correct sequence for on-the-fly change of the microsteps/step is as follows:

- read the active edge of the step clock after a delay of 3 µs;
- read the status level of the SYNC pin (high or low) after this delay;
- if the status level has changed after the 3 µs, program the new microsteps/step rate;
- complete the programming before the arrival of the next active edge of the step clock signal;

The three microstep programming pins (8a, 8c, 12c) as well as the SYNC pin (12a) are not galvanically isolated. Their level is TTL compatible only.

SETTING OF THE ACTIVE EDGE OF THE STEP CLOCK

The step clock active edge (i.e. the edge that advances the motor by one step) can be the rising or the falling edge depending on the position of the switch SW4.
The following table allows the proper setting:

SW4	ACTIVE TRANSITION
ON	Low-to-high
OFF	High-to-low

SETTING OF THE DIRECTION POLARITY

The rotation direction signal must be applied between pin 4a and 4c.

The direction (CW or CCW) depends on the status of the direction signal and of the position of the switch SW5 as shown in the following table:

DIR SIGNAL	SW5	ROTATION
HIGH	ON	CCW
HIGH	OFF	CW
LOW	ON	CW
LOW	OFF	CCW

PHASE CURRENT PROGRAMMING

The GS-D350M can be used to drive both four-wires and eight-wires motors.

Particular care must be paid to connect the wires with the correct polarity.

The GS-D350M uses four powerfet H-bridges (PHA, PHB, PHC, PHD outputs respectively)

PHA and PHB are energized in parallel as well PHC and PHD.

The possible connections of a motor are shown in fig. 5 and fig. 6.

In case of a four-wires motor, PHA and PHC only must be used.

Each H-bridge can deliver up to 2.8 Apk that is also the maximum current for a winding.

Therefore a four-wires motor can have a maximum phase current of 2.8 A.

Figure 5. Four Wires Motor Connection

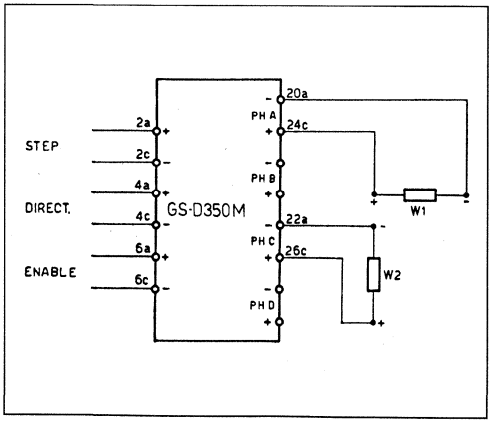
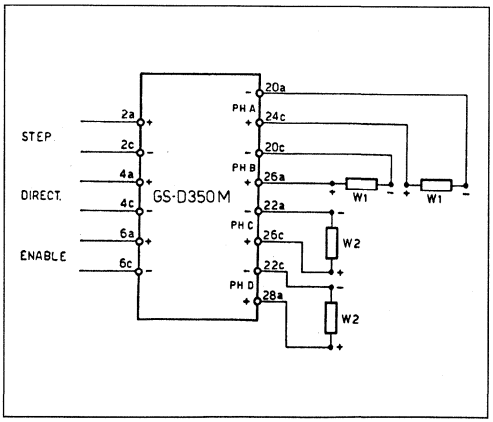


Figure 6. Eight Wires Motor Connection



In the case of an eight-wires motor the maximum phase current is 2 x 2.8 = 5.6 Apk.

The output peak current level can be programmed by a single resistor Rx that acts on all the four H-bridges.

The value of Rx for a given I_{pk} is

$$R_X = [\frac{3.2}{I_{pk}} - 1] \, k\Omega$$

The maximum value of I_{pk} is 2.8 Apk and the minimum value of Rx is 143 Ω.

The factory setting is for 1.6 Apk current for each output.

The user can modify the peak current by a proper substitution of Rx.

PHASE CURRENT RIPPLE PROGRAMMING

The phase current level control is performed by a chopping method with fixed off-time (about 32 µs) i.e. by Frequency Modulation technique.
By definition, a chopping control imposes a certain ripple on the average current. Being the off-time fixed, the amount of the current decay during the off-time, i.e. the current ripple, depends on many variables such as:

- Supply voltage
- Motor winding inductance L and resistance R
- Maximum step rate
- Microsteps/step rate.

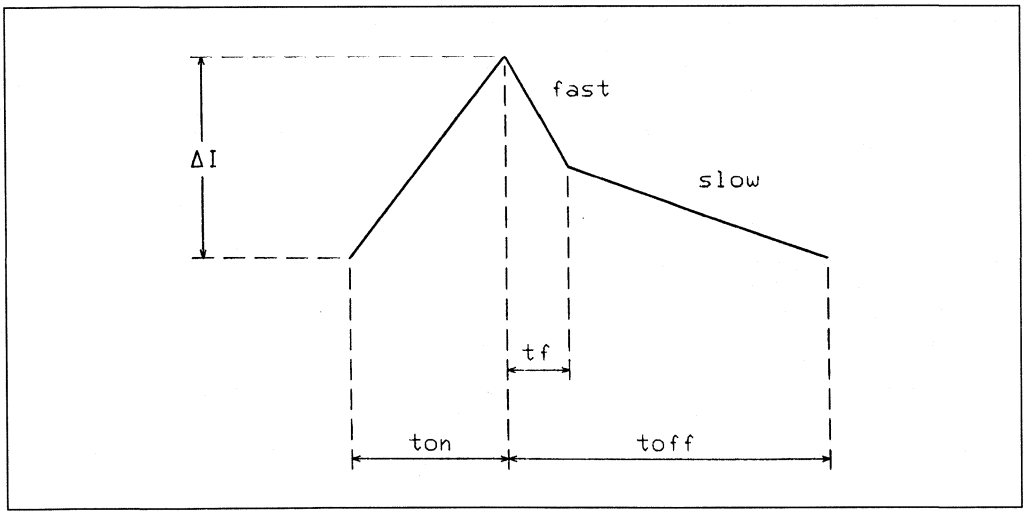
It depends also on the method used to recirculate the phase curent during the off-time (slow decay i.e. two quadrants operation or fast decay i.e. four quadrants operation).

The amplitude of the phase current ripple is a very important parameter for every microstepping drive mode because it contributes to the electromechanical performance of the system.

A low current ripple offers noiseless operation and reduced power dissipation in the motor.

The GS-D350M uses a mixed recirculating method: fast and slow decay as shown qualitatively in fig. 7.

Figure 7. Mixed Decay Method



During the time t_f, a fast decay (four quadrants operation) is imposed. The off-time is then completed in a slow decay (two quadrants operation). The current ripple is, therefore, a function of t_f too. The fast decay time t_f can be continuously adjusted by acting on potentiometer P1 (R36) provided on the front edge of the board.

The proper setting of P1 (R36) can be made by monitoring the phase current under the worst case operation and by adjusting P1 (R36) until a sinusoidal current waveform is reached.

When the motor is at rest, no back EMF is generated and the current ripple might increase. To prevent this phenomenon, the automatic ripple reduction feature at rest has been implemented in the GS-D350M.

By putting the switch SW6 in the ON position, the phase current recirculates in a slow decay for all the off-time ($t_f = 0$), so giving the minimum possible ripple current determined, only, by the supply voltage and the L/R constant of the motor.

The user could eventually reduce the external supply voltage at rest to further reduce the current ripple. If the SW6 is in the OFF position there is no ripple reduction at rest.

INPUT COMMANDS

In its most straightforward application, the GS-D350M requires just three input commands as shown in fig. 5 (STEP CLOCK, DIRECTION, ENABLE).

The module is disabled when pin 6a is at high logic level versus pin 6c.

These three signals are galvanically isolated by internal optocouplers. (Isolation voltage: 500V).

The level of the input signal is field programmable. The factory setting is for TTL signals.

In case the signals level is 12V or 24V, a DIL resistor array must be changed as shown in fig. 8.

THERMAL PROTECTION

The GS-D350M board has an integral heatsink that allows continuous operation up to 50°C ambient temperature if the phase current is limited to 4 Apk.

At higher ambient temperature and/or higher phase current levels additional cooling must be provided by forced ventilation or by additional heatsink.

The maximum allowable winding current for an eight-wires motor versus the ambient temperature is shown in fig. 9 while fig. 10 shows maximum current level at rest.

To protect the system against unforeseen odd events, a thermal protection is activated whenever the heatsink temperature reaches about 90°C. The thermal protection disables the module and the condition is signaled by the FAULT signal.

OUTPUT OVERLOAD AND SHORT CIRCUIT PROTECTION

To prevent permanent damage to the GS-D350M, three protections have been implemented against overload and short circuits between:

- output to supply voltage
- output to output
- output to ground.

When one of these adverse conditions occurs, the drive of the output H-bridges in disabled and the condition is signaled by the FAULT signal.

FAULT SIGNAL

The FAULT signal is available at pin 10a and 10c. When a fault is present, pin 10a goes low versus pin 10c.

This output is a galvanically isolated TTL signal. Whenever the FAULT signal is activated, the LED provided in the front edge of the module is switched ON.

Figure 8. Input Signal Level Programming

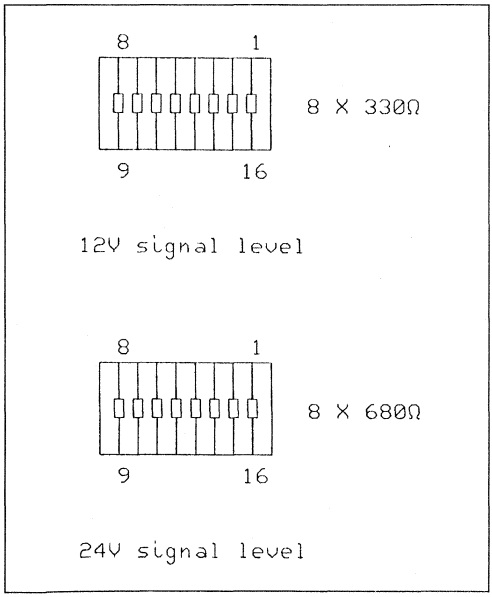


Figure 9. Thermal behaviour when stepped

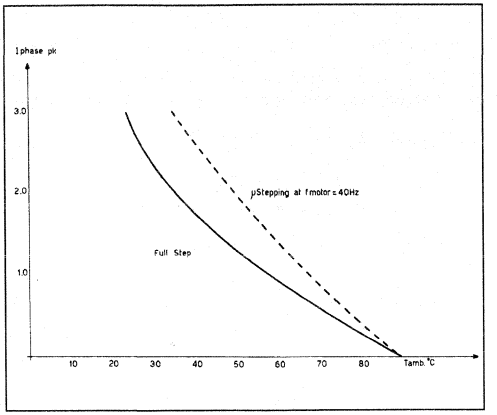
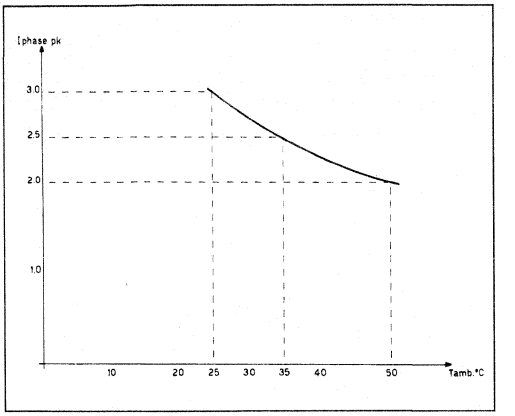


Figure 10. Thermal behaviour at rest

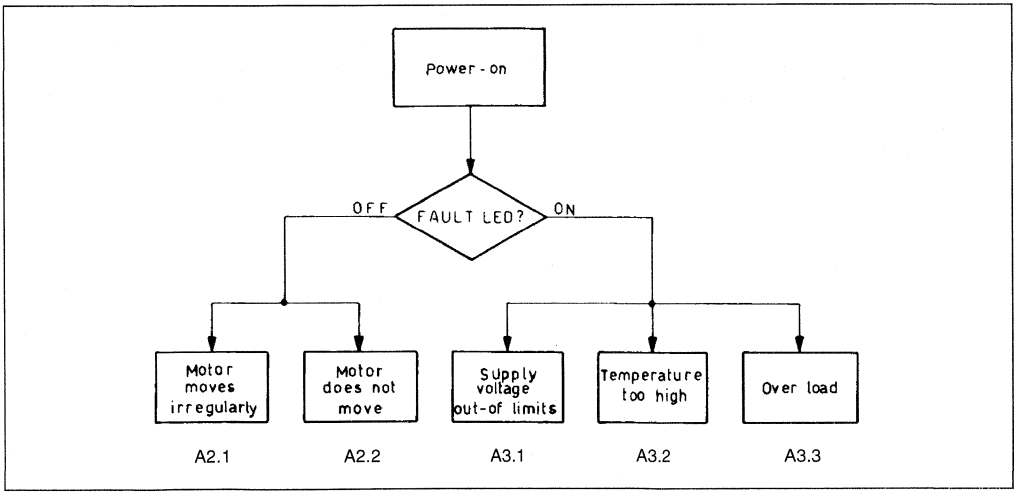


The FAULT signal is active (low) when:

- the supply voltage is lower than 18V
- the supply voltage is higher than 42V
- the heatsink temperature is higher than 90°C
- an output overload is present.

A - TROUBLE SHOOTING

A1 - Troubleshooting Sequence



A2 - FAULT SIGNAL INACTIVE

A2.1 - The motor moves irregularly if:

a) there is an error in the motor connection;

b) the step rate is close to the resonance frequency or too high;

c) the load plus friction torque is close to motor torque;

d) the motor is defective.

The corrective actions are:

a) check and correct the motor connections;

b) change the step rate;

c) increase the phase current or decrease the step rate;

d) substitute the motor.

A2.2 - The motor doesn't move if:

a) there is an error in the motor connection;

b) the Step-clock signal is not present, wrongly connected or badly timed;

c) the load plus friction torque is too high;

d) the motor is defective.

The corrective actions are:

a) check and correct the motor connections;

b) verify the step-clock connection and the timing;

c) increase the phase current or use a larger motor;

d) substitute the motor.

A3 - FAULT SIGNAL ACTIVE

The fault output is active when:

a) the supply voltage is lower than 18V;

b) the supply voltage is higher than 42V;

c) the heatsink temperature is higher than 90°C;

d) there is an output overload condition.

A3.1 - An anomalous supply voltage condition occurs if:

a) the power supply is incorrectly set or a power supply fault has occurred;

b) the motor is used as a generator;

c) very fast deceleration is used.

The corrective actions are:

a) check and correct the power supply setting;

b) use the bus discharge circuit and limit the motor speed to safe values;

c) use the bus discharge circuit and longer deceleration times.

A3.2 - The heatsink temperature is higher than 90°C if:

a) the ambient temperature (around the board) is too high.

The corrective actions are:

a) provide an adequate heatsink, space and ventilation to the board.

A3.3 - An output overload condition is detected if:

a) an accidental short circuit phase-to-phase, phase-to-ground or phase-to-supply has occurred;

b) the motor has an internal short circuit.

The corrective actions are:

a) check the integrity of the connections between the board and the motor;

b) substitute the motor.

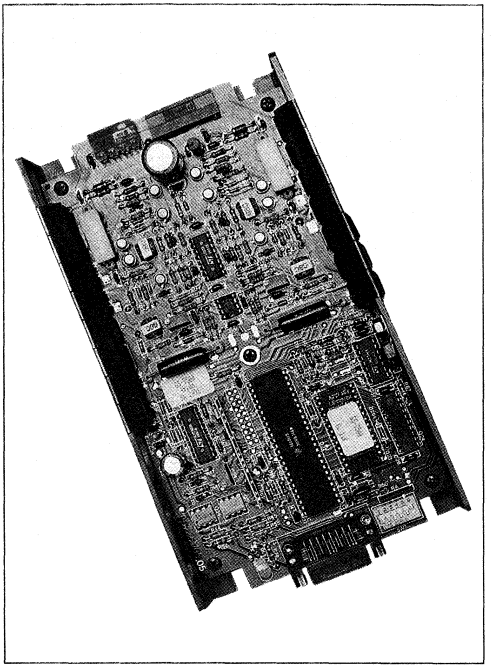
SGS-THOMSON MICROELECTRONICS

GS-D500

70V/5A STEP AND MICROSTEP DRIVE BOARD FOR STEPPER MOTORS

FEATURES

- 5A/phase peak current
- 5, 25, 125 microsteps/step
- Full step and half step operation
- User selectable phase current
- 90° out of phase chopping to save power consumption
- Galvanic isolation
- Full output protection against short-circuits
- Thermal and undervoltage protection
- Step clock in excess of 200kHz
- Fault indication output
- Special circuit to reduce midrange instability



DESCRIPTION

The **GS-D500** is a member of the SGS-THOMSON family of stepper motor driver modules and boards. It drives motors in full step, half step and microstep mode.

On top of that it offers an unusually large number of features that allow a complete control of the electromechanical characteristics of the motion system to obtain optimum performance.

The powermos output stages offer both low conduction and commutation losses for increased efficiency; this, combined with a complete protection scheme, results in an extremely rugged unit suitable for harsh environment operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Motor Supply Voltage	75	V
V_{SS}	DC Logic Supply Voltage	13	V
I_{ph}	Output current per Bridge	6	Apk
I_i	Logic Input Current	30	mA
V_{is}	Isolation Voltage	500	V
T_{stg}	Storage Temperature Range	–20 to +85	°C
T_{hop}	Operating Heatsink Temperature *	+85	°C

* Thermal protection intervention @ Th > 90°C

ABSOLUTE MAXIMUM RATINGS ARE LIMIT VALUES ABOVE WICH THE UNIT CAN BE PERMANENTLY DAMAGED

ELECTRICAL CHARACTERISTICS ($T_{amb.}$ = 25°C and V_S = 24V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	DC Motor Supply Voltage		12		70	V
V_{SS}	DC Logic supply Voltage		11.5	12	12.5	V
I_{ph}	Phase Current per Output *		0.5		5	A
I_i	Logic Input Current			10		mA
V_{SI}	On board Logic Supply Output		4.75	5	5.25	V
I_{OSI}	On board Logic Supply Current Output				100	mA
fc	Clock Pulse Frequency				200	kHz

* Output shorts protection phase-to-phase, phase-to-ground.

Note: the unit requires an input filtering capacitor in the range of 4700F to 10,000/100V, with low ESR and located as close as possible to the board.

Fig. 1 - Signals timing

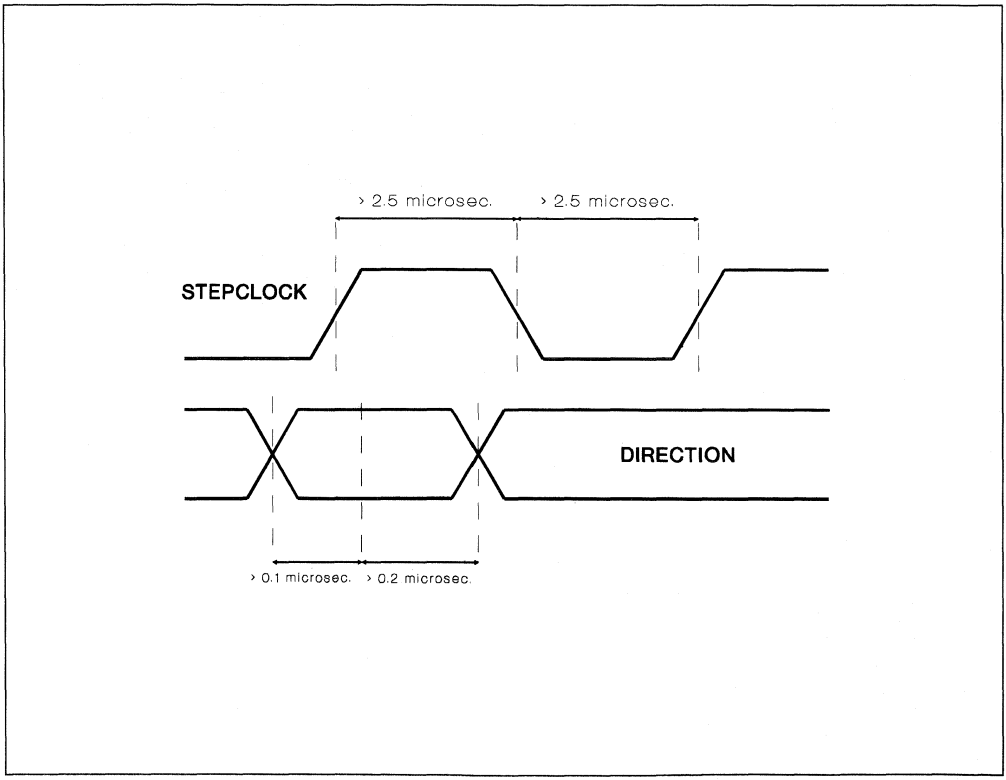
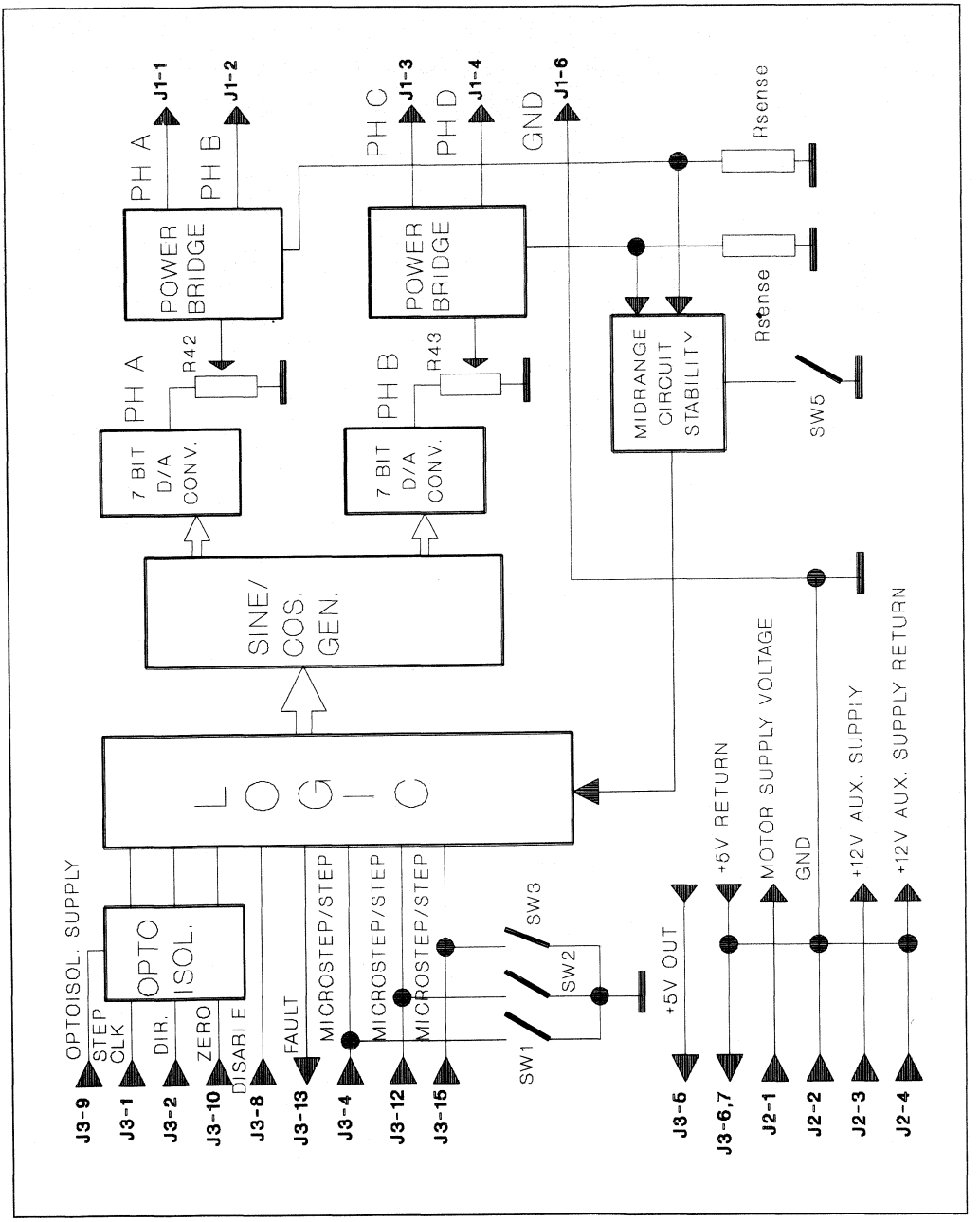
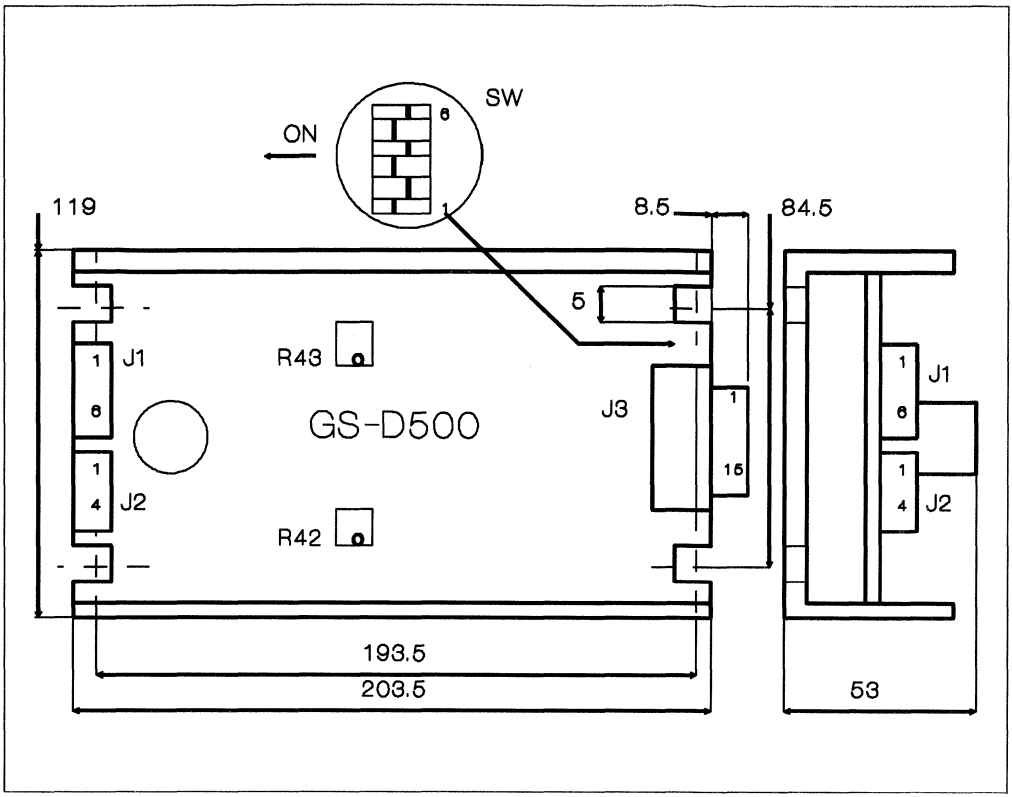


Fig. 2 - Block diagram



MECHANICAL DATA (dimension are in millimeters)



GS-D500 HARDWARE AVAILABLE COMMANDS

SW1, SW2, SW3	Microsteps/step programming
SW4	Phase peak current selection
SW5	Midrange stabilization ON/OFF
SW6	Current reduction at rest
R42	Phase **A** current programming
R43	Phase **B** current programming

GS-D500 CONNECTORS PINS DESCRIPTION.

CONNECTOR J1

J1-1	Phase **A** output
J1-2	Phase **B** output
J1-3	Phase **C** output
J1-4	Phase **D** output
J1-6	Ground

CONNECTOR J2

J2-1	Motor Supply Voltage
J2-3	Auxiliary Supply voltage (+12V)
J2-2,4	Ground

CONNECTOR J3

Pin	**Function**
J3-1	Step clock isolated input (see fig.3): this is a logic input that performs the step function
J3-2	Direction isolated input (see fig.4): the logic state applied to this pin decides the rotation direction of the motor shaft.
J3-4	Microsteps/step rate remote programming (SW1).
J3-5	On board +5V output
J3-6,7	Return path for on board +5V output
J3-8	Disable input (see fig.6): a logic high level applied to this input causes the power driver outputs to float. This condition allows the manual positioning of the system. are must be used when this input is activated because the detention torque is lost.
J3-9	Optocoupler supply voltage.
J3-10	Zero current control isolated input (see fig.5): when activated the phase current is reduced to zero.
J3-12	Microsteps/step rate remote programming (SW2).
J3-13	Fault logic output (see fig.9): this output is at a low logic level whenever an anomalous condition is detected.
J3-15	Microsteps/step rate remote programming (SW3).

Figure 3. Stepclock input circuit

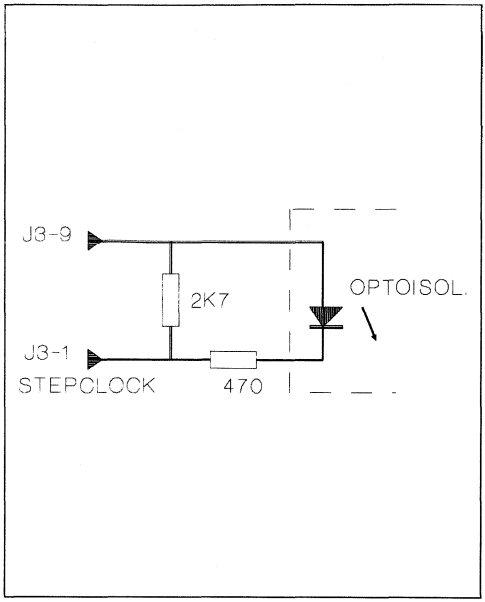


Figure 4. Direction input circuit

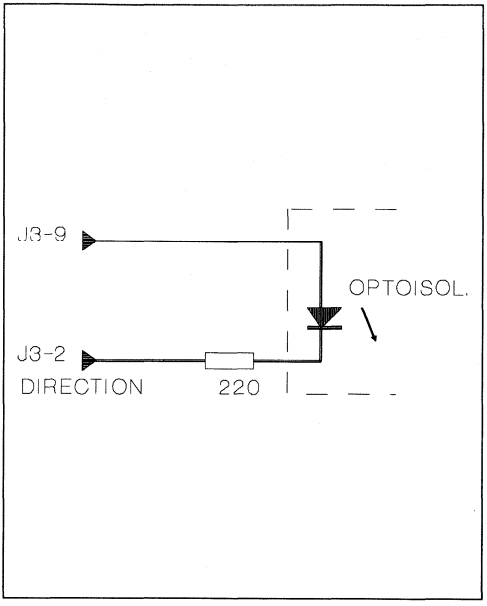


Figure 5. Zero current input circuit

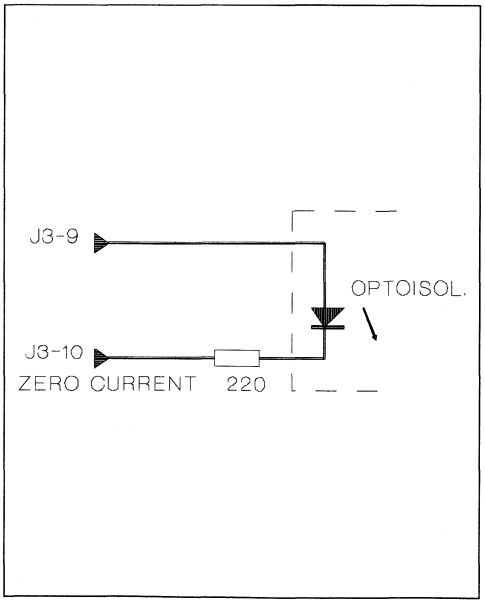
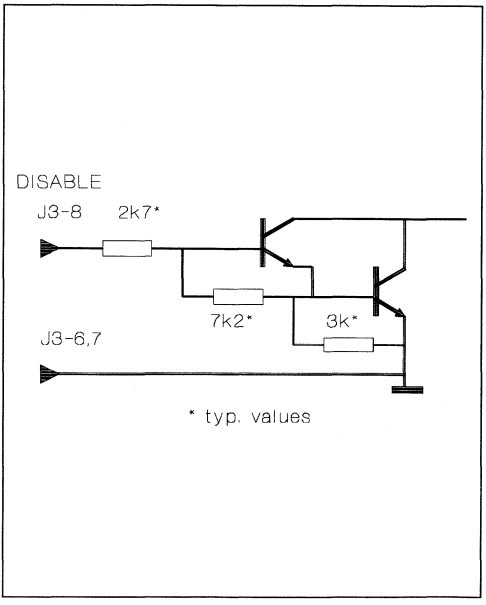


Figure 6. Disable input circuit



GS-D500 DESCRIPTION

The **GS-D500** is a complete subsystem to drive stepper motors either in full step or microstep mode.

A very large number of auxiliary functions has been included to allow extreme simplicity and flexibility in use.

Particular care has been devoted to protections, so that the GS-D500 can be safely used in very harsh environments.

In addition to the obvious function to drive the motor phases in a chopping mode, the following functions have been implemented:

-Sine/cosine generation

-Selection of three different microsteps/step rates

-Selection of full/half step drive

-Programming of peak phase current to optimize the torque

-Automatic phase current reduction at rest (selectable)

-Full protection against short-circuits between phase-to-phase and phase-to-ground

-Thermal and undervoltage protection

-Galvanic isolation of 3 input signals (**clock, direction, zero current**).

-Fault indication output

-On board auxiliary voltages generation.

-Midrange stability circuitry (selectable)

As a result, the **GS-D500** can provide up to 5A per phase and, in its simplest application, just three command signals are required: **step clock, direction, disable**.

Supply Voltage

THE POWER SUPPLY MUST BE TURNED OFF WHEN PLUGGING OR UNPLUGGING THE BOARD

The supply pins are:

J2-1 for Motor Supply Voltage

J2-3 for Auxiliary Voltage

J2-2,4 for Ground rail

The other supply voltages needed by the boards are internally generated.

If an undervoltage condition is detected (Vs < 10V) the **GS-D500** is automatically disabled and an led is activated.

The Motor Supply voltage is in the range from 12 to 70V, the Auxiliary voltage from 11 to 13V.

At power-on the Auxiliary Supply voltage must be applied before the Motor Supply voltage, while at power-off the Motor Supply voltage must be removed before the Auxiliary voltage.

Full-Step/Half-Step/Microstep Programming by Hardware

The number of microsteps per step is field programmable. The digitized sine and cosine functions, required by a microstepping control, are stored in a Lock-Up-Table inside the GS-D500.

Two options are provided for the proper microsteps/step rate selection.

Three switches (SW1, SW2, SW3) are available on the front edge of the board.

The full-step/half-step/microstep mode is defined by the following table.

SW1	SW2	SW3	MODE
OFF	ON	OFF	Half step
ON	ON	OFF	125 microsteps/step
ON	OFF	ON	25 microsteps/step
OFF	ON	ON	5 microsteps/step
ON	ON	ON	Full step

The switches are in OFF condition when the knob is pulled versus the board edge.

Invalid combinations disable the board.

Microstep Programming by Host Computer

The microsteps/step rate can also be remotely changed by using the three logic inputs available on the J3 connector (pins 4,12 and 15) that correspond, respectively, to SW1, SW2, SW3.

The interaction between logic signals and hardware switches is shown in fig. 7.

To operate the logic pins of the J3 connector, the three internal switches must be in the OFF state.

Current Reduction at Rest

Phase current can be reduced when the motor is stopped if SW6 is open.

Current reduction is operative about 1 second after the last clock pulse.

Setting of the Direction Polarity

The rotation direction signal must be applied at pin J3-3.

The direction (CW or CCW) depends on the status of the direction signal as shown in the following table:

DIR. SIGNAL	ROTATION
HIGH	CCW
LOW	CW

Phase Current Programming

The phase current can be programmed by means two on-board trimmer called **R42** and **R43** (see machanical drawing).

R42 programs the current in phase **AB**, while **R43** programs the current in phase **CD**.

A6 - MIDRANGE STABILITY

A particular circuitry is implemented on the board to avoid midrange oscillations.

This circuit is inserted on the current control loop when SW5 is OFF.

Current Selection in Microstep/Costant Current Switching (SW4)

When the board is used to drive a motor in microstep mode, an automatic switching from sinusoidal/cosinusoidal current to costant current is performed when the sinusoidal output waveform exceeds 500Hz. The costant output current can be choosen to be 0.707 of the peak current or the peak current: this possibility is given by SW4.
See fig.8).

SW4 OFF	0.707 * Ipeak
SW4 ON	Ipeak

An histeresys is inserted on the 500Hz threshold to avoid unwanted oscillations.

Fig. 7 - Remote microstepping programming

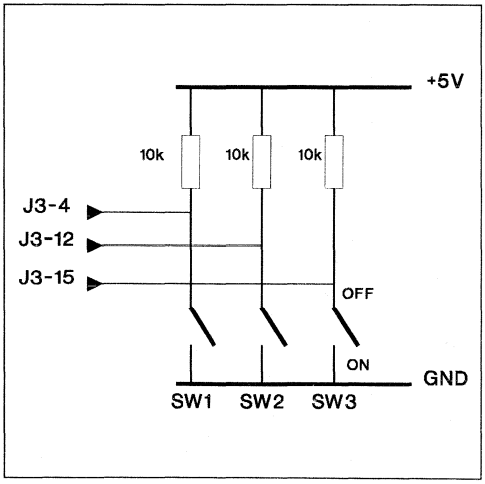
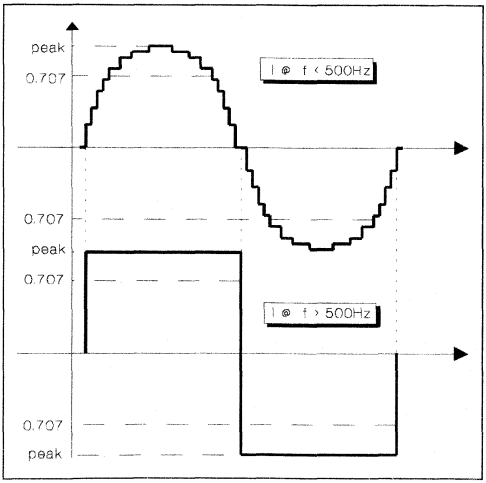


Fig. 8 - Current selection by SW4



Output Overload and Short Circuit Protection

To prevent permanent damage to the GS-D500. three protections have been implemented against overload and short circuits between:

- output to output
- output to ground.

When one of these adverse conditions occurs. the driver of the output H-bridges is disabled for about 500ms and the condition is signaled by the FAULT signal.

Fault Signal

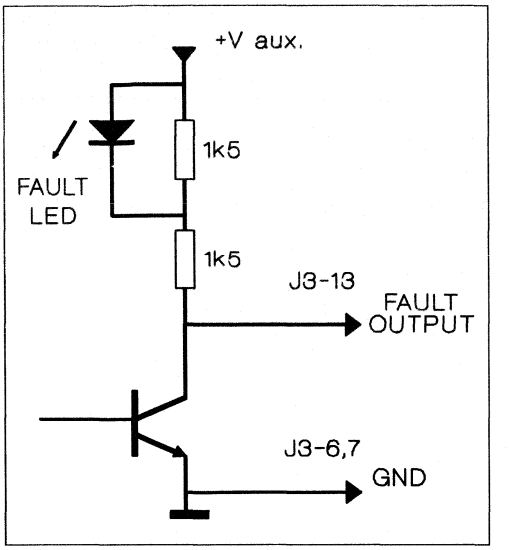
The FAULT signal is available at pin J3-13. When a fault is present, pin 13 goes low versus pins 6,7.

Whenever the FAULT signal is activated. the led provided in the front edge of the module is switched ON.

The FAULT signal is active (low) when:

- the supply voltage is lower than 12V
- the heatsink temperature is higher than 90°C
- an output overload is present
- a disable is active.

Fig. 9 - FAULT signal output circuit



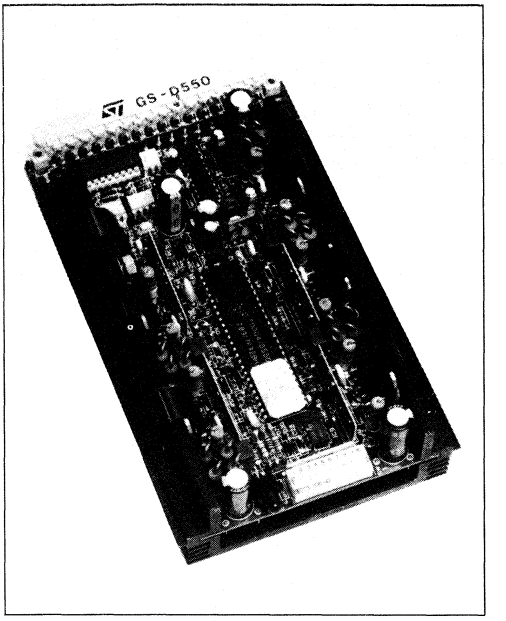
SGS-THOMSON MICROELECTRONICS

GS-D550

2/5 PHASE STEPPING MOTOR DRIVE BOARD

FEATURES

- Two and five phase motor drive
- Half and full step operation
- User programmable phase current during acceleration, slewing, rest
- Two/four quadrant current chopping
- Programmable phase current ripple
- Step clock frequency up to 100 kHz
- Galvanic isolation of input/output signals
- Thermal, undervoltage, overvoltage protection
- Single unregulated supply voltage
- On-board auxiliary voltages generation



DESCRIPTION

The GS-D550 is a board designed to drive stepper motors with 2 or 5 phases and with a current per phase up to 2.8A.
A very large number of auxiliary functions have been designed in, so that the interface to the microprocessor or host computer is reduced to a minimum.
The five output stages use powerfet H-bridges to ensure low conduction and switching losses; full protection against short circuits results in an extremely rugged unit suitable for harsh environment operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
I_{ph}	Continuous Phase Current per Output	2.8	Apk
I_{dis}	Supply Bus Discharge Current	4	A
I_i	Logic Input Current	30	mA
I_o	Logic Output Current	10	mA
V_{is}	Logic to Supply Isolation Voltage	500	V
T_{stg}	Storage Temperature Range	–20 to +85	°C
T_{hop}	Operating Heatsink Temperature Range*	+85	°C

* Thermal protection intervention @ Th> 90°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_S	DC Supply Voltage	18		40	V
Iph	Phase Current per Output* (5 phase)	0.5		2.8	A
Iph	Phase Current per Output* (2 phase, eight wires)	1.0		5.6	A
I_i	Logic Input Current**		10		mA
V_O	Logic Output Voltage (TTL compatible) Low High	2		0.8 5	V
fc	Clock Pulse Frequency			100	kHz
fs	Chopping Frequency		20		kHz

Note: The unit requires an input filtering capacitor 4700µF/50V, with low ESR and located as close as possible to the board.

* Output shorts protection phase-to-phase, phase-to-supply and phase-to-ground.

** TTL, 12V, 24V Programmable input voltage level.

Figure 1. Signals Timing

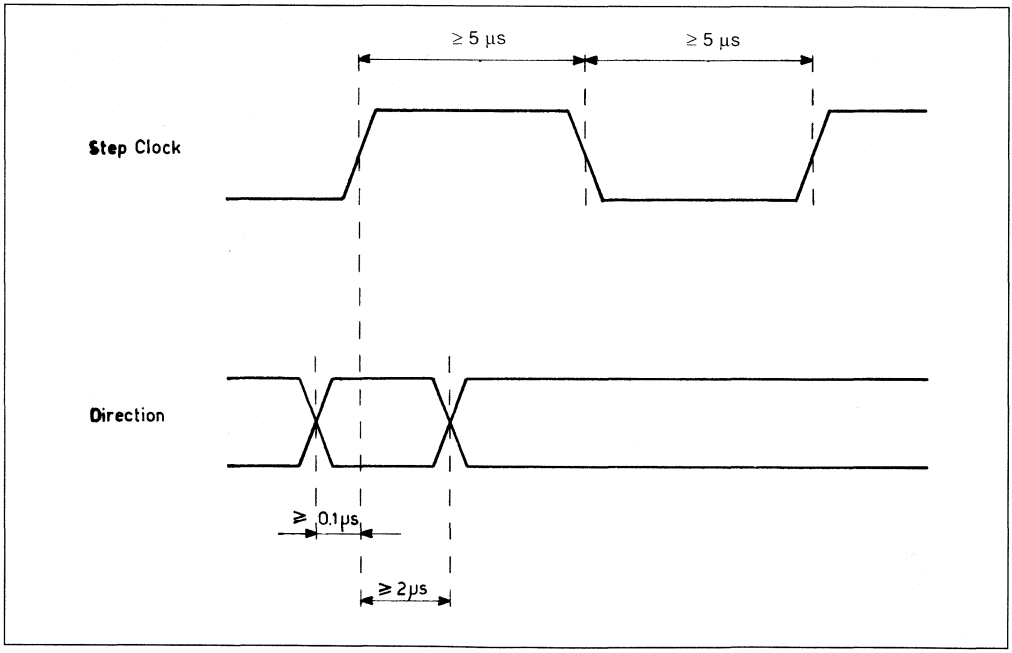
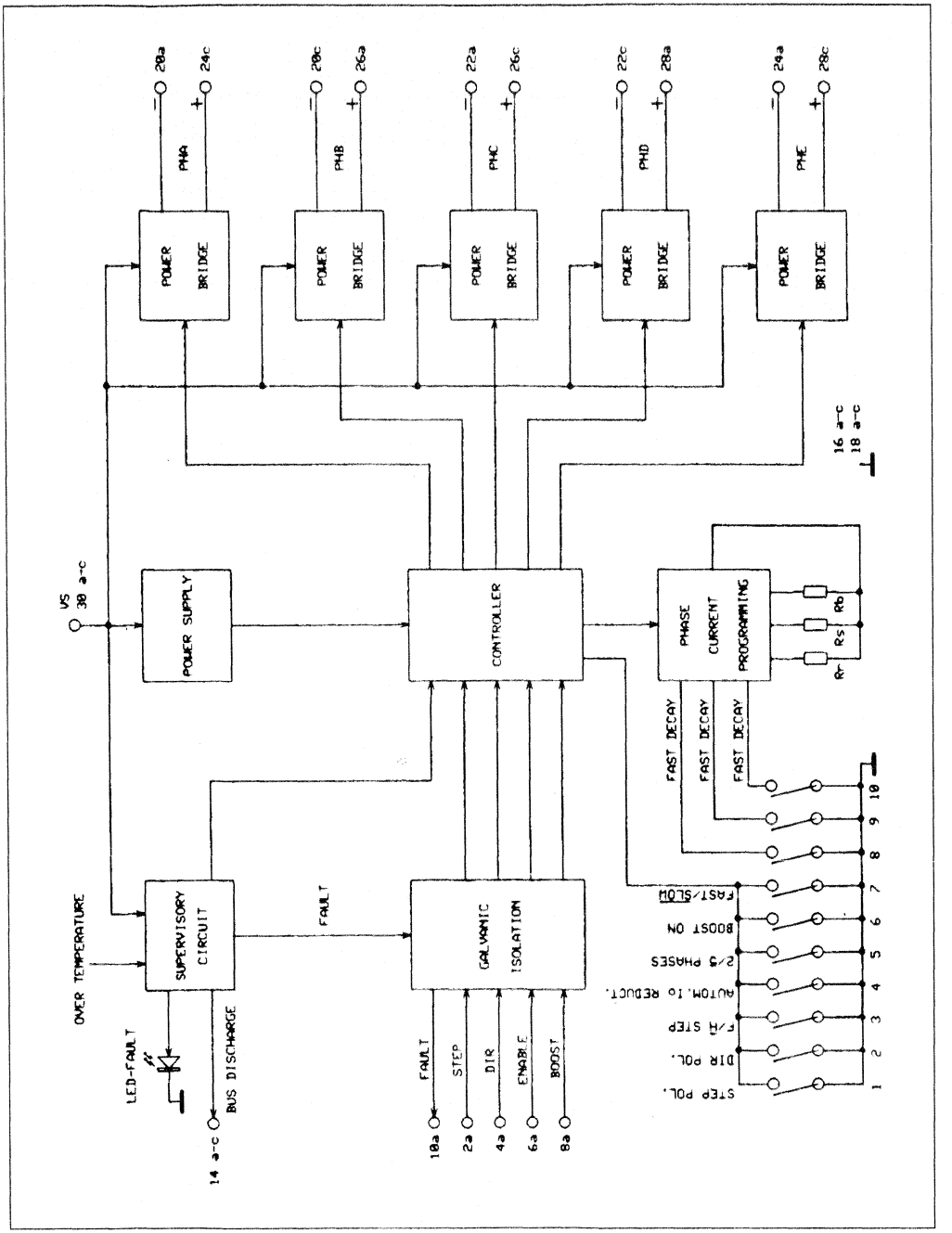
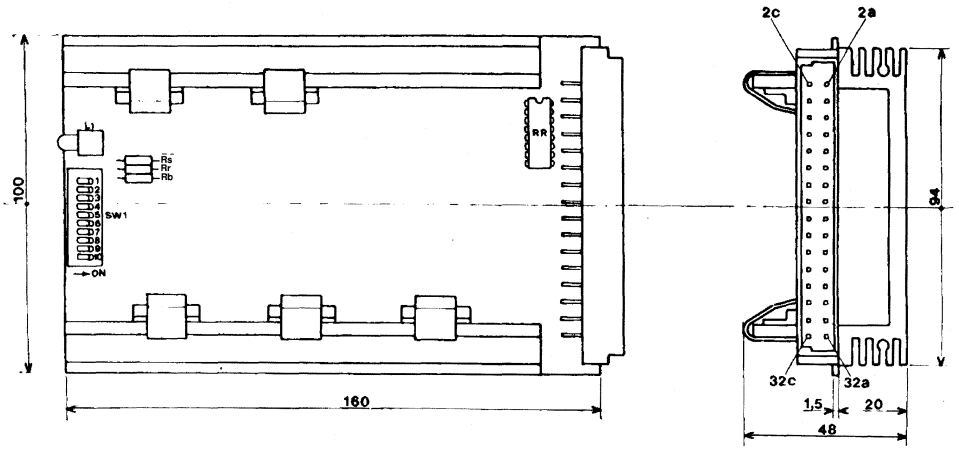


Figure 2. GS-D550 Block Diagram



CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm

GS-D550 Hardware available commands

SW1	Step clock transition selection
SW2	Direction polarity selection
SW3	Half/full step mode selection
SW4	Automatic current reduction at rest
SW5	2/5 phases drive selection
SW6	Boosted phase current selection
SW7	Fast/slow decay phase current recirculation selection
SW8	Fast recirculation time duration
SW9	Fast recirculation time duration
SW10	Fast recirculation time duration
R_r	Rest current resistor
R_S	Slew current resistor
R_b	Boost current resistor
R_R	Resistor array for logic level setting

GS-D550M BUS CONNECTOR PINS DESCRIPTION

The GS-D550M uses a 32 pins (16+16) DIN 41612-VG95324 male connector.

Pin	Function
2a	Step clock input: this is a logic input that performs the step function, i.e. on every transition of this input the motor is moved one step in the proper direction. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
2c	Return path for the Step clock input.
4a	Direction input; the logic state applied to this pin decides the rotation direction of the motor shaft. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
4c	Return path for the Direction input.
6a	Enable input; a logic high level applied to this input causes the power driver outputs to float. This condition allows the manual positioning of the system. Care must be used when this input is activated because the detention torque is lost. The input is isolated and its logic level can be selected among TTL, 12V and 24V.
6c	Return path for the Enable input.
8a	Current Boost input; a logic high level applied to this input causes the phase current value to rise to a predetermined level. In a particular condition of a DIP switch setting, the activation of this pin has the same effect as the ENABLE input. The input is isolated and its logic level can be selected between TTL, 12V, 24V.
10a	Fault logic output. This isolated output is at a low logic level whenever an anomalous condition is detected. The output is open collector, i.e. a pull-up resistor is required.
10c	Fault output return path. Must be connected to the driven logic ground.
12a	Synchronization signal for Microsteps/Step logic programming.
12c	Microsteps/Step rate remote programming.
14a-c	Supply bus discharge output; this output is activated when an overvoltage condition is detected. A resistive load connected between this pin and the supply bus can be used to sink power to limit the maximum supply voltage to safe conditions.
16a-c	Power supply ground.
18a-c	Power supply ground.
20a	Phase A- output.
20c	Phase B- output.
22a	Phase C- output.
22c	Phase D- output.
24a	Phase E- output.
24c	Phase A+ output.
26a	Phase B+ output.
26c	Phase C+ output.
28a	Phase D+ output.
28c	Phase E+ output.
30a-c	Module supply voltage; hazardous voltages may be present on these pins.

GS-D550 DESCRIPTION

The GS-D550 is a complete sybsystem to drive stepper motors in half/full step mode.
A very large number of auxiliary functions has been included to allow extreme simplicity and flexibility in use. Particular care has been devoted to protections, so that the GS-D550 can be safely used in very harsh environments.

MOTOR CONNECTION

The GS-D550 can be used to drive both two phases and five phases motors, therefore five output H-bridges power stages are present.
Particular care must be used to connect the motor windings so that they can be energized by the correct sequence and polarity.

To obtain the best overall performances it is recommended to respect the following common sense rules.

The connectors to the motor must be made by using low resistance twisted wires in order to minimize both losses and radiated noise.

If the distance is greater than 3 meters (10 feet) it's good practice to shield the cables and connect the shield to the supply voltage return pin of the board. This is only to meet the international rules for radiated noise.

Connection of two-phase, 4 wires motor

Two windings only are available so that the maximum phase current is the maximum current a H-bridge can deliver, i.e. 2.8 A.
The connection must be made as shown in fig. 3.
PHA and PHC must be mandatorily used.

Connection of two-phases, 8 wires motors

Two windings are available for a single phase. The maximum current per winding is still 2.8 A and the maximum phase current is, therefore, 5.6A.
The connection must be made as shown in fig. 4.
PHE output is not used. The use of 8 wires motors is recommended to achieve higher torque and tighter control of the phase current.

Connection of five-phase motors

A five-phase motor must be connected to the GS-D550 as shown in fig. 5.

Figure 4. Two-phase, Eight Wires Stepper Motor Connection

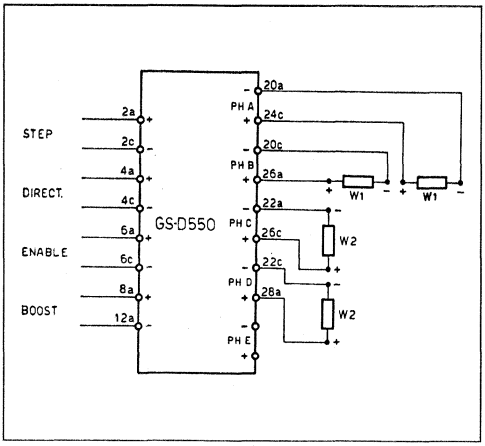


Figure 3. Two-phase, Four Wires Stepper Motor Connection

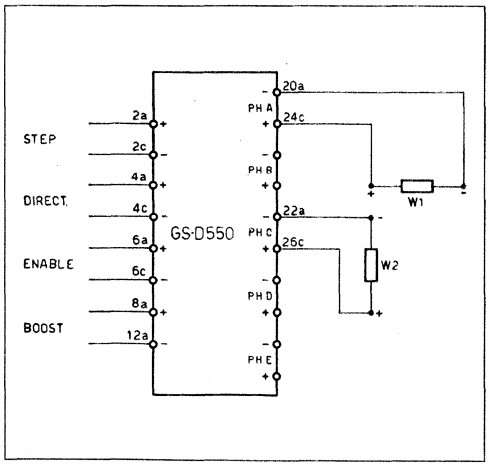
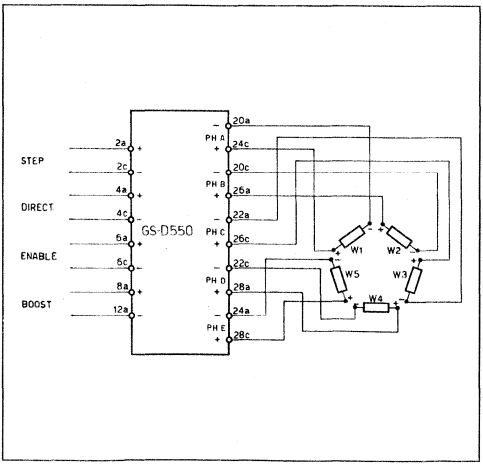


Figure 5. Five-Phase, Stepper Motor Connection



SUPPLY VOLTAGE

A single, unregulated supply voltage is requested to operate the board.

THE POWER SUPPLY MUST BE TURNED OFF WHEN PLUGGING OR UNPLUGGING THE BOARD.

The supply pins are: 30a, 30c positive rail
16a, 16c, 18a, 18c ground rail.

The other supply voltages needed by the board are internally generated by a high efficiency step down switch mode regulator that provides also the subsystem reset at power on.
The supply voltage range is between 18V and 42V: it is recommended to operate the board at a maximum voltage of 40V.
If an undervoltage condition is detected (V_S < 18V) the GS-D550 is automatically disabled and an LED is activated.

If a voltage above 42V is applied to the board, the following features are activated:

- An LED is turned on.
- An automatic overvoltage active clamping is turned on.

The active clamping system is implemented as shown in fig. 6.
The active overvoltage clamping is mainly intended to clamp transient overvoltages.

In case of permanent overvoltage, excessive power dissipation can occur. Therefore, if the supply voltage is derived from a rectified and filtered secondary winding of an AC main transformer, this voltage at no load and at maximum main AC voltage must be lower than 42V (50/60 Hz ripple included).
Overvoltages may occur because of transient spikes on the AC main supply, during very fast deceleration cycles and when the output bridges are in the fast decay recirculation mode. During this mode, the phase current pulses (up to 5.6 A) are returned to the supply voltage (four quadrant operation): if the impedance of the voltage supply is not adequately low, these current pulses can raise the voltage well above the nominal level.

To avoid that the overvoltage clamping is activated at a chopping mode switching frequency, a 4700µF/50V capacitor must be connected as close as possible to the supply pins.
The ESR of the capacitor at the switching frequency (about 20÷30 kHz) must be very low.

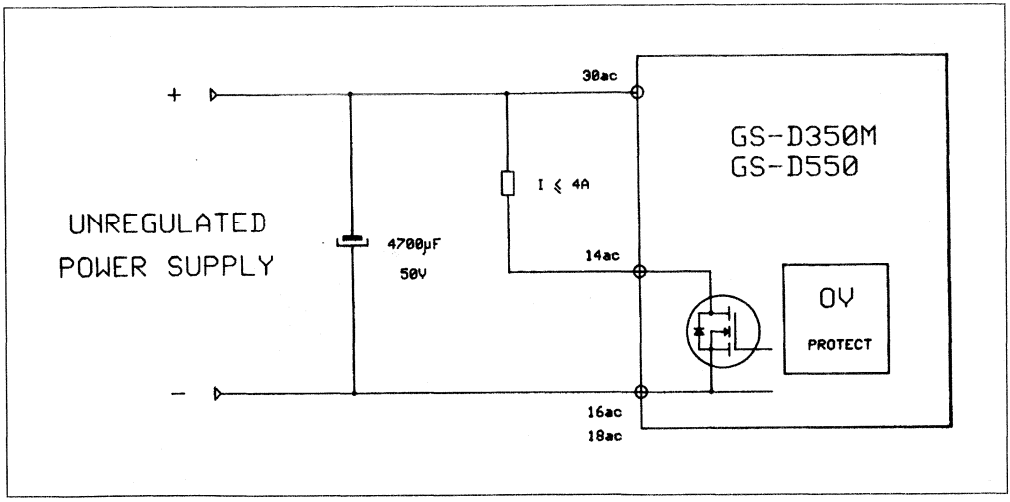
The power rating of the external bleeder resistor can range from 10 to 50W depending on AC main supply condition (overvoltage transients frequency). The resistor must be of a low inductance type to allow fast discharge of the bus voltage.

This value varies according to the operating conditions, but in first approximation it can be calculated according to the following formula:

$$R_{bleeder} \geq \frac{V_S}{4} [\Omega]$$

This is the minimum usable value.

Figure 6. Active Overvoltage Clamping



PHASE CURRENT PROGRAMMING

The maximum output current of each output bridge can be programmed according to the various tasks to be performed. This feature is particularly useful to drive the motor phase by a current that optimizes the torque value.

A typical movement of a positioning system has the speed profile shown in fig. 7.

To optimize the torque during the various conditions it is convenient to adopt a phase current profile as shown in fig. 8.

The phase current is boosted to the maximum value compatible with the motor cahacteristics during the positive and negative acceleration periods to reach as fast as possible the slew condition. This current is shown as I_b.

When the top speed is reached, the motor rotates at constant SLEW speed and the phase current can be reduced to the minimum value necessary to overcome the system losses (friction) and the load inertia. This current is shown as I_s.

During the STALL period the motor is at rest and the phase current can be further reduced to the bare minimum necessary to maintain the load in the right mechanical position. This current is shown as I_r.

The GS-D550 board allows the independent programming of the three values of I_r, I_s, I_b by the proper setting of resistors R_r, R_s, R_b. (See the mechanical drawing).
To calculate the proper values the following formulas apply:

$$K_r = \frac{5}{0.33 \cdot I_r} - 1 \qquad \text{Rest current factor}$$

$$K_s = \frac{5}{0.33 \cdot I_s} - 1 \qquad \text{Slew current factor}$$

$$K_b = \frac{5}{0.33 \cdot I_b} - 1 \qquad \text{Boost current factor}$$

then the three resistor values can be defined

$$R_r = K_r \qquad \text{Rest current setting resistor}$$

$$R_s = \frac{K_r \cdot K_s}{K_r - K_s} \qquad \text{Slew current setting resistor}$$

$$R_b = \frac{K_s \cdot K_b}{K_s - K_b} \qquad \text{Boost current setting resistor}$$

where I_r, I_s, I_b are expressed in Ampere (A),
R_r, R_s, R_b are expressed in kohm (kΩ).

If, for example, the following set of currents are required:

I_r = 1.16 A
I_s = 2.0 A
I_b = 2.5 A

the formulas give

$$K_r = \frac{5}{0.33 \cdot 1.16} - 1 = 12.0$$

$$K_s = \frac{5}{0.33 \cdot 2.0} - 1 = 6.57$$

Figure 7. Speed versus Time Profile

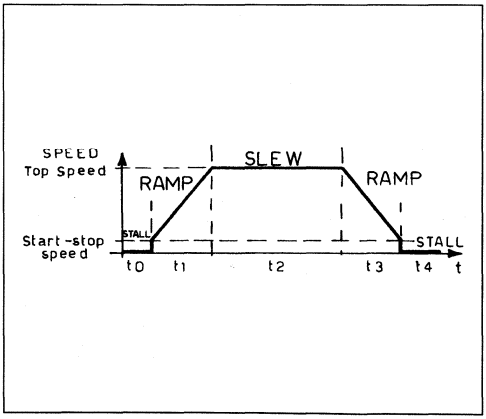
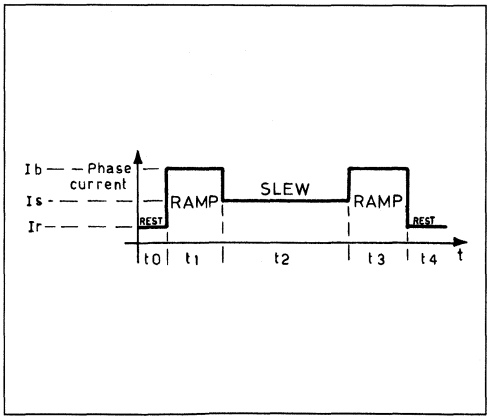


Figure 8. Phase Current versus Time Profile



$$K_b = \frac{5}{0.33 \cdot 2.5} - 1 = 5.06$$

Therefore

$$R_b = K_r = 12\ k\Omega$$

$$R_s = \frac{12 \cdot 6.57}{12 - 6.57} \approx 15\ k\Omega$$

$$R_b = \frac{6.57 \cdot 5.06}{6.57 - 5.06} = 22\ k\Omega$$

This example reports values that are the factory setting for R_r, R_b, R_s.

The three levels of phase current at rest, ramp and slew are actuated by internal and external commands conditioned by hardware commands setting as follows:

I_r Actuation

The actuation is automatically executed by the GS-D550 and it is conditioned by the position of the hardware command SW4 as per the following table.

SW4	STATUS
ON	No automatic reduction at rest
OFF	Automatic current reduction at rest.

I_s Actuation

No signal is needed and the condition is reached whenever the motor runs at top speed.

I_b Actuation

To boost the phase current during the ramps an external signal must be applied to pin 8a. The command is conditioned by the position of the hardware command SW6 as per the following table.

BOOST	SW6	PHASE CURRENT
ON	ON	BOOSTED
OFF	ON	NORMAL
ON	OFF	ZERO
OFF	OFF	NORMAL

PHASE CURRENT RIPPLE PROGRAMMING

The chopping control of the phase current implies automatically some amount of current ripple that depends on many parameters such as:

- supply voltage
- inductance L and resistance R of the motor windings
- back EMF
- method adopted for phase current recirculation during off-time (two quadrants or four quadrants)
- duration of the off-time when the current is allowed to decay.

The phase current ripple generates additional power dissipation inside the board (switching losses) and inside the motor.

A two quadrant recirculation mode (slow decay) causes the minimum current ripple, being all the other conditions equal and the minimum power dissipation. However the braking characteristics of the motor are impaired because of the high energy stored into the motor windings.

The four quadrant recirculation improves these braking characteristics, but it generates higher current ripple i.e. higher power dissipation.
It is quite important, therefore, to have the possibility to control the amount of current ripple.
The GS-D550 allows the user to program the ripple to a value that best fits to her/his needs.

Four hardware commands are provided to this purpose:

SW7, SW8, SW9, SW10

The conditions generated by these commands are shown by the following tables.

SW7	RECIRCULATION MODE
ON	Four quadrants
OFF	Two quadrants.

The first condition allows a fast decay but the current ripple is at its maximum for a given supply voltage, L/R time constant of the motor back EMF. Because the current ripple depends also on the off-time this maximum value can be decreased by reducing the off-time that is conditioned by the status of SW8, SW9, SW10 as follows:

SW8	SW9	SW10	OFF-TIME
OFF	OFF	OFF	12.6 µs
ON	OFF	OFF	11.0 µs
OFF	ON	OFF	9.4 µs
ON	ON	OFF	7.8 µs
OFF	OFF	ON	6.2 µs
ON	OFF	ON	4.6 µs
OFF	ON	ON	3.0 µs
ON	ON	ON	1.4 µs

STEP MODE SELECTION

The GS-D550 can drive the stepper motor according to two possible step modes:

- Full step
- Half step

To reduce the burden of the Host computer to a minimum just the clock signal must be provided externally to pin 2a: the driving signal sequence is generated inside the board and the stepping mode is defined by the hardware command SW3 as follows:

SW3	STEP MODE
ON	Half step
OFF	Full step

2/5 PHASE STEPPING MOTOR SELECTION

The connection of the motor windings is described on page 6 (MOTOR CONNECTION).

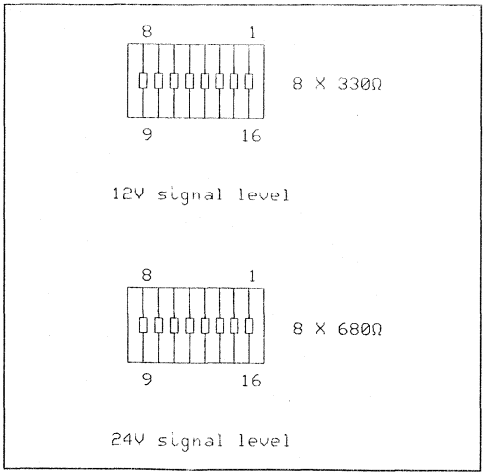
To drive motors with two or five phases, the GS-D550 must be properly set by acting on the hardware command SW5 according to the following table:

SW5	MOTOR
ON	Five phases
OFF	Two phases.

SETTING OF THE INPUT SIGNALS POLARITY

The flexibility of the GS-D550 is further enhanced by the availability of two additional hardware commands SW1, SW2, that allow to select the proper polarity of the input signals.

Figure 9. Input Signal Level Programming



SETTING OF THE ACTIVE EDGE OF THE STEP CLOCK

The step clock active edge i.e. the edge that advances the motor by one step, can be the rising or the falling edge depending on the position of the hardware command SW1.

SW1	ACTIVE TRANSITION
ON	Low-to-High
OFF	High-to-Low.

SETTING OF THE DIRECTION POLARITY

The rotation direction signal must be applied between pin 4a and 4c.

The direction (CW or CCW) depends on the status of the direction signal and on the position of the SW5 command as shown in the following table:

DIR SIGNAL	SW1	ROTATION
HIGH	ON	CCW
HIGH	OFF	CW
LOW	ON	CW
LOW	OFF	CCW

SETTING OF INPUT SIGNALS LEVEL

The input signals to the GS-D550 board are:

- Step clock
- Direction
- Enable
- Boost.

These four signals are galvanically isolated by internal opto couplers (isolation voltage: 500 V).

The board is enabled when pin 6a is low versus pin 6c. The input driving signals logic level can be selected according to the following options:

- TTL compatible
- 12 V
- 24 V

The factory setting is for TTL compatible signals. To modify the level, a DIL resistor array must be changed as shown in fig. 9.

BOARD PROTECTIONS

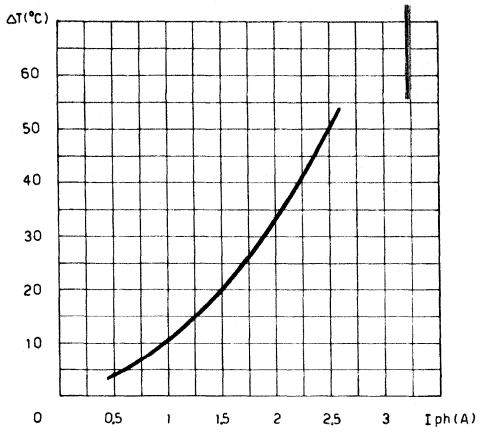
The board is protected against:

- Supply overvoltage
- Supply undervoltage
- Output short circuits: phase-to-supply
  phase-to-phase
  phase-to-ground
- Overtemperature

The thermal protection is activated when the temperature of the integral heatsink reaches about 90°C. In such a case the board is automatically disabled and the FAULT signal is activated.

The heatsink temperature depends on the ambient temperature and the internal power dissipation. Fig. 10 and 11 show the increase of heatsink temperature versus the phase current. The GS-D550 can be operated at a phase current up to 2A if the ambient temperature is less than 50°.

Figure 10. Two-phase mode thermal

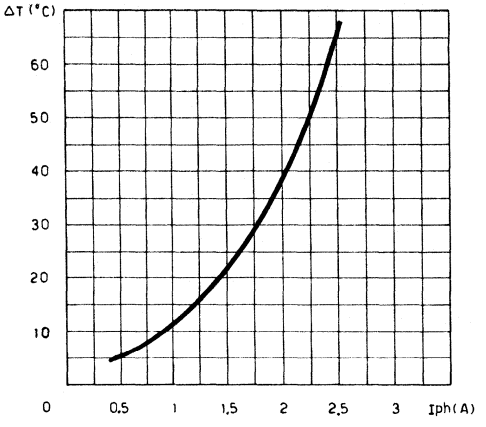


In case of out of range supply voltage and/or overloads the board is automatically disabled and the condition is signaled by an LED and by the FAULT signal.

FAULT SIGNAL

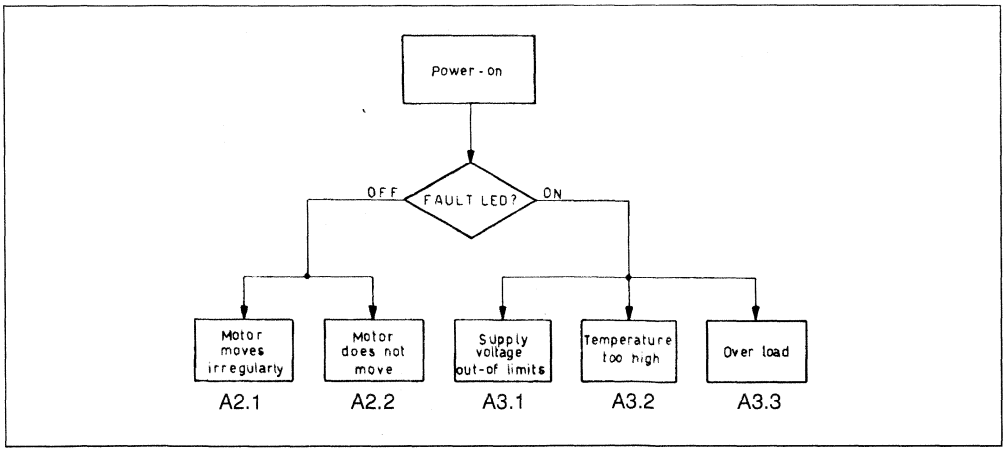
The FAULT signal is available at pin 10a and pin 10c. When a FAULT is present, pin 10a goes low versus pin 10c. This output is a galvanically isolated TTL signal.

Figure 11. Five-phase mode thermal



A-TROUBLE SHOOTING

A.1-Troubleshooting sequence



FAULT SIGNAL INACTIVE

A2.1-The motor moves irregularly if:

a) there is an error in the motor connection;
b) the step rate is close to the resonance frequency or too high;
c) the load plus friction torque is close to motor torque;
d) the motor is defective.

The corrective actions are:

a) check and correct the motor connections;
b) change the step rate;
c) increase the phase current or decrease the step rate;
d) substitute the motor.

A2.2-The motor doesn't move if:

a) there is an error in the motor connection;
b) the step-clock signal is not present, wrongly connected or badly timed;
c) the load plus friction torque is too high;
d) the motor is defective.

The corrective actions are:

a) check and correct the motor connections;
b) verify the Step-clock connection and the timing;
c) increase the phase current or use a larger motor;
d) substitute the motor.

A3-FAULT SIGNAL ACTIVE

The fault output is active when:

a) the supply voltage is lower than 18V;
b) the supply voltage is higher than 42V;
c) the heatsink temperature is higher than 90°C;
d) there is an output overload condition.

A3.1-An anomalous supply voltage condition occurs if:

a) the power supply is incorrectly set or a power supply fault has occurred;
b) the motor is used as a generator;
c) very fast deceleration is used.

The corrective actions are:

a) check and correct the power supply setting;
b) use the bus discharge circuit and limit the motor speed to safe values;
c) use the bus discharge circuit and longer deceleration times.

A3.2-The heatsink temperature is higher than 90°C if:

a) the ambient temperature (around the board) is too high.

The corrective actions are:

a) provide an adequate heatsink, space and ventilation to the board.

A3.3-An output overload condition is detected if:

a) an accidental short circuit phase-to-phase, phase-to-ground or phase-to-supply has occurred,
b) the motor has an internal short circuit.

The corrective actions are:

a) check the integrity of the connections between the board and the motor;
b) substitute the motor.

SGS-THOMSON MICROELECTRONICS

GS-DC200

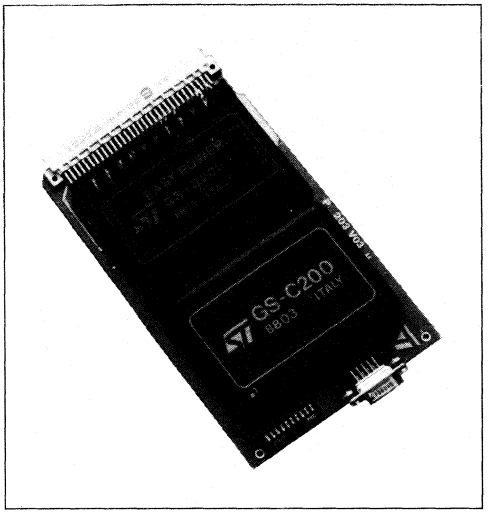
STEPPER MOTOR CONTROL AND DRIVE SYSTEM FAMILY

DESCRIPTION

The **GS-DC200** series is a family of single Eurocard boards that contain all the logic necessary to operate a stepper motor, including the instructions decoding, the step timing generation, the storage of the program to be executed. The motor interface can deliver phase current up to 2.5A.

The boards can be used as a stand alone complete motion control system or they can be driven by a central host computer.

The **GS-DC200** family is built around the **GS-C200**, **GS-C200S**, **GS-D200**, **GS-D200S** modules, (see the relevant data sheet) and it retains all the features of these modules.



SELECTION CHART

Ordering Number	Controller Sequencer Driver	Instruction Set Commands	Phase Current (A)
GS-DC200	GS-C200+GS-D200	25	2.0
GS-DC200S	GS-C200+GS-D200S	25	2.5
GS-DC200SS	GS-C200S+GS-D200S	29	2.5

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	42	V
T_{stg}	Storage Temperature Range	–40 to +105	°C
T_{hop}	Max Operating Heatsink Temperature (GS-D200/200S)	+85	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_S=24V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	DC Supply Voltage		12		40	V
I_S	Quiescent Supply Current			150		mA
V_i	Logic Input Voltage	Low High	 2		0.8 5	V V
V_o	Logic Output Voltage	Low High	 2		0.8 5	V V
I_{ph}	Programmable Phase Current	GS-DC200 GS-DC200S/SS			2 2.5	A A
f_c	Chopper Frequency			17		kHz
t_{cpw}	Clock Pulse Width				5	µs
t_{rpw}	Reset Pulse Width (Internal)				500	µs

MOTION CHARACTERISTICS

Speed Range	10 to 10000 steps
Speed Resolution	10 steps
Ramp Length	1 to 999 steps
Ramp Resolution	1 step
Positioning Range (GS-DC200/S)	0 to 9999999
Positioning Range (GS-DC200SS)	–8388608 to +8388607
Single Movement Range	1 to 999999 steps
Positioning Resolution	1 step
Positioning Repeatibility	± 0 step
Program Storage Capability	119 Bytes

COMMUNICATION PORT CHARACTERISTICS

SIGNAL LINES	3(TXD, RXD, GND)
BAUD RATE RANGE	110 to 9600
FORMAT	1 Start Bit
	7 Data Bit
	2 Stop Bit
	Odd Parity

Figure 1. GS-DC200, GS-DC200S and GS-DC200SS Block Diagram

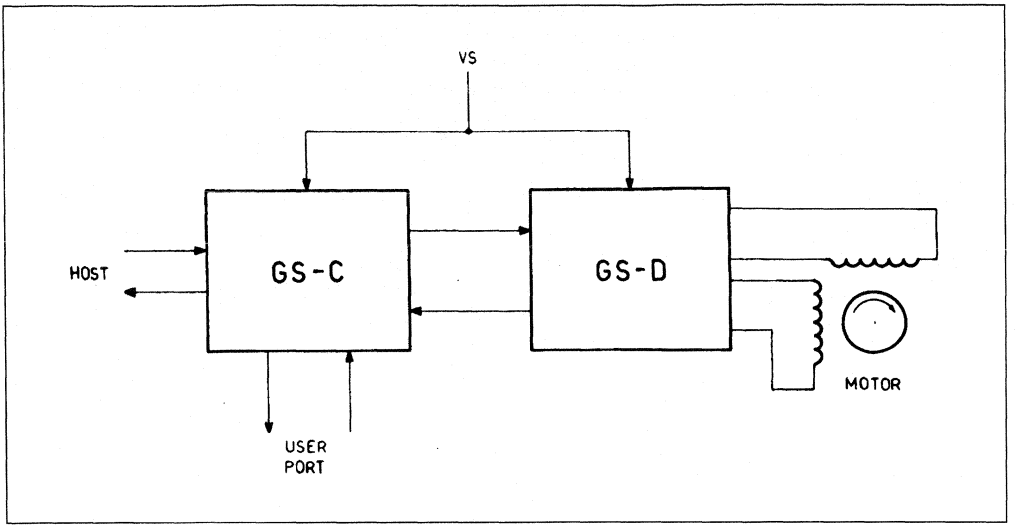
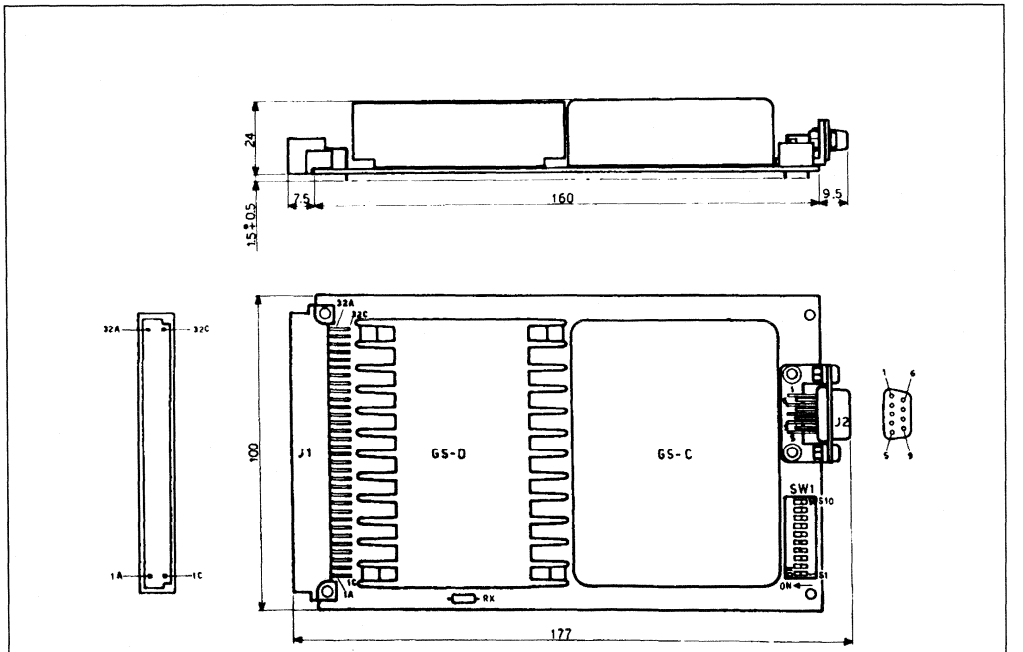
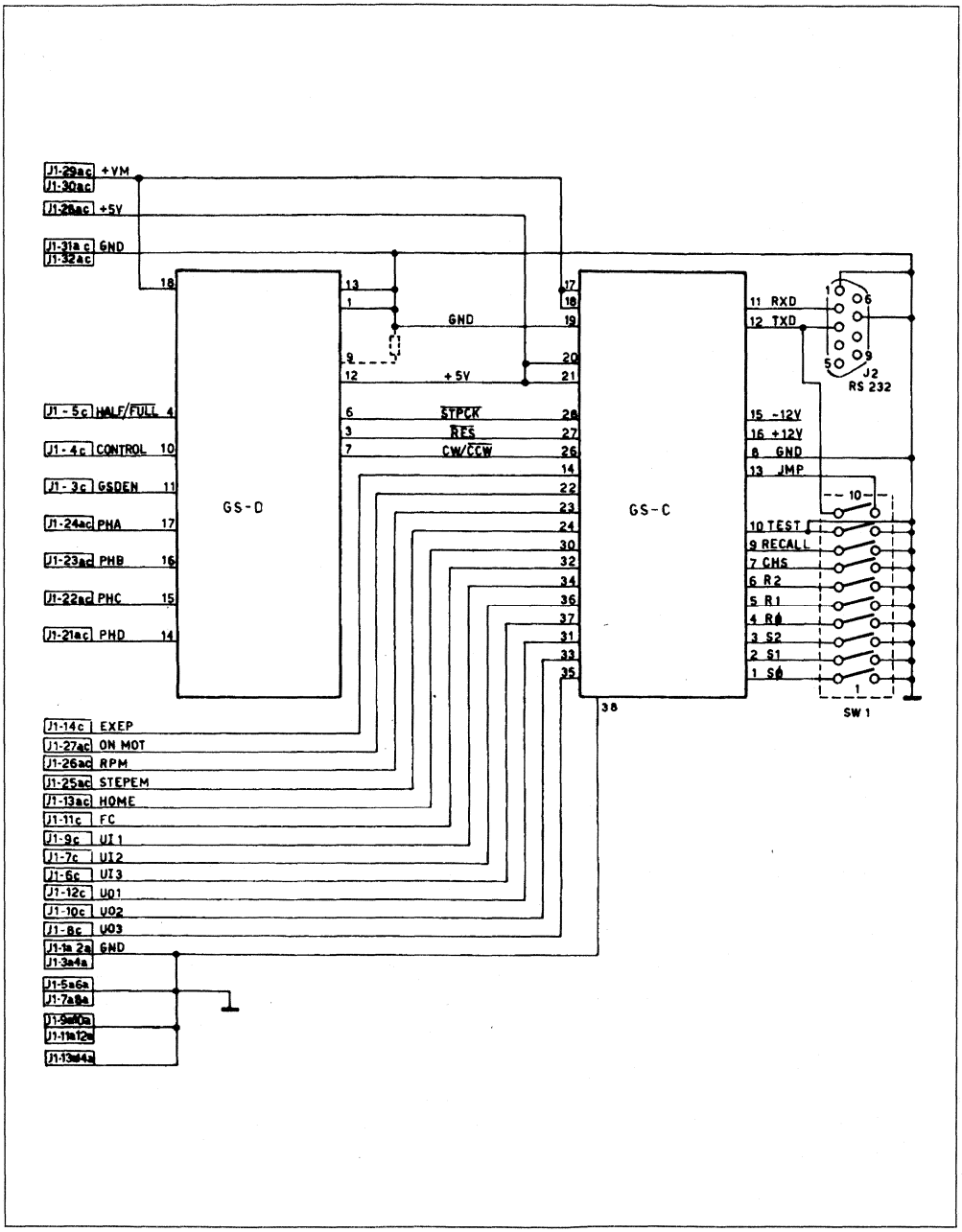


Fig. 2 - GS-DC Stepper Motor Driver/Controller Board



Dimensions in mm

Fig. 3 - GS-DC200, GS-DC200S and GS-DC200SS Schematic Diagram



GS-DC FAMILY BUS CONNECTOR PINS DESCRIPTION

The GS-DC family uses a 32 pin (16+16) DIN 41612-VG 95324 male connector and a RS-232 connector.

DIN BUS CONNECTOR (J1)

Pin	Row a Signal	Row c Signal
1	Ground	Not used
2	Ground	Not used
3	Ground	Power driver enable input
4	Ground	Power driver control input
5	Ground	Half/Full step select
6	Ground	User input 3
7	Ground	User input 2
8	Ground	User output 3
9	Ground	User input 1
10	Ground	User output 2
11	Ground	End-of-travel switch
12	Ground	User output 1
13	Ground	Home switch
14	Ground	Prog. under execution output
15	Not used	Not used
16	Not used	Not used
17	Not used	Not used
18	Not used	Not used
19	Not used	Not used
20	Not used	Not used
21	Phase D output	Phase D output
22	Phase C output	Phase C output
23	Phase B output	Phase B output
24	Phase A output	Phase A output
25	Step enable input	Stop enable input
26	Ramp in execution logic output	Ramp in execution logic output
27	Motor moving	Motor moving
28	+5V output	+5V output
29	Supply voltage	Supply voltage
30	Supply voltage	Supply voltage
31	Supply ground	Supply ground
32	Supply ground	Supply ground

RS-232 CONNECTOR (J2 - DB9)

Pin 1	Ground
Pin 2	Received data input
Pin 3	Transmitted data output
Pin 7	Ground

GS-DC FAMILY HARDWARE AVAILABLE COMMANDS

Dip switch configuration selection (0=OFF 1=ON)

S1	S2	S3	Address	Protocol
0	0	0	–	Point-to-point
1	0	0	1	Multipoint
0	1	0	2	Multipoint
1	1	0	3	Multipoint
0	0	1	4	Multipoint
1	0	1	5	Multipoint
0	1	1	6	Multipoint
1	1	1	7	Multipoint

S4	S5	S6	Baud rate
0	0	0	110
1	0	0	150
0	1	0	300
1	1	0	600
0	0	1	1200
1	0	1	2400
0	1	1	4800
1	1	1	9600

S7	Checksum
1	Disable
0	Enable

S8	Stand alone operation
1	Enable
0	Disable

Note: Switch position 9 is not used.

S10	RS232 TXD pull-down
0	Not connected
1	Connected

Rx	Phase peak current programming

USER NOTES

To correctly operate the GS-DC boards family, it is recommended to read the following data sheets: GS-C200/200S; GS-D200/200S; GS-C200 PROG.

Supply Voltage

The recommended operating maximum supply voltage must include the ripple voltage on the V_S supply rail and it must not exceed 40V to avoid permanent damage to the board.

The boards have internal capacitors connected between the supply and ground pins to assure the electrical stability. These capacitors cannot handle high values of current ripple and they would be permanently damaged if the voltage source impedance is not adequately low.

The use of a low ESR, high current ripple, 470µF/50V capacitor located as close as possible to the board is recommended. Suitable units are the Sprague type 672 D or 678 D, the RIFA type PEC 126 or any equivalent unit.

Board Protections

The GS-DC200 board is protected against occasional or permanent short circuits to the supply voltage of the phase output pins.

The GS-DC200S and GS-DC200SS are protected also against short circuits to ground or to another phase output.

For the GS-DC200S and GS-DC 200SS the protection is of the latching type i.e. when an overload occurs, the board is automatically disabled. To restart the operations, the supply voltage must be switched off for at least 100 ms.

Motor Connection

When long wires are needed to connect a remote motor, it is recommended to use twisted pair cables with a proper cross section to minimize DC losses and RFI problems.

Phase Current Programming

The maximum output current/phase can be programmed by changing the value of the R_X resistor. The factory setting is for maximum current of

1 A GS-DC 200

2 A GS-DC200S / GS-DC200SS.

The new value of R_X resistor for a different value of maximum phase current I (A) can be calculated according to the following formulas:

GS-D200

I > 1A

$$Rx = [\frac{10 - I}{0.993 * I - 1}]\ k\Omega \quad Rx \geq 8.2K\Omega$$

I < 1A

$$Rx = [\frac{I}{1 - 0.993 * I}]\ k\Omega$$

GS-D200S

I > 2A

$$Rx = [\frac{10 - 0.33 * I}{0.473 * I - 1}]\ k\Omega \quad Rx \geq 50K\Omega$$

I < 2A

$$Rx = [\frac{I}{1 - 0.993 * I}]\ k\Omega$$

The maximum programmed current must not exceed 2.0A for the GS-DC200 and 2.5A for the GS-DC200S/GS-DC200SS.

Thermal Characteristics

The maximum power dissipation occurs on the GS-D200/GS-D200S modules used on the boards. The thermal resistance case-to-ambient of the integral heatsink of these modules is 5°C/W. This means a 50°C temperature increase of the heatsink if the internal power dissipation is 10W.
The maximum allowed heatsink temperature is 85°C. Therefore, according to the ambient temperature and/or the internal power dissipation, forced ventilation may be required.

Programming

To correctly program motion sequences, see the GS-C200/200S and/or GS-C200 PROG data sheets.

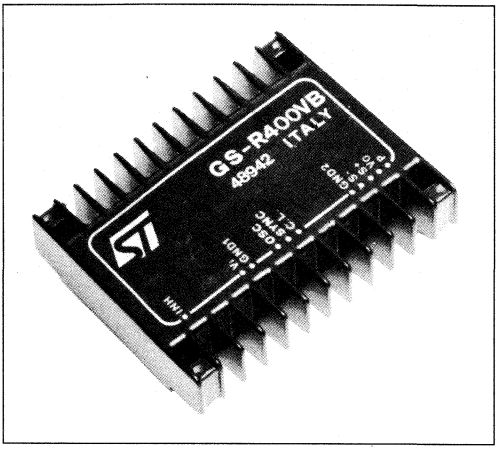
SGS-THOMSON MICROELECTRONICS

GS-R400 FAMILY

20W TO 140W STEP-DOWN SWITCHING REGULATOR FAMILY

FEATURES

- MTBF in excess of 200,000 hours
- 4A max output current
- 46V max input voltage
- 4V max drop-out voltage
- Soft start
- Remote logic inhibit/enable
- Remote output voltage sense
- Non-latching overload and short circuit protection
- Crow-bar output overvoltage protection



DESCRIPTION

The GS-R400 series is a versatile family of high current, high voltage step-down switching voltage regulators.

The integral heatsink allows a large power handling capability and it provides also an effective shielding to minimize EMI.

SELECTION CHART

Type Ordering Number	Output Voltage (V)	Input Voltage (V)	Output Ripple (mVpp)	Regulation Line (mV/V)	Regulation Load (mV/A)	Efficiency (%)	Notes
GS-R405	5.1 ± 2%	9 to 46	25	2	20	70	Fixed output voltage
GS-R412	12.0 ± 4%	16 to 46	50	5	40	80	"
GS-R415	15.0 ± 4%	19 to 46	65	5	60	85	"
GS-R424	24.0 ± 4%	28 to 46	100	6	90	90	"
GS-R405S	5.1 ± 2%	9 to 46	25	2	20	70	Reset output
GS-R400V	5.1 to 40	Vo+4 to 46	25 to 100	6	20 to 90	70 to 90	Progr. output voltage
GS-R400VB	5.1 to 40	Vo+4 to 46	25 to 100	6	20 to 90	70 to 90	Progr. output voltage and current. Frequency synchr.

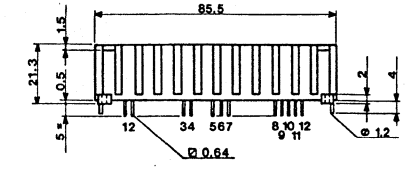
Note: The line regulation is measured at I_{out}=1A
The load regulation is measured at V_{in}=V_O+8V and I_{out}=1 to 3A
For $V_O \geq 36V$ and I_o = 4A an external heatsink or forced ventilation are required.

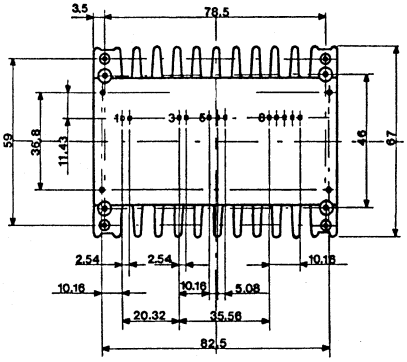
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	48	V
I_{rt}*	Reset Output Sink Current	20	mA
T_{stg}	Storage Temperature Range	–40 to +105	°C
T_{cop}	Operating Case Temperature Range	–20 to +85	°C

* GS-R405S only

CONNECTION DIAGRAM AND MECHANICAL DATA





Pin 2 GS-R405S only
Pin 5,6,7 GS-R400VB only
Pin 12 GS-R400V/VB only

Dimensions in mm

Bottom view

PIN DESCRIPTION

Pin	Function	Description
1	Inhibit	The module is disabled by a high logic level applied to this pin.
2	Reset	Reset output (GS-R405S only).
3	+ Input	DC input voltage. Recommended maximum voltage is 46V.
4	Input GND	Return for input voltage source.
5	Oscillator	100kHz oscillator output. To be connected to Sync (pin 6) input if the unit is a master and left open if it is a slave (GS-R400VB only). See fig. 5.
6	Sync	Synchronization input. To be connected to the Oscillator output (pin 5) of the master (GS-R400VB only). See fig. 5.
7	Current limiting	A resistor ($\geq$2.2kΩ) connected from this pin to pin 9 sets the current limiting level (GS-R400VB only).
8	Output GND	Return for output current path. Internally connected to pin 4.
9	– Sense	Senses the remote load return. Must be tied to pin 8 when the remote sensing feature is not used. See fig. 1.
10	+ Sense	Senses the remote load high side. Must be tied to pin 11 when the remote load sensing feature is not used. See fig. 1.
11	+ Output	Regulated DC output voltage.
12	Program	A resistor ($\leq$18kΩ) connected between this pin and pin 10 sets the output voltage (GS-R400V and GS-R400VB only).

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$\Delta V_O/\Delta T$	Temperature Stability	V_i=V_O+8V I_O = 1A		0.2/1.6		mv/°C
I_O	Output Current	V_i=V_O+8V	0.2		4	A
I_{OL}	Current Limit	V_i=V_O+8V		5	8	A
I_{isc}	Average Input Current	V_i=46V Output Shorted		0.1	0.2	A
f_S	Switching Frequency	I_O=1A		100		KHz
SVR	Supply Voltage Rejection	f_O=100Hz I_O=1A		4/12		mV/V
V_r	Ripple Voltage	I_O=2A		25/150		mV_{pp}
t_{ss}	Soft Start Time	V_i=V_O+8V		10/35		ms
V_{inhl}	Low Inhibit Voltage				0.8	V
V_{inhh}	High Inhibit Voltage		2		5.5	V
I_{inhh}	High Inhibit Input Current	V_{inh}=5V			500	µA
tcb	Crow-bar Delay Time			5		µs
V_{rh}*	Reset High Level			5		V
V_{rl}*	Reset Low Level	I_{rl} = 5mA I_{rl} = 10mA			0.2 0.4	V
t_{rd}*	Reset Delay Time			100		ms
V_{cth}	Crowbar Intervention Threshold			V_O•1.25		V
V_{sd}	Voltage Sense Compensation (per leg)				250	mV
R_{th}	Thermal Resistance	Case to ambient		5		°C/W

* GS-R405S only

USER NOTES

Input Voltage

The recommended operating maximum DC input voltage is 46V inclusive of the ripple voltage.

Remote Sensing

The remote voltage sense compensation range is for a total drop of 500mV equally shared between the load connecting wires. It is a good practice to shield the sensing wires to avoid oscillation.
Each sense input must be connected to its companion output power pin when the remote sense capability is not used (see fig. 1).

Case Grounding

The module case is internally connected to pin 9 and it must be isolated from ground (pins 4 and 8) when the remote sense capability is used.
The PCB area below the module can be used as an effective sixth side shield against EMI.

Thermal Characteristics

The case-to-ambient thermal resistance of all the GS-R400 modules is about 5°C/W. This produces a 50°C temperature increase of the module surface for 10W of internal power dissipation.
Depending on the ambient temperature and/or on the power dissipation, an additional heatsink or forced ventilation may be required.

Input Impedance

The module has an internal capacitor connected between the input pins in order to assure PWM stability. This capacitor cannot handle large values of high frequency ripple current and it can be permanently damaged if the primary energy source impedance is not adequate. The use of an external low ESR, high ripple current capacitor located as close the module as possible is recommended.
Suitable units are the SPRAGUE type 672D and 678D and the RIFA type PEG 126 or any equivalent unit. When space is a limitation, a 22µF ceramic

multilayer capacitor must be connected to the module input pins.

Output Voltage Programming

The GS-R400V and GS-R400VB output voltage is programmed by using a resistor (see pin function table and fig. 4). The resistor must be located very close the module and the PCB layout must mimimize injected noise. The value of the resistor is calculated by using the following formula:

$$R_V = 2.67 \left(\frac{V_O}{5.1} - 1 \right) k\Omega$$

V_O can be adjusted between 5.1 and 40V.

Current Limiting Programming

The GS-R400VB current limiting is programmed by using a resistor (see pin function table and fig. 4).

The value of the resistor is calculated by using the following formula:

$$R_i = [2.2 + (5 \bullet I_O)]\ k\Omega$$

Module Protection

The modules are protected against occasional and permanent short circuits of the output pin to ground, as well as against output current overload.
When the output current exceeds the maximum value, the output is automatically disabled. After a fixed time the module starts again in a soft mode. The cycle is repeated until the overload condition is removed.
A crowbar output overvoltage protection is activated whenever the output voltage exceeds the nominal output voltage by more than 25%.

Figure 1. Load Connection

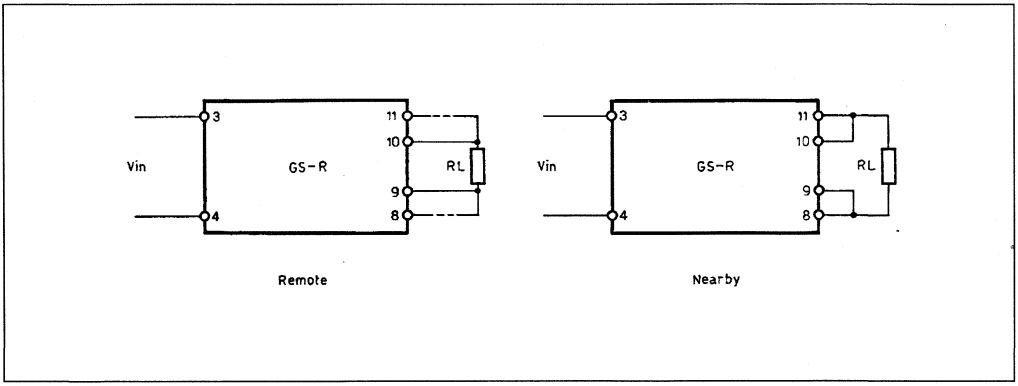


Figure 2. Remote Inhibit Operation

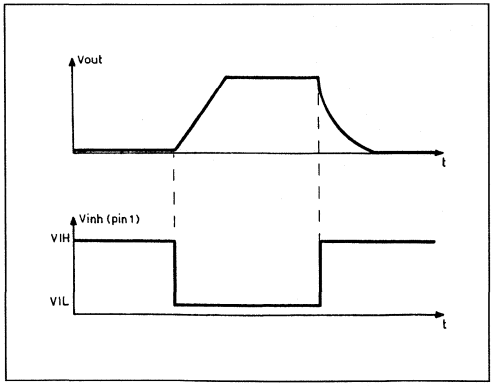


Figure 3. Reset Operation

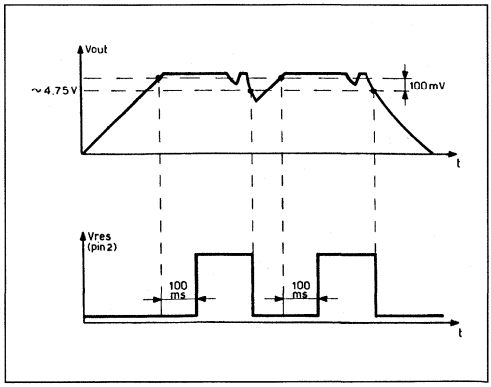


Figure 4. Voltage and Current Programming

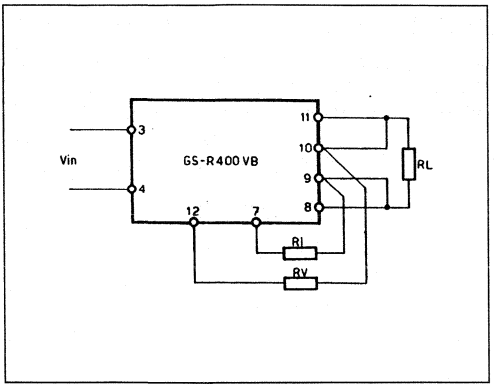
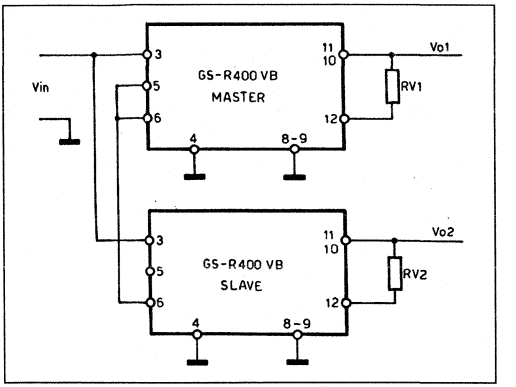


Figure 5. Multiple Units Synchronization



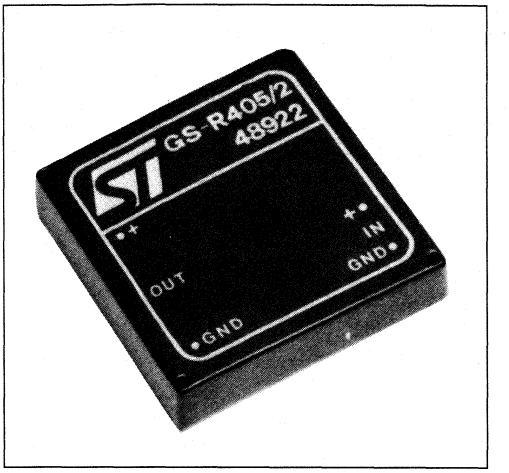
SGS-THOMSON MICROELECTRONICS

GS-R400/2 FAMILY

SMALL SIZE STEP-DOWN SWITCHING REGULATOR FAMILY

FEATURES

- MTBF in excess of 500,000 hours
- 4A max output current
- 40V max input voltage
- 4V max drop-out voltage
- Soft start
- Non-latching short circuit protection
- Crow-bar output overvoltage protection



DESCRIPTION

The GS-R400/2 series is a family of small sized high current, high voltage step-down switching regulators.

The integral heatsink allows a large power handling capability and it provides also an effective shielding to minimize EMI.

SELECTION CHART

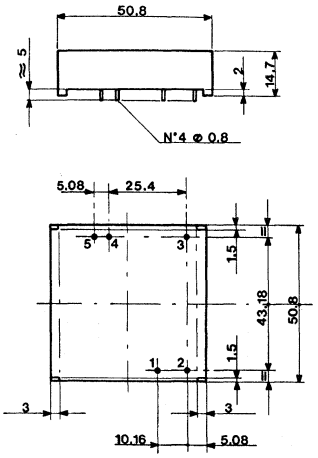
Type Ordering Number	Output Voltage (V)	Input Voltage (V)	Output Ripple (mVpp)	Regulation		Efficiency (%)	Notes
				Line (mV/V)	Load (mV/A)		
GS-R405/2	5.1 ± 2%	9 to 40	25	2	20	80	Fixed output voltage
GS-R412/2	12.0 ± 4%	16 to 40	50	5	40	85	"
GS-R415/2	15.0 ± 4%	19 to 40	65	6	60	87	"
GS-R424/2	24.0 ± 4%	28 to 40	100	6	80	90	"
GS-R400V/2	5.1 to 24	Vo+4 to 40	25 to 100	2 to 6	20 to 80	80 to 90	Progr. output voltage

Note : Line regulation is measured at I_{out}=1A.
Load regulation is measured at $V_{in}=V_o+8V$ and I_{out}=0.5 to 1.5A.
Case temperature must be kept below 85° C

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	42	V
I_o	Output Current	4	A
T_{stg}	Storage Temperature Range	–40 to +105	°C
T_{cop}	Operating Case Temperature Range	–20 to +85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Pin 5 GS-R400V/2 only

Dimensions in mm Bottom view

PIN DESCRIPTION

Pin	Function	Description
1	+ Input	DC input voltage. Recommended maximum voltage is 40V.
2	Input GND	Return for input voltage source.
3	Output GND	Return for output current path. Internally connected to pin 2.
4	+ Output	Regulated DC output voltage.
5	Program	A resistor (<10kΩ) connected between this pin and pin 4 sets the + output voltage of the GS-R400V/2.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$\Delta V_O/\Delta T$	Temperature Stability	V_i=V_O+8V I_O = 1A		0.2/0.6		mV/°C
I_O	Output Current	V_i=V_O+8V	0.1		4	A
I_{OL}	Current Limit	V_i=V_O+8V		5	8	A
I_{isc}	Average Input Current	V_i=40V Output Shorted		0.1	0.2	A
f_S	Switching Frequency	I_O=1A		100		kHz
SVR	Supply Voltage Rejection	f_O=100Hz I_O=1A		4/12		mV/V
V_r	Ripple Voltage	I_O=1A		25/100		mVpp
tss	Soft Start Time			10/35		ms
tcb	Crowbar Delay Time			5		µs
Vcth	Crowbar Intervention Threshold			V_O•1.25		V
Rth	Thermal Resistance	Case to ambient		8		°C/W

USER NOTES

Input Voltage

The recommended operating maximum DC input voltage is 40V inclusive of the ripple voltage.

Case Grounding

The module case is internally connected to pin 2 and pin 3.
The PCB area below the module can be used as an effective sixth side shield against EMI.

Thermal Characteristics

The case-to-ambient thermal resistance of all the GS-R400/2 modules is about 8°C/W. This produces a 32°C temperature increase of the module surface for 4W of internal power dissipation.
Depending on the ambient temperature and/or on the power dissipation, an additional heatsink or forced ventilation may be required.

Input Impedance

The module has an internal capacitor connected between the input pins in order to assure PWM stability. This capacitor cannot handle large values of high frequency ripple current and it can be permanently damaged if the primary energy source impedance is not adequate.
The use of an external low ESR, high ripple current capacitor located as close the module as possible is recommended.
Suitable units are the SPRAGUE type 672D and 678D and the RIFA type PEG 126 or any equivalent unit. When space is a limitation a 22µF ceramic multilayer capacitor must be connected to the module input pins.

Output Voltage Programming

The GS-R400V/2 output voltage is programmed by using a resistor.
The resistor must be located very close the module and the PCB layout must minimize injected noise. The value of the resistor is calculated by using the following formula:

$$R_V = 2.67 \left(\frac{V_o}{5.1} - 1 \right) k\Omega$$

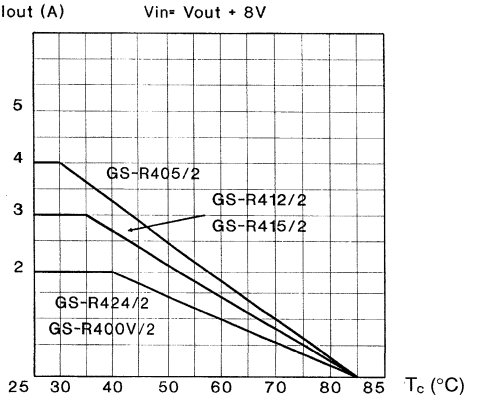
V_o can be adjusted between 5.1 and 24V.

Module Protection

The modules are protected against occasional and permanent short circuits of the output pins to ground. During short circuit (when the output current exceeds the maximum value) the output is automatically disabled. After a fixed time the module starts again in a soft mode. The cycle is repeated until the short circuit condition is removed.

The module can be permanently damaged if the case temperature exceeds 85° C

Power Derating Curve



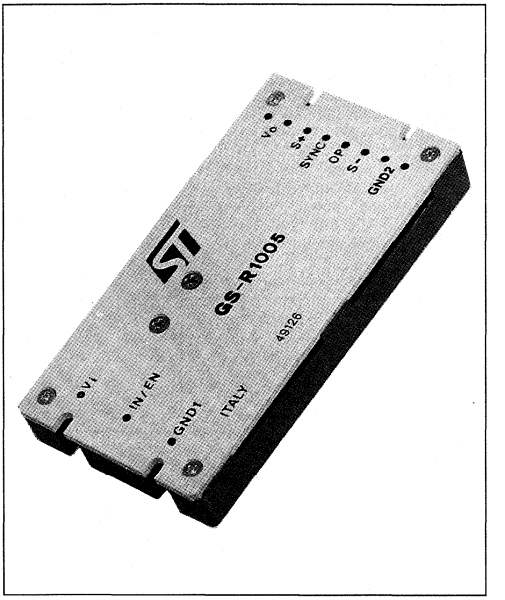
SGS-THOMSON MICROELECTRONICS

GS-R1005

50W STEP-DOWN SWITCHING REGULATOR

FEATURES

- Wide input voltage range (12 to 36V)
- High efficiency (80% min.)
- Parallel operation with current sharing
- Synchronization
- Remote inhibit/enable
- Remote load voltage sense
- Output short-circuit protection
- Soft-start
- PCB or chassis mountable



DESCRIPTION

The **GS-R1005** is a step-down switching voltage regulator suitable to provide 5V/10A output voltage from a wide input voltage range (12 to 36V).

ABSOLUTE MAXIMUM RATINGS

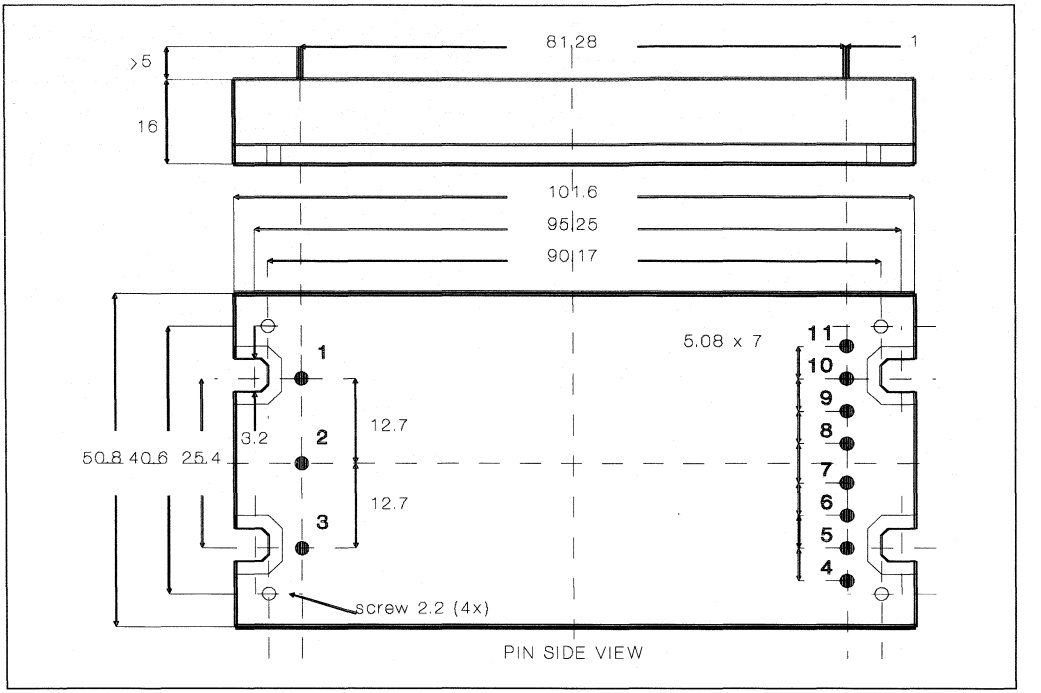
V_i	DC Input Voltage	40	V
V_{iinh}	High Inhibit voltage	28	V
T_{stg}	Storage Temperature Range	–20 to +105	°C
T_{cop}	Operating Case Temperature Range	0 to +75	°C

ELECTRICAL CHARACTERISTICS ($T_{amb.}$ = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 5.05V	I_O = 1.2 to 10A	12	24	36	V
I_i	Input Current	V_i = 24V	I_O = 10A	2.5	A		
I_{ir}	Reflected Input Current	V_i = 24V	I_O = 10A		200	220	mApp
		with external filter (C= 470µF)					
Vien	Enable Input Voltage	V_i = 12 to 36V	I_O = 1.2 to 10A	0		1.2	V
Viinh	Inhibit Input Voltage	V_i = 12 to 36V	I_O = 1.2 to 10A	2		24	V
Iiinh	Inhibit Input Current	V_i = 12 to 36V	I_O = 1.2 to 10A		0.3	0.5	mA
V_O	Output Voltage	V_i = 12 to 36V	I_O = 1.2 to 10A	4.9	5.05	5.2	V
Vor	Output Ripple Voltage	V_i = 24V Io= 10A			100	120	mVpp
δV_O	Line Regulation	V_i = 12 to 36V	I_O = 10A			0.5	%
δV_O	Load Regulation	V_i = 24V	I_O = 1.2 to 10A			1	%
δV_O	Remote Sense Compensation	V_i = 24V I_O =				0.5	V
I_O	Output Current*	V_i = 12 to 36V V_O = 5.05V		0		10	A
Iol	Output Current Limiting	V_i = 12 to 36V		12.5		13.7	A
Iosc	Short-circuit Output Current	V_i = 24V				16	A
δI_O	Current Sharing Deviation	V_i = 24V I_O = 2 to 10A two modules in parallel				10	%
η	Efficiency	V_i = 12 to 36V I_O = 10A		80	83		%
fs	Switching Frequency	V_i = 24V I_O = 1.2 to 10A			100		kHz
tss	Soft-start Time	V_i = 24V I_O = 10A			15		ms
tr1	Line Transient Recovery Time	V_i = 12 to 36V I_O = 5A			60		µs
tr2	Load Transient Recovery Time	V_i = 24V I_O = 1.2 to 10A			100		µs
Rthc	Thermal Resistance Case-to-ambient				7.5		°C/W

* Note: when output current is less than 1.2A, output ripple voltage increases due to discontinuous operation.

CONNECTION DIAGRAM AND MECHANICAL DATA



PIN DESCRIPTION

Pin	Function	Description
1	GND Input	Return for input voltage source. Internally connected to pin 10,11.
2	Inhibit	The converter is ON (Enable) when this pin is unconnected or the voltage applied is lower than 1.2V. The converter is OFF (Inhibit) for a control voltage in the range of 2 to 24V.
3	+Vin	DC Input voltage; recommended maximum voltage is 36V. External capacitor between pin 3 and pin 1 is mandatory; recommended value is 470µF/50V for switching application.
4,5	+ Vout	+5V output voltage.
6	+ Sense	Senses the remote load high side. To be connected to pin 4,5 when remote sense is not used.
7	Sync	Synchronization output. See figures 1,2,3,4. Open when not used.
8	Parallel	Parallel output. See figures 1,2,3,4. Open when not used.
9	– Sense	Senses the remote load return. To be connected to pin 10,11 when remote sense is not used. In parallel configuration
10,11	GND Output	Return for output current path. Internally connected to pin 1.

USER NOTES

Input Voltage

The recommended operating maximum DC input voltage is 36V inclusive of the ripple voltage. The use of an external low ESR, high ripple current capacitor located as close the module as possible is mandatory; recommended value is 470µF/50V.

Softstart

To avoid heavy inrush current the output voltage rise time is typically 15ms in any condition of load.

Remote Sensing

The remote voltage sense compensation range is for a total drop of 500mV equally shared between the load connecting wires. It is a good practice to shield the sensing wires to avoid oscillations. See the connection diagram on figures 1, 2, 3, 4.

Parallel Operation

To increase available output regulated power, the module features the parallel connection possibility with equal current sharing and maximum deviation of 10% (two modules in parallel). See the connection diagram on figures 1, 2, 3, 4.

Module Protection

The module is protected against occasional and permanent shortcircuits of the output pins to ground as well as against output current overload. It uses a current limiting protection circuitry, avoiding latch-up problems with certain types of loads.

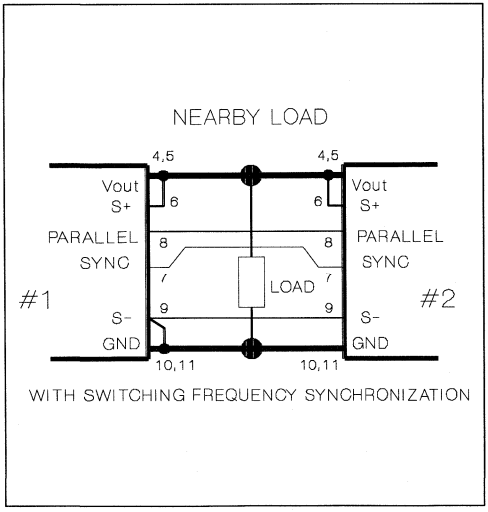
Thermal characteristics: how to choose the heat-sink

Sometimes the **GS-R1005** requires an external heat-sink depending on both operating temperature conditions and power.
Before entering into calculations details, some basic concepts will be explained to better understand the problem.
The thermal resistance between two points is represented by their temperature difference in front of a specified dissipated power, and it is expressed in Degree Centigrade per Watt (°C/W).
For GS-R1005 the thermal resistance case to ambient is 7.5°C/W.
This means that an internal power dissipation of 1W will bring the case temperature at 7.5°C above the ambient temperature.
The maximum case temperature, at which the module provides 10A, is 75°C (see fig.6).
Let's suppose to have a GS-R1005 that delivers a load current of 10A at an ambient temperature of 40°C.
The dissipated power in this operating condition is about 10.2W (at typical efficiency of 83%), and the case temperature of the module will be:

Tcase = Tamb+PdxRth = 40+10.2x7.5 = 116.8°C

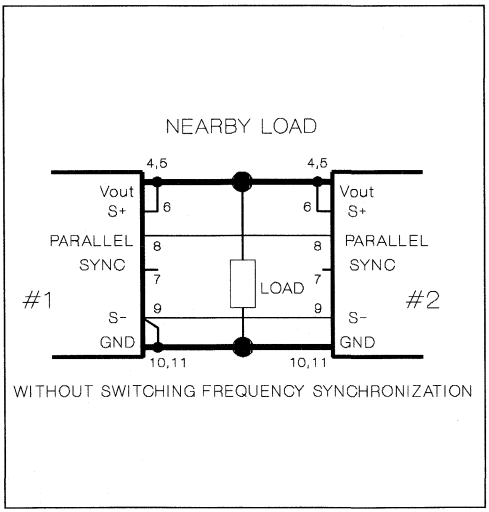
This value exceeds the maximum allowed temperature and an external heat-sink must be added. To

Figure 1



WITH SWITCHING FREQUENCY SYNCHRONIZATION

Figure 2



WITHOUT SWITCHING FREQUENCY SYNCHRONIZATION

Figure 3.

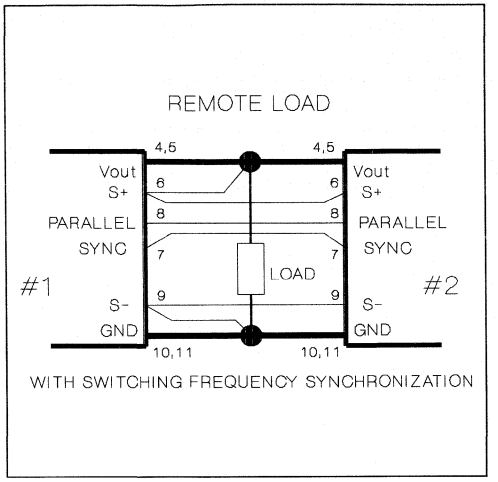
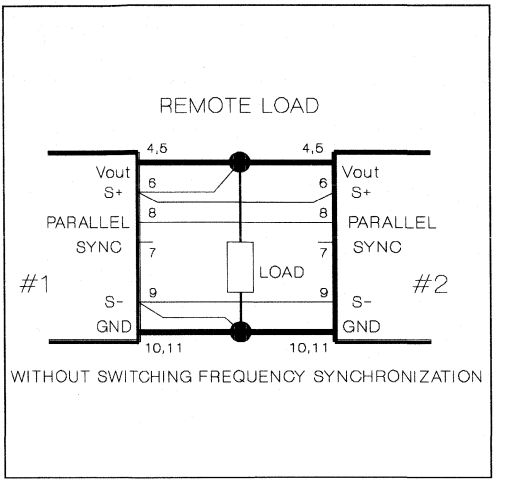


Figure 4.



this purpose four holes (see mechanical drawing) are provided on the metal surface of the module. To calculate this heat-sink, let's first determine what the total thermal resistance should be.

$$Rth = \frac{Tcase\ (max)\ Tamb}{Pd} = \frac{75-40}{10.2} = 3.421\ °C/W$$

This value is the resulting value of the parallel connection of GS-R thermal resistance and of the additional heatsink thermal resistance.

$$\frac{Rth\ (GSR) \times Rth\ (Heatsink)}{Rth\ (GSR) + Rth\ (Heatsink)} = 3.42\ °C/W$$

To calculate the thermal resistance of the additional heat-sink the following equation may be used:

$$Rth\ (Heatsink) = \frac{3.42 \times Rth(GSR)}{Rth\ (GSR) - 3.42} = \frac{3.42 \times 7.5}{7.5-3.42} = 6.29\ °C/W$$

Figure 5. Efficiency vs. Output Current.

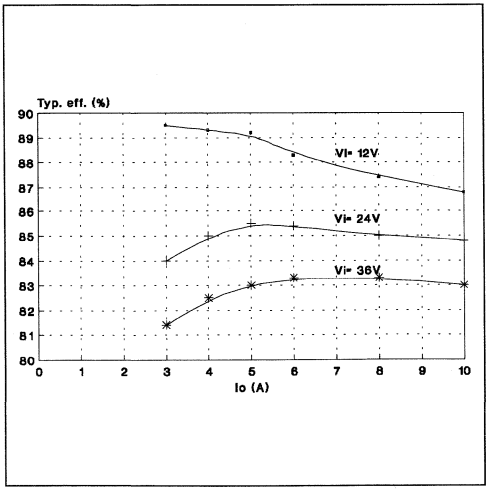
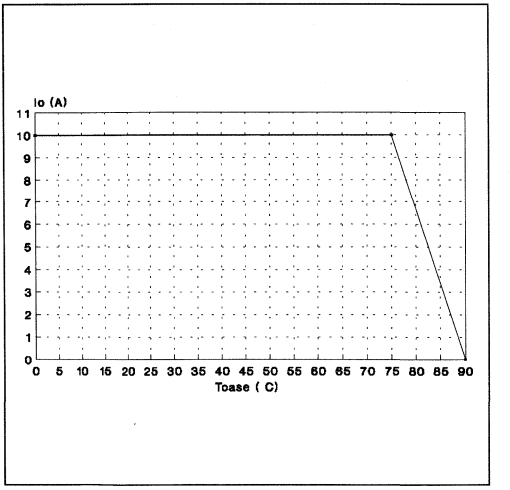


Figure 6. Output Current vs. T case.



The following list may help the designer to select the proper commercially available heat-sink. Sometimes it can be more convenient to use a custom made heat-sink that can be experimently designed and tested.

Manufacturers	Type	Height (mm)	Rth (°C/W)
ALUTRONIC	PR139	20	3
	PR140	19	2
	PR159	20	2.5
ASSMAN	V5440	19	3
	V5805	15	2
	V5280	19	2
AAVID	60885	14	4.5
	60660	25.5	1.5
	62355	33.5	3
AUSTERLITZ	KS50	12	3
	KS100.3	15	2.5
FISCHER	SK16	25.5	1.5
	SK52	19	2
SGE BOSARI	L30	21	3
	LZ50	24	3
THERMALLOY	6155	14	4.5
	6601	14	5
	6176	24	4.5
	6320	30	1.5

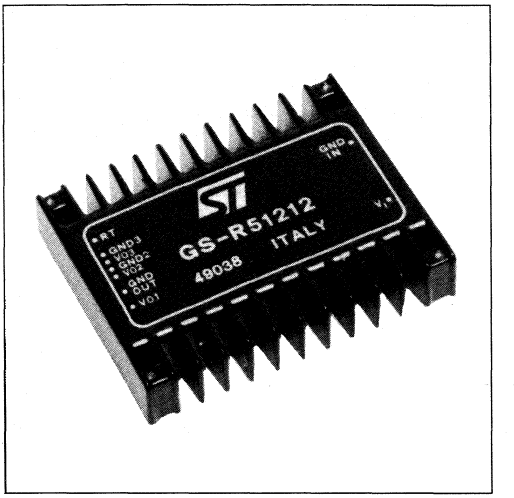
SGS-THOMSON MICROELECTRONICS

GS-R51212

20W TRIPLE OUTPUT STEP-DOWN SWITCHING REGULATOR

FEATURES

- MTBF in excess of 200,000 hours
- 4V max drop-out voltage
- Soft start
- Reset output
- Non-latching short circuit protection
- Crow-bar output overvoltage protection



DESCRIPTION

The GS-R51212 is a versatile triple output, high current, high voltage step-down switching regulator module that provides a +5V and two isolated 12V outputs. It is ideal for microprocessor based boards because it powers the logic and the communication ports and it has a Reset output for the correct system start-up.

The integral heatsink allows a large power handling capability and it provides also an effective shielding to minimize EMI.

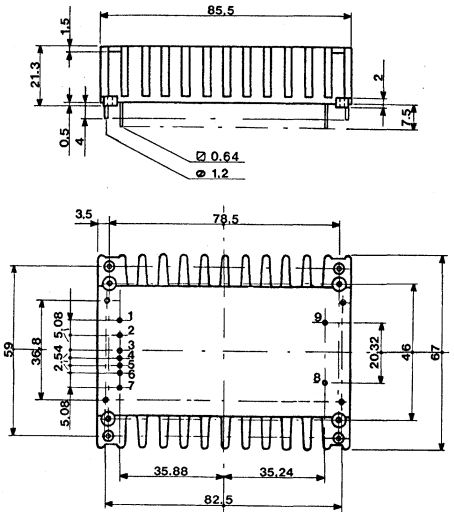
MAIN CHARACTERISTICS

V_i	Input Voltage	9 to 40V
V_{o1} I_{o1}	Output Voltage Output Current	5.1V 3.5A
V_{o2} I_{o2}	Output Voltage Output Current	12V 0.1A
V_{o3} I_{o3}	Output Voltage Output Current	12V 0.1A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	42	V
I_{rt}	Reset Output Sink Current	20	mA
T_{stg}	Storage Temperature Range	–40 to +105	°C
T_{cop}	Operating Case Temperature Range	–20 to +85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm

Bottom view

PIN DESCRIPTION

Pin	Function	Description
1	Output 1	Regulated 5.1V output.
2	Output GND	Return for output1 current path. Internally connected to pin 8.
3	Output 2	Regulated 12V output.
4	Ground 2	Return of output 3 current path.
5	Output 3	Regulated 12V output.
6	Ground 3	Return of output 3 current path.
7	Reset	Open collector Reset output.
8	Input GND	Return of input voltage source. Internally connected to pin 2.
9	+ Input	DC input voltage. Recommended maximum voltage is 40V.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{o1}	Output Voltage	V_i=24V I_{o1}=2.5A	4.95	5.1	5.2	V
V_{o2}	Output Voltage	V_i=24V I_{o2}=0.1A	11.5		12.5	V
V_{o3}	Output Voltage	V_i=24V I_{o3}=0.1A	11.5		12.5	V
$\Delta V_o/\Delta T$	Temperature Stability	All Outputs		0.2		mV/°C
V_i	Input Voltage		9		40	V
I_{o1}	Output Current	V_i=24V	0.5		3.5	A
I_{o2}	Output Current	V_i=24V			0.1	A
I_{o3}	Output Current	V_i=24V			0.1	A
I_{isc}	Average Input Current	V_i=40V V_{o1}=0V		0.1	0.2	A
I_{isc}	Average Input Current	V_i=40V $V_{o1/2/3}$=0V		0.1	0.2	A
I_{ir}	Reflected Input Current	V_i=24V I_{o1}=2.5A $I_{o2,3}$=0.1A		200		mApp
V_{is}	5V to 12V Isolation Voltage		200			Vdc
f_s	Switching Frequency			100		kHz
η	Efficiency	V_i=24V I_{o1}=2.5A $I_{o2,3}$=0.1A		70		%
ΔV_o	Line Regulation	I_{o1}=2.5A V_i=15 to 25V $I_{o2,3}$=0.1A		2		mV/V
ΔV_o	Load Regulation	V_i=24V I_{o1}=0.5 to 2.5A V_i=24V $I_{o2,Io3}$=0.05 to 0.1A		35 600		mV/A
SVR	Supply Voltage Rejection	50/60Hz		4		mV/V
V_r	Ripple Voltage	V_i=24V I_{o1}=2.5A		30		mVpp
V_n	Noise Voltage	V_i=24V I_{o1}=2.5A		40		mVpp
I_{rh}	Reset Leakage Current			100		µA
V_{rl}	Reset Low Level	I_{reset}=5mA		0.2		V
t_{rd}	Reset Delay Time			100		ms
t_{r1}	Line Transient Recovery Time	I_{o1}=2.5A V_i=15 to 35V		500		µs
t_{r2}	Load Transient Recovery Time	V_i=24V I_o=0.5 to 2.5A		200		µs
t_{ss}	Soft Start Time			10		ms
t_{cd}	Crowbar Delay Time			5		µs
V_{cth}	Crowbar Intervention Threshold			6.37		V
R_{th}	Thermal Resistance	Case to ambient		5		°C/W

USER NOTES

Input Voltage

The recommended operating maximum DC input voltage is 40V inclusive of the ripple voltage.

Case Grounding

The module case is internally connected to pin 2 and pin 8.
The PCB area below the module can be used as an effective sixth side shield against EMI.

Thermal Characteristics

The case-to-ambient thermal resistance of the GS-R51212 module is about 5°C/W. This produces a 50°C temperature increase of the module surface for a 10W of internal power dissipation.
Depending on the ambient temperature and/or on the power dissipation, an additional heatsink or forced ventilation may be required.

Input Impedance

The module has an internal capacitor connected between the input pins in order to assure PWM stability. This capacitor cannot handle large values of high frequency ripple current, and it can be permanently damaged if the primary energy source impedance is not adequate.
The use of an external low ESR, high ripple current capacitor located as close to the module as possible is recommended. Suitable units are the SPRAGUE type 672D and 678D, and the RIFA type PEG 126 or any equivalent unit. When space is a limitation, a 22µF ceramic multilayer capacitor must be connected to the module input pins.

Module Protection

The module is protected against occasional and permanent short circuits of the output pins to ground, as well as against output current overload. When the output current at 5V output exceeds the maximum value, the output is automatically disabled. After a fixed time the module starts again in a soft mode. The cycle is repeated until the overload condition is removed.
A crow-bar output overvoltage protection is activated when the output voltage on V_{o1} exceeds 6.37V.

Output Current

The output current of the main output is 3.5A. The max output current of the two 12V outputs is a function of the input voltage and of the main output current as shown in fig. 1.
If the main current is zero, no voltage will be available on the 12V outputs.

Figure 1. Output Current Capability vs. Operating Conditions

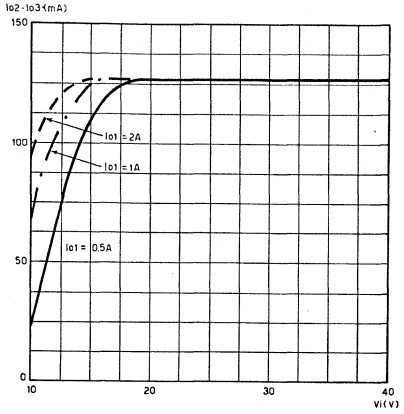


Figure 2. Reset Operation

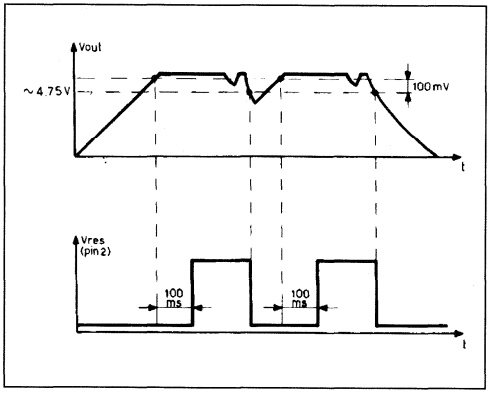
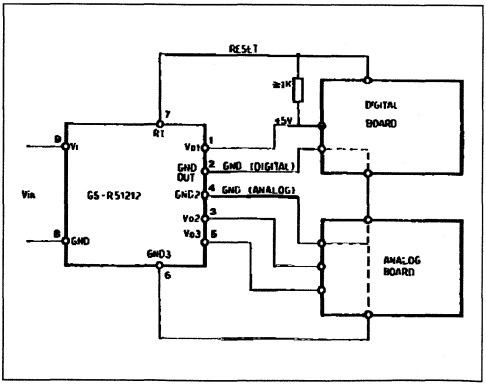


Figure 3. Typical application



SGS-THOMSON MICROELECTRONICS

SGS-THOMSON MICROELECTRONICS

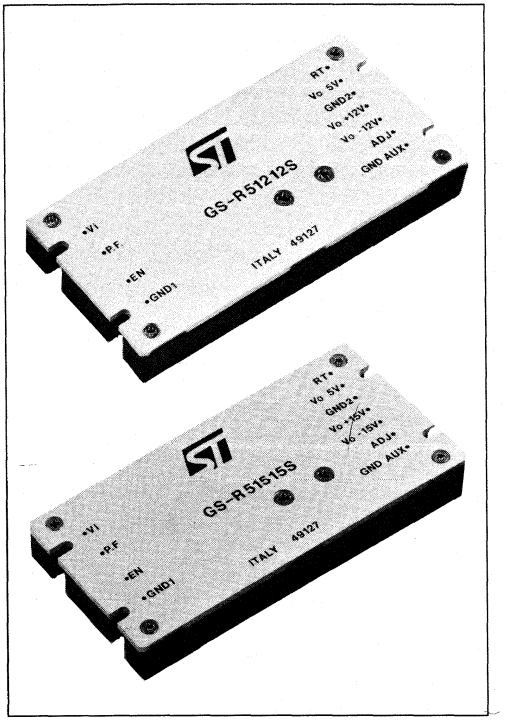
GS-R51212S
GS-R51515S

31W TRIPLE OUTPUT STEP-DOWN SWITCHING REGULATORS

PRELIMINARY

FEATURES

- 5.1V/4.5A and 12V/0.35A or 15V/0.3A output voltages
- 12 or 15V externally adjustable
- High efficiency (81% typ.)
- Short-circuit protection
- Reset output
- Power Fail programmable input
- Inhibit/Enable control input
- Soft-start
- PCB or chassis mounting



DESCRIPTION

The **GS-R51212S** and **GS-R51515S** are versatile triple output, high current step-down switching regulators that provide +5.1V/4.5A output voltage and an isolated 12V/0.35A or 15V/0.3A dual output voltage.

They are ideal for microprocessor based boards because power the logic and the communication ports and have Reset output and Power Fail programmable input for the correct system start-up.

The Inhibit/Enable pin allows the ON/OFF logic function with TTL/CMOS compatible input signal.

The auxiliary outputs (12V or 15V) are externally adjustable in a very wide range, i.e. from 4.25V to 12.45V on **GS-R51212S** and from 4.50V to 15.25V (typical values) on **GS-R51515S**.

SELECTION CHART

Type Ordering Number	Supply Voltage	Output 1	Output 2	Output 3
GS-R51212S	15 to 40V	5.1V/4.5A	+12V/0.35A	-12V/0.35A
GS-R51515S	15 to 40V	5.1V/4.5A	+15V/0.3A	-15V/0.3A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	44	V
I_{rs}	Reset Output Sink Current	20	mA

ELECTRICAL CHARACTERISTICS ($T_{amb.}$ = 25°C unless otherwise specified)

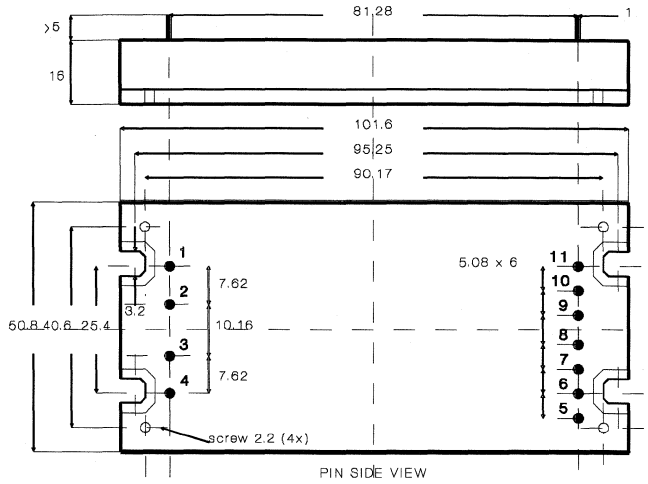
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_i	Input Voltage	V_{o1} = 5.1V V_{o2} = +12 or +15V V_{o3} = -12 or –15v	I_{o1} = 4.5A I_{o2} = 0.35 or 0.3A I_{o3} = 0.35 or 0.3A	15		40	V
I_{ir}	Input Reflected Current	V_i = 24V	$I_{o1,2,3}$ = Full Load		0.5		App
		No external input capacitor					
I_{ir}	Input Reflected Current	V_i = 24V	$I_{o1,2,3}$ = Full Load		0.15		App
		C_i (external)= 100µF/50V					
V_{o1}	Output Voltage 1	V_i = 15 to 40V	I_{o1} = 0 to 4.5A I_{o2} = 0 to 0.35/0.3A I_{o3} = 0 to 0.35/0.3A	5	5.1	5.2	V
V_{o2}	Output Voltage 2	V_i = 15 to 40V	I_{o1} = 0 to 4.5A I_{o2} = 0 to 0.35/0.3A I_{o3} = 0 to 0.35/0.3A	+11.5 or +14.5	+12 or +15	+12.5 or +15.5	V
V_{o3}	Output Voltage 3	V_i = 15 to 40V	I_{o1} = 0 to 4.5A I_{o2} = 0 to 0.35/0.3A I_{o3} = 0 to 0.35/0.3A	–11.5 or 14.5	–12 or –15	–12.5 or –15.5	V
V_{or1}	Output Ripple Voltage 1	V_i = 24V	I_{o1} = 4.5A		30	50	mVpp
$V_{or2,3}$	Output Ripple Voltage 2,3	V_i = 24V	$I_{o2,3}$ = 0.35/0.3A		50	100	mVpp
δV_{o1}	Line Regulation 1	V_i = 15 to 40V	I_{o1} = 2.5A $I_{o2,3}$ = 0.35/0.3A		0.5		mV/V
$\delta V_{o2,3}$	Line Regulation 2,3	V_i = 15 to 40V	I_{o1} = 2.5A $I_{o2,3}$ = 0.35/0.3A		1		mV/V
δV_{o1}	Load Regulation 1	V_i = 24V	I_{o1} = 0.5 to 4.5A $I_{o2,3}$ = 0.35/0.3A		2		mV/A
$\delta V_{o2,3}$	Load Regulation 2,3	V_i = 24V	I_{o1} = 2.5A I_{o2}, I_{o3} = 0.05 to 0.35/0.3A		500		mV/A
I_{o1}	Output Current 1	V_i = 15 to 40V V_{o1} = 5.1V	$I_{o2,3}$ = 0 to 0.35/0.3A	0		4.5	A
I_{o2}	Output Current 2*	V_i = 15 to 40V V_{o2} = +12 or +15V	I_{o1} = 0 to 4.5A I_{o3} = 0 to 0.35/0.3A	0		0.35 or 0.3	A
I_{o2}	Output Current 2*	V_i = 15 to 40V V_{o2} = +12 or +15V	I_{o1} = 0 to 4.5A I_{o3} = 0A	0		0.7 or 0.6	A
I_{o3}	Output Current 3*	V_i = 15 to 40V V_{03} = –12 or –15V	I_{o1} = 0 to 4.5A I_{o2} = 0 to 0.35/0.3A	0		0.35 or 0.3	A
I_{o3}	Output Current 3*	V_i = 15 to 40V V_{o3} = –12 or –15V	I_{o1} = 0 to 4.5A I_{o2} = 0A	0		0.7 or 0.6	A
I_{osck1}	Output Current Limit 1	V_i = 15 to 40V	Overload		5.5		A
I_{osc1}	Output Short-circuit Current 1	V_i = 15 to 40V			3		A

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$I_{osc2,3}$	Output Short-circuit Current 2,3	V_i = 15 to 40V			0.8		A
η	Efficiency	V_i = 24V	$I_{o1,2,3}$ = Full Load	78	81		%
fs	Switching Frequency	V_i = 15 to 40V V_{o1}= 5.1V V_{o2} = +12 or +15V V_{o3} = −12 or −15V	I_{o1} = 0.5 to 4.5A I_{02}, I_{03} = 0.05 to 0.35/0.3A		100		kHz
δ Vpk	Overshoot Peak Voltage	V_i = 15 to 40V	I_{o1} = 1A			250	mV
ts	Settling Time	V_i = 15 to 40V	δI_{o1} = 1A			200	µs
V_{iinh}	Inhibit Input Voltage	V_i = 15 to 40V		1.2		+V_i	V
V_{ien}	Enable Input Voltage	V_i = 15 to 40V		0		0.8	V
I_{ien}	Enable Input Current	V_i = 15 to 40V				−1	mA
tss	Soft-start time				10		ms
tdr	Reset Time Delay				100		ms
Rth	Thermal Resistance				7.5		°C/W
Tstg	Storage Temperature Range			−40		+105	°C
Tcop				0		+85	°C

* **Note:** when output current is less than 50mA, output ripple voltage increases due to discontinuous operation.

CONNECTION DIAGRAM AND MECHANICAL DATA



Dimensions in mm

PIN DESCRIPTION

Pin	Function	Description
1	**GND IN**	Return for input voltage source. Internally connected to pin 7.
2	**EN.**	Inhibit/Enable control input.
3	**P.F.**	Power Fail programmable input. If unconnected the Power Fail threshold voltage is 11V with 1V hysteresis (factory setting).
4	**+ Vin**	DC input voltage. Recommended maximum voltage is 40V.
5	**RT**	Reset output (active high). When the supply voltage +Vin and the regulated output voltage +Vo1 are in the correct range this signal is generated after a delay time of 100ms typical.
6	**Vo +5V**	Regulated +5.1V output voltage.
7	**GND 1**	Return for output 1 current path. Internally connected to pin 1.
8	**Vo +12/15V**	Regulated +12 or +15V output.
9	**Vo -12/15V**	Regulated –12 or –15V output.
10	**ADJ.**	External adjustement for output voltages ±12 and ±15V.
11	**GND Aux.**	Return for ±12 and ±15V output current path.

USER NOTES

Input Voltage

The recommended operating maximum DC input voltage is 40V inclusive of the ripple voltage. The use of an external low ESR, high ripple current capacitor located as close the module as possible is recommended; suggested value is 100µF/50V.

Soft-start

To avoid heavy inrush current the output voltage rise time is typically 10ms in any condition of load.

Power Fail - Reset Circuit

The module include a voltage sensing circuit that may be used to generated a power-on/power-off reset signal for a microprocessor system.

The circuit senses the input supply voltage and the output generated voltage Vo +5V and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation.

When both the supply voltage and the regulated voltage are in the correct range the output Reset signal is generated after a delay time t_{DR} of 100ms typical.

A latch assures that if a spike is present on the sensed voltage the delay time circuit discharges completely before inizialization of a new reset cycle.

Reset output has internal pull-up resistor of 10kΩ connected to Vo +5V pin. Maximum sink output current is 20mA at V_{RESET}(sat)= 200mV.

Fig.1 and fig.2 show reset waveforms.

Power Fail Programmable Input

This pin is internally connected via a divider to the +Vin pin for Power Fail function.

The factory setting is for a value of 11V with 1V hysteresis.

It is possible to program a different value of Power Fail threshold by connecting a resistor (Rpf) between pin 2 (Power Fail Input) and pin 1 (GND Input). The value of Rpf must be calculated according to the following formula:

$$Rpf = \frac{5.1}{\frac{Vpf-5.1}{34} - 0.191} = (k\,\Omega)$$

where Vpf is the desired value of Power Fail threshold voltage.

Example: Vpf= 24V (must not be lower than 12V):

$$Rpf = \frac{5.1}{\frac{24-5.1}{34} - 0.191} = 14k\,\Omega$$

Figure 1. Reset and Power Fail waveforms.

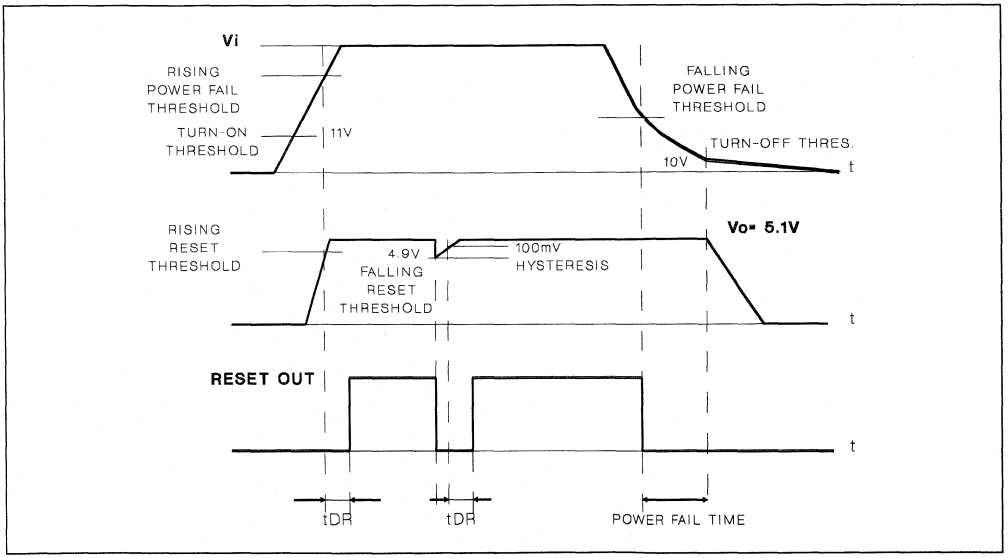
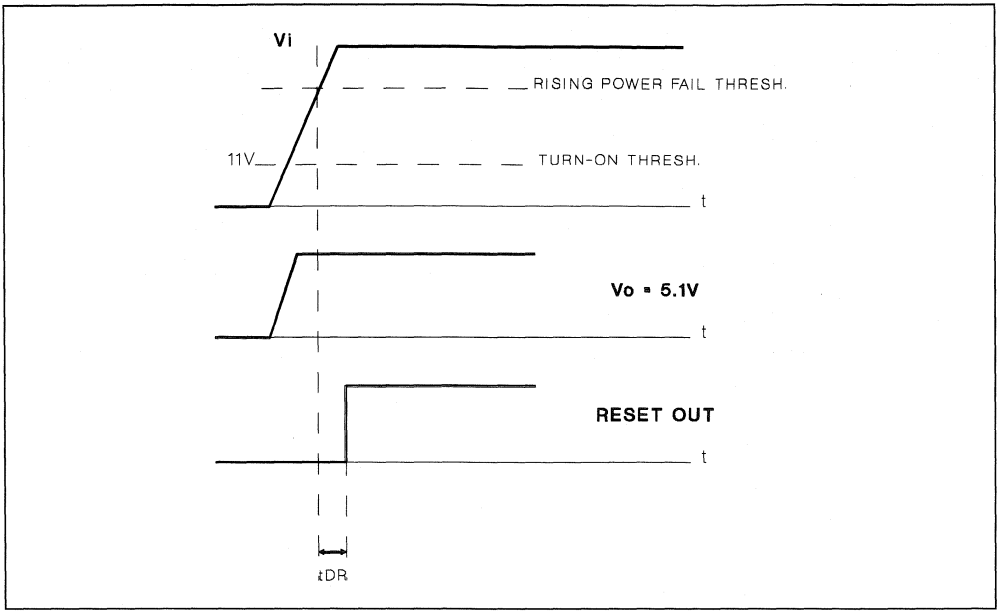


Figure 2. Reset and Power Fail waveforms



Auxiliary Outputs

The auxiliary outputs (12V or 15V) are externally adjustable in symmetric way by connecting a resistor Ra between pin 10 (ADJ.) and pin 8 (Vo 12/15V), according to the following formula:

GS-R51212S $Ra = 32.66 \times \frac{Vo - 4.229}{12.485 - Vo}$

GS-R51515S $Ra = 38.66 \times \frac{Vo - 4.39}{15.252 - Vo}$

where Vo is the desired dual output voltage.

Example: Vo= ±5V.

Ra (GS-R51212S) = 3.36kΩ

Ra (GS-R51515S) = 2.3kΩ

Example: Vo= ±10V.

Ra (GS-R51212S) = 75.8kΩ

Ra (GS-R51515S) = 41.3kΩ

Inhibit/Enable Input

The Inhibit/Enable function allows the ON/OFF logic control of the module.

The converter is ON (Enable) when the voltage applied to pin 2 (EN.) and referred to pin 1 (GND IN) is lower than 0.8V (TTL, CMOS, open collector compatible level). The converter is OFF (Inhibit) when pin 2 is unconnected or the voltage applied is in the range of 1.2V to +Vin. Maximum sinking current is 1mA.

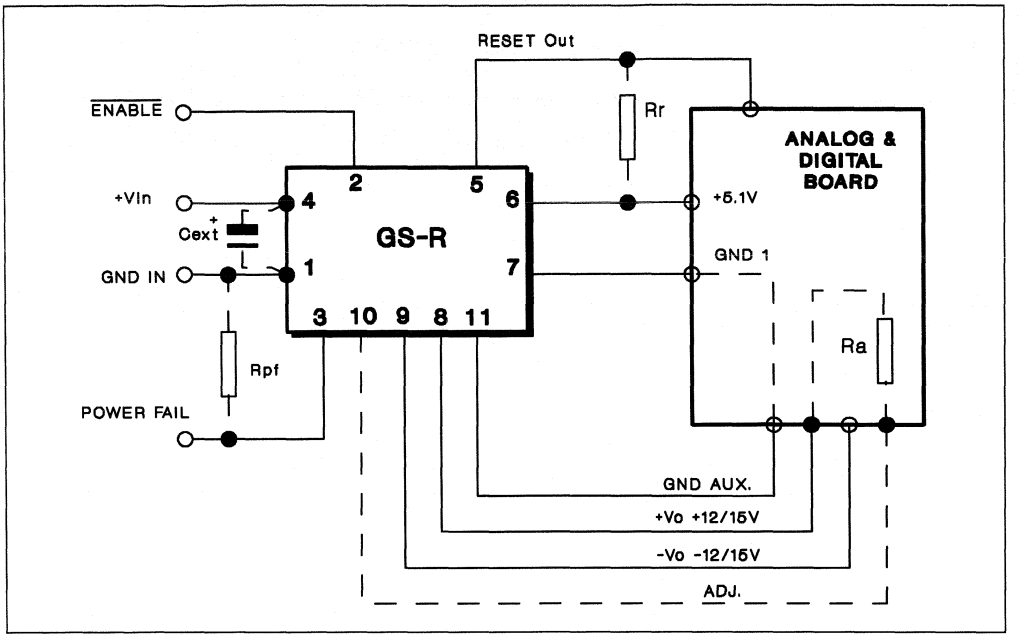
Module Protection

The module is protected against occasional and permanent short-circuits of the output pins to ground, as well as against output current overload.

The main output (+5.1V) uses a foldback current limiting; the output current decreases with increasing overload, reaching a minimum at short-circuit condition. This solution minimizes internal power dissipation.

The auxiliary outputs (±12V or ±15V) use a current limiting protection circuitry.

Figure 3. Typical Application



Thermal characteristics

Sometimes the **GS-R51212S** and **GS-R51515S** require an external heat-sink depending on both operating temperature conditions and power.

Before entering into calculations details, some basic concepts will be explained to better understand the problem.

The thermal resistance between two points is represented by their temperature difference in front of a specified dissipated power, and it is expressed in Degree Centigrade per Watt (C/W).

For the modules the thermal resistance case to ambient is 7.5°C/W. This means that an internal power dissipation of 1W will bring the case temperature at 7.5°C above the ambient temperature.

The maximum case temperature is 85°C.

Let's suppose to have a GS-R51515S that delivers the maximum output power of 31.4W at an ambient temperature of 40°C.

The dissipated power in this operating condition is about 7.4W (at typical efficiency of 81%), and the case temperature of the module will be:

$T_{case} = T_{amb} + Pd \times Rth = 40+7.4x7.5 = 95.5°C$

This value exceeds the maximum allowed temperature and an external heat-sink must be added. To this purpose four holes (see mechanical drawing) are provided on the metal surface of the module.

To calculate this heat-sink, let's first determine what the total thermal resistance should be.

$$Rth = \frac{T_{case}\,(max) - Tsubamb}{Pd} = \frac{85-40}{7.4} = 5.40 \pm C/W$$

This value is the resulting value of the parallel connection of GS-R thermal resistance and of the additional heatsink thermal resistance.

$$\frac{Rth\,(GSR) \times Rth\,(Heatsink)}{Rth\,(GSR) + Rth\,(Heatsink)} = 5.40\,°\,C/W$$

To calculate the thermal resistance of the additional heat-sink the following equation may be used:

$$Rth\,(Heatsink) = \frac{5.40 \times Rth\,(GSR)}{Rth\,(GSR) - 5.40} = \frac{5.40 \times 7.50}{7.5 - 5.40}\ 19.3\ °C/W$$

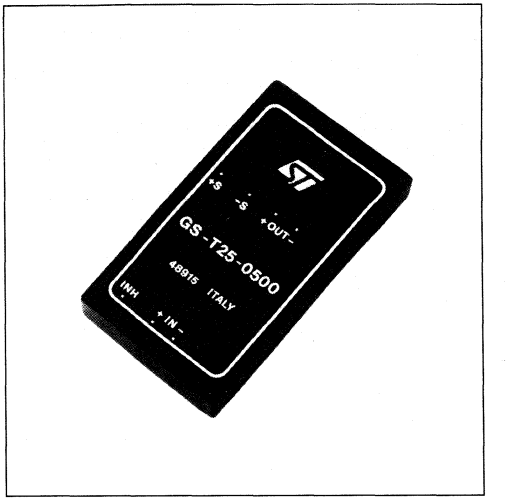
In turn of or in addition to the external heatsink, a forced ventilation with an air speed of about 200 linear feet/minute can be used reducing the thermal resistance of the module at the specified value.

SGS-THOMSON MICROELECTRONICS

GS-T25/30 FAMILY

25-30 WATT DC-DC CONVERTERS

- MTBF IN EXCESS OF 1M HOURS AT + 45°C AMBIENT TEMPERATURE
- PCB OR CHASSIS MOUNTABLE
- NO EXTERNAL COMPONENT REQUIRED
- SIX SIDED CASE
- HIGH EFFICIENCY (see data)
- 500 V_{DC} MINIMUM ISOLATION
- WIDE INPUT VOLTAGE RANGE (36 to 72V)
- REVERSE INPUT POLARITY PROTECTION
- PEAK INPUT OVERVOLTAGE WITHSTAND (90V/1 sec.)
- MINIMIZED INPUT REFLECTED CURRENT
- SOFT START
- REMOTE INHIBIT/ENABLE WITH LOW STAND BY CURRENT
- REMOTE OUTPUT VOLTAGE SENSE
- NON LATCHING PERMANENT SHORT CIRCUIT PROTECTION
- LATCHING OUTPUT OVERVOLTAGE PROTECTION
- REDUNDANT OPERATION
- NO DERATING OVER THE TEMPERATURE RANGE



DESCRIPTION

The GS-T25/30 series is a family of isolated DC-DC converters specially designed for Telecom application, available in different output voltages : 5V ; 6V; 12V and 15V. (OTHER OUTPUT VOLTAGES available on request).

The output power is in the range of 25W to 30W.

To ensure very long life, these converters don't use any electrolytic capacitor or optoelectronic feedback system.

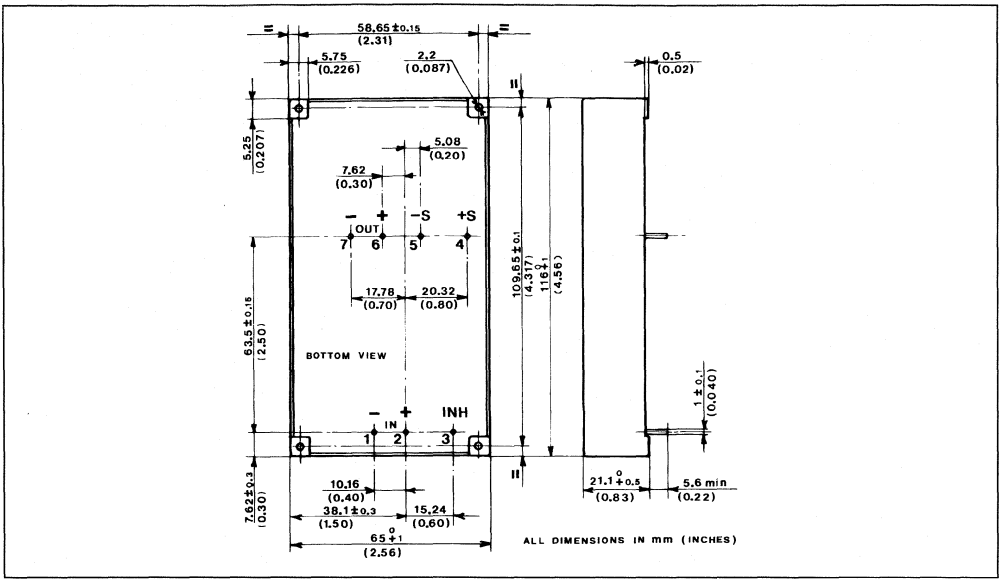
PRODUCTS FAMILY

Order Number	Output Voltage	Output Current	Output Power
GS-T25-0500	5V	5A	25W
GS-T27-0600	6V	4.5A	27W
GS-T30-1200	12V	2.5A	30W
GS-T30-1500	15V	2A	30W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	34 to 72	V
V_{ipk}	Input Transient Overvoltage (T ≤ 1sec.)	90	V
V_{ir}	Input Reverse Voltage	100	V
T_{stg}	Storage Temperature Range	– 55 to 105	°C
T_{op}	Operating Temperature Range	– 25 to 71	°C

CONNECTION DIAGRAM AND MECHANICAL DATA (bottom view)



PIN FUNCTIONS

Pin	Function
1	– Input.
2	+ Input. Unregulated input voltage (typically 48V) must be applied between pin 1-2. The input section of the DC-DC converter is protected against reverse polarity by a series diode. No external fuse is required. Input is filtered by a Pi network.
3	Remote inhibit/enable logically compatible with CMOS or open collector TTL. The converter is ON when the voltage applied to pin 3 is $1.8V_{DC}$ min or left open referenced to the pin 1. The converter is OFF for a control voltage lower than $1.2V_{DC}$.
4	Sensing Positive. For connection to remote loads this pin allows voltage sensing to the load itself. TO BE CONNECTED TO PIN 6 WHEN REMOTE SENSING IS NOT USED.
5	Sensing Negative. See pin 4. TO BE CONNECTED TO PIN 7 WHEN REMOTE SENSING IS NOT USED.
6	+ Output.
7	– Output.

ELECTRICAL CHARACTERISTICS (Tamb = 25°C unless otherwise specified)

INPUT

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max	
V_i	Input Voltage	Full Load	36	48	72	36	48	72	36	48	72	36	48	72	V
I_i	No Load Input Current	V_{IN} = 48V		15			15			15			20		mA
I_i	Full Load Input Current	V_{IN} = 48V		640			680			730			730		mA
I_{ir}	Input Reflected Current (sinusoidal)	V_{IN} = 48V/full Load		50			50			50			50		mApp
I_i	Input Short Circuit Current	V_{IN} = 48V		710			760			820			820		mA
I_{isb}	Input Stand by Current	V_{IN} = 48V V_3 = 0V		5			5			5			5		mA
V_{INHL}	Low Inhibit Voltage	V_{IN} = 48V, Full Load			1.2			1.2			1.2			1.2	V
V_{INHH}	High Enable Voltage	V_{IN} = 48V, Full Load	1.8 or open			1.8 or open			1.8 or open			1.8 or open			V
I_{INH}	Input Inhibit Current	V_{IN} = 48V, Full Load		1.8			1.8			1.8			1.8		mA

OUTPUT

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage	V_{IN} = 48V Full Load	4.95	5.00	5.05	5.94	6.00	6.06	11.88	12.00	12.12	14.85	15.00	15.15	V
ΔV_O	Line Regulation	V_{IN} = 36V to 72V Full Load		± 0.001			± 0.001			± 0.001			± 0.001		%
ΔV_O	Load Regulation	V_{IN} = 48V Full Load to no Load		± 0.05			± 0.05			± 0.05			± 0.05		%
V_r	Ripple and Noise Voltage	V_{IN} = 48V Full Load		5			5			5			5		mVRMS
$V_{O\,OV}$	Output Overvoltage Protection	V_{IN} = 48V Full Load			6.8			8.2			15			18	V
ΔV_O	Remote Sense per Leg	V_{IN} = 36V			0.6			0.6			0.6			0.6	V
t_{ss}	Soft Start Time	V_{IN} = 48V Full Load		30			30			30			30		ms
I_o	Max Output Current	V_{IN} = 48V			5			4.5			2.5			2	A
I_{osc}	Output Average Short Circuit Current	V_{IN} = 48V,		5.5			4.95			2.75			2.2		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT (continued)

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{rt}	Transient Recovery Time	V_{IN} = 48V ΔI_o = 25% Step Load Change		75			75			75			75		µs
T_c	Temperature Coefficient	V_{IN} = 48V, Full Load ; Operating Temperature Range		+ 0.02			+ 0.02			+ 0.02			+ 0.02		%/°C

GENERAL

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max	
η	Efficiency	V_{IN} = 36 to 72V Full Load		81			82			86			86		%
P_d	Power Dissipation in Short Circuit Condition	V_{IN} = 48V		1.06			1.15			2.06			2.6		W
V_{IS}	Isolation Voltage			500			500			500			500		V_{DC}
R_{IS}	Isolation Resistance			10^9			10^9			10^9			10^9		Ω
f_s	Switching Frequency	V_{IN} = 48V Full Load		150			150			150			150		kHz

The GS-T25/30 series of DC-DC converter has been designed to meet the demanding application of the Telecommunication industry.

Particular attention has been devoted to maximize the reliability of the converters as described in the following.

SYSTEM ARCHITECTURE

The switching push-pull current mode architecture has been adopted because :

- it allows large duty cycle (80%) so lowering the input peak current ;
- it minimizes the transformer flux imbalance (current mode cycle by cycle control) :
- it allows, because of its symmetry and together with a switching frequency of 150kHz, to minimize the inductance and capacitance values ;
- it offers exceptional performance in terms of line regulation because of the feedforward effect inherent to current mode control.

COMPONENT CHOICE

Because of the system architecture, ceramic or solid tantalum capacitors only are used.

In addition, the voltage regulation loop is closed by sensing directly the output voltage on the secondary side without any optocoupler feedback device.

Power MOS transistors with a current capability 30 times larger than maximum operating condition have been adopted as primary side switches ; voltage capability is 2.5 times higher than nominal condition.

Efficiency is maximized by lowering switching and conduction losses on the primary side and rectification losses on the secondary side by use of Schottky diodes on the GS-T25/27 models.

PACKAGE

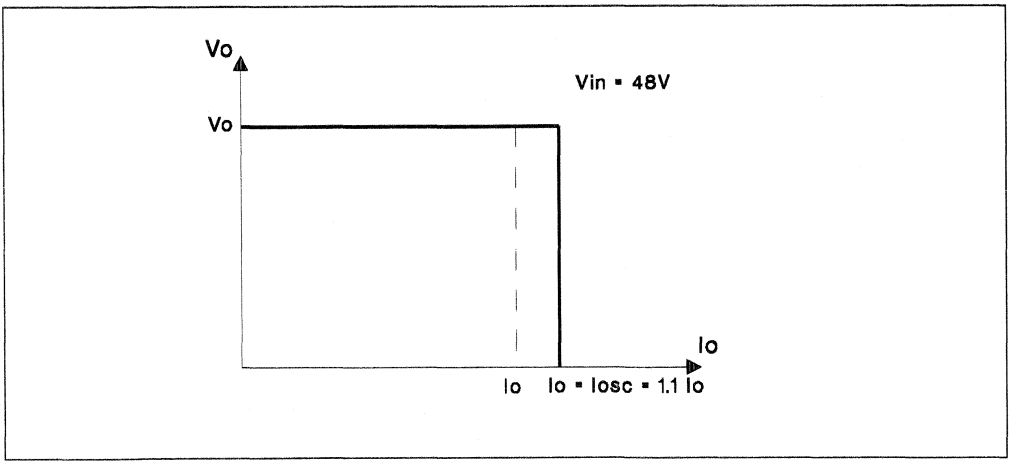
The package is of die casted aluminum type that offers a typical thermal resistance case to ambient of 4°C/W.

This, together with the low power dissipation, allows to keep junction temperature of silicon devices at less than 100°C even for ambient temperature of 71°C with free air convection.

OVERLOAD PROTECTION

The typical diagram of this protection is shown in fig. 1.

Figure 1 : Typical Overload Protection.



During short circuit, current stres on primary side is actually lower than in nominal condition.

Power dissipation inside the module is minimized.

OVERVOLTAGE PROTECTION

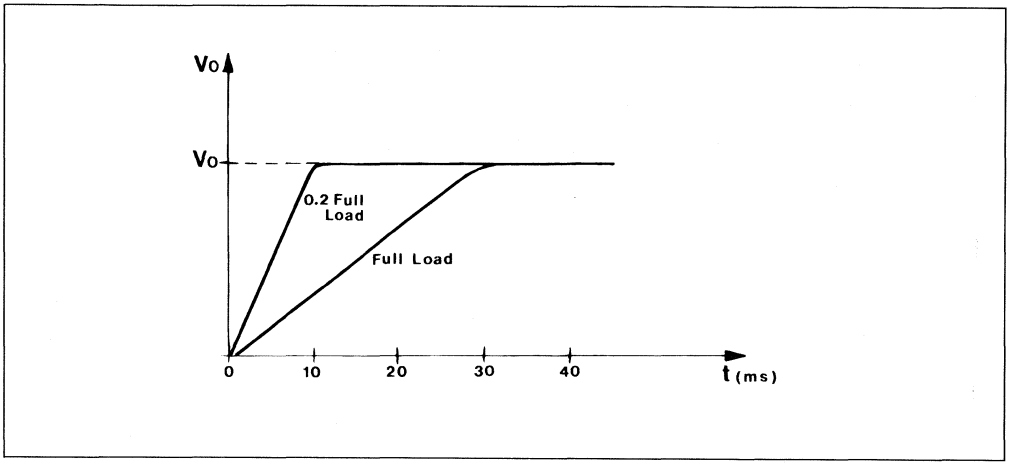
In case of output voltage higher than overvoltage limits, the DC-DC converter is shut down and it remains in a latching condition.

Current drain at the input is 20mA typically, so that this latching condition is not hazardous for the whole equipment where the DC-DC converter is used.

SOFT START

To avoid heavy inrush current the output voltage rise time is controlled as a function of the load condition : the larger the output current, the softer the output voltage rise. See fig. 2.

Figure 2 : Soft Start as a Function of the Output Current.



EFFICIENCY

The efficiency of these DC-DC converters is shown in fig. 3, 4, 5 and 6.

Figure 3.

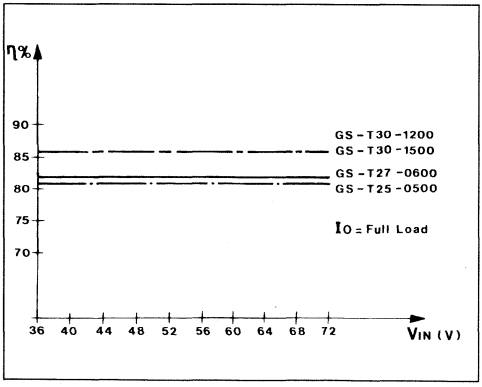
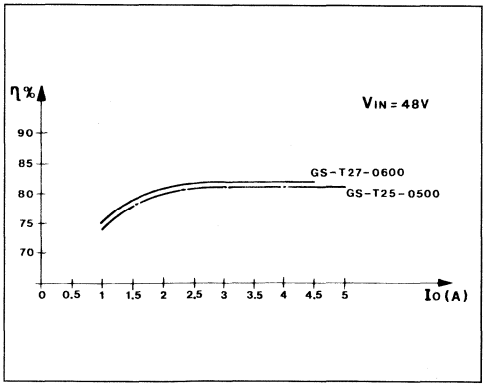


Figure 4.



SGS-THOMSON MICROELECTRONICS

Figure 5.

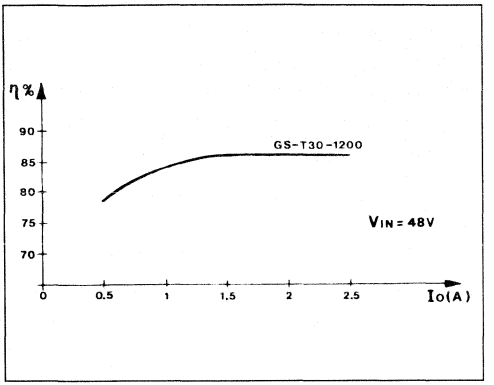
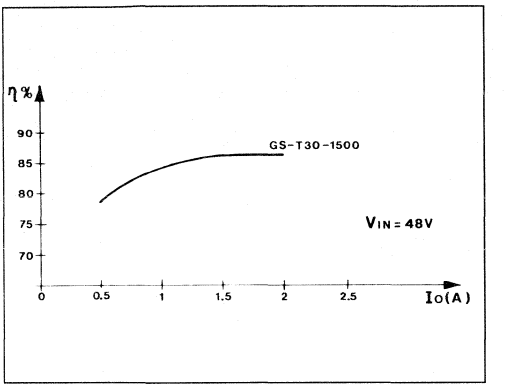


Figure 6.



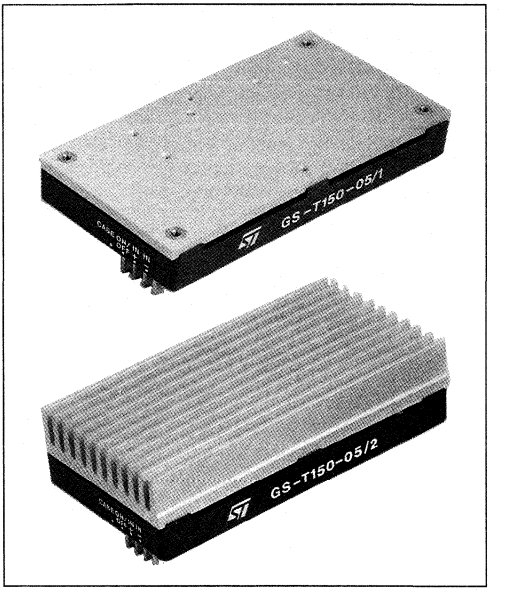
SGS-THOMSON MICROELECTRONICS

GS-T150-05

150W DC-DC CONVERTER

FEATURES

- High output power (150W)
- High efficiency (80% min.)
- Parallel operation with current sharing
- Synchronization
- Remote ON/OFF
- Remote load voltage sense
- Output short-circuit protection
- Undervoltage lock-out
- Minimal overshoot during load transients
- Output overvoltage protection
- Input to output isolation
- Internal input and output filtering
- Softstart
- Low profile
- Two packaging options
- PCB or chassis mountable



DESCRIPTION

The **GS-T150-05** is a 150W DC-DC converter used to generate a 5.075V isolated output with a current of 30A from a wide range input voltage (38 to 60V).

PACKAGING OPTIONS

Ordering Number	Description	Dimensions (mm)
GS-T150-05/1	GS-T150-05 with flat heatsink (see fig.1)	125 x 66.5 x 19
GS-T150-05/2	GS-T150-05 with integral finned heatsink (see fig.2)	125 x 66.5 x 34

ELECTRICAL CHARACTERISTICS (Tamb.= 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 5.075V I_o = 0 to 30A	38	48	60	Vdc
V_{iuv}	Input Undervoltage Lock-out	V_o = 5.075V I_o = 0 to 30A	32	34	36	Vdc
I_i	Input Current	V_i = 48V I_o = 30A		3.85	3.9	Adc
I_{iq}	Input Quiescent Current	V_i = 38V V_i = 60V I_o = 0A I_o = 0A			40 45	mAdc
I_{irush}	Peak Inrush Current	V_i = 60V I_o = 30A Unit off			0.2	A^2s
I_{ir}	Reflected Input Current	V_i = 38 to 60V I_o = 30A with 220µF/30µH external filter		15	30	mApp
I_{ir}	Reflected Input Current	V_i = 48V I_o = 30A without external filter			300	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_o = 0 to 30A	0		1.2	V
V_{iinh}	Max Inhibit Voltage	V_i = 38 to 60V I_o = 0 to 30A V_{ien} = open	8		18	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_o = 0 to 30 A V_{ien} = 0V			-1	mA
V_o	Output Voltage	V_i = 38 to 60V I_o = 0 to 30A	4.90	5.075	5.25	V
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_o = 30A		15	30	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_o = 30A		30	50	mVpp
V_{oov}	Output Overvoltage Protection	V_i = 48V I_o = 0 to 30A	5.80	6.2	6.60	Vdc
δV_o	Line Regulation	V_i = 38 to 60V I_o = 30A			5	mV
δV_o	Load Regulation	V_i = 48V I_o = 0 to 30A			20	mV
δV_o	Remote Sense Compensation	V_i = 48V I_o = 30A			0.5	V
δV_o	Peak Load Transient Response	V_i = 48V δI_o = 5A slope = 0.5A/µs			120	mVp
t_s	Load Transient Settling Time	V_i = 48V δI_o = 5A slope = 0.5A/µs			50	µs
I_o	Output Current	V_i = 38 to 60V	0		30	Adc
I_{ol}	Output Current Limiting	V_i = 38 to 60V	31		34	Adc
I_{osc}	Short-circuit Output Current	V_i = 48V			49	Adc
δI_o	Current Sharing Deviation	V_i = 48V I_o = 3 to 30A two modules in parallel			10	%
η	Efficiency	V_i = 38 to 60V I_o = 30A	80	82		%
f_s	Switching Frequency	V_i = 38 to 60V I_o = 0.5 to 30A		200		kHz
V_{is}	Isolation Voltage		500			V
t_{on}	Turn-on Time	V_i = 0 to 48V I_o = 30A V_{ien} = 0V			10	ms
t_{on}	Turn-on Time	V_i = 48V I_o = 30A V_{ien} = from high to low			5	ms
R_{th}	Thermal Resistance	GS-T150-05/1 Flat Heatsink		5.2		°C/W
R_{th}	Thermal Resistance	GS-T150-05/2 Finned Heatsink		2.8		°C/W
T_{stg}	Storage Temperature Range		-40		+105	°C
T_{cop}	Operating Case Temperature Range		0		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA

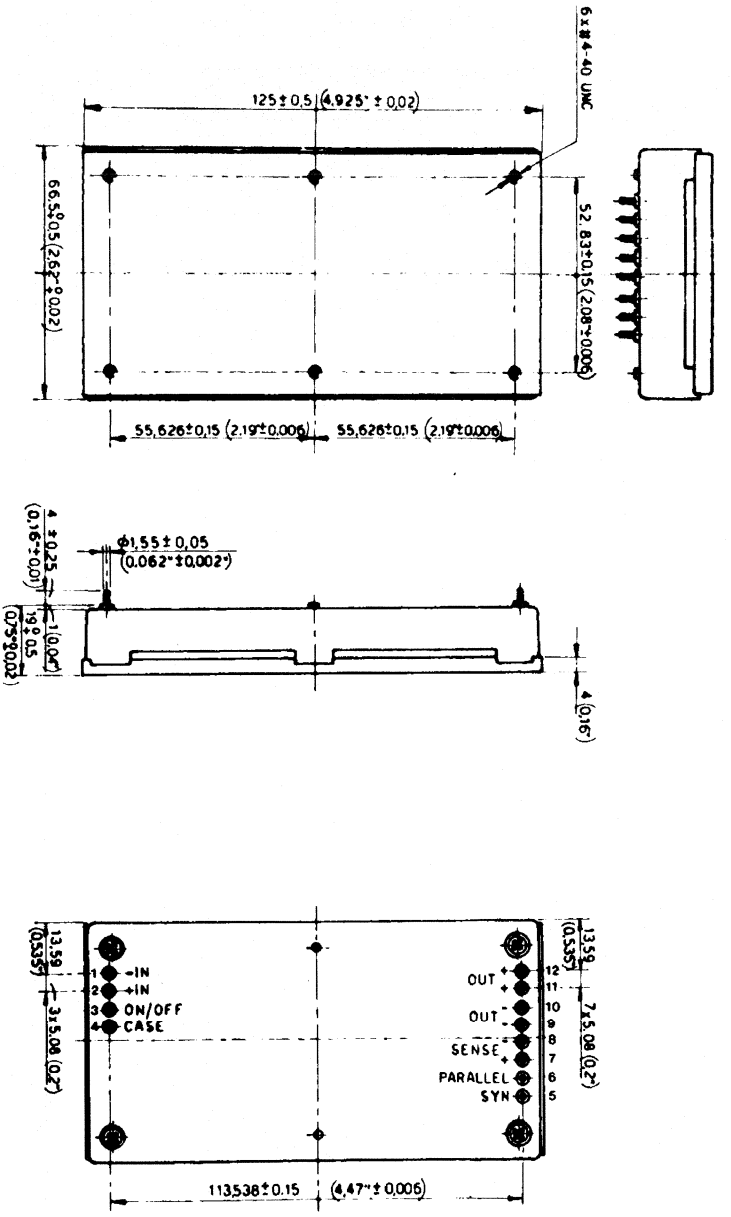
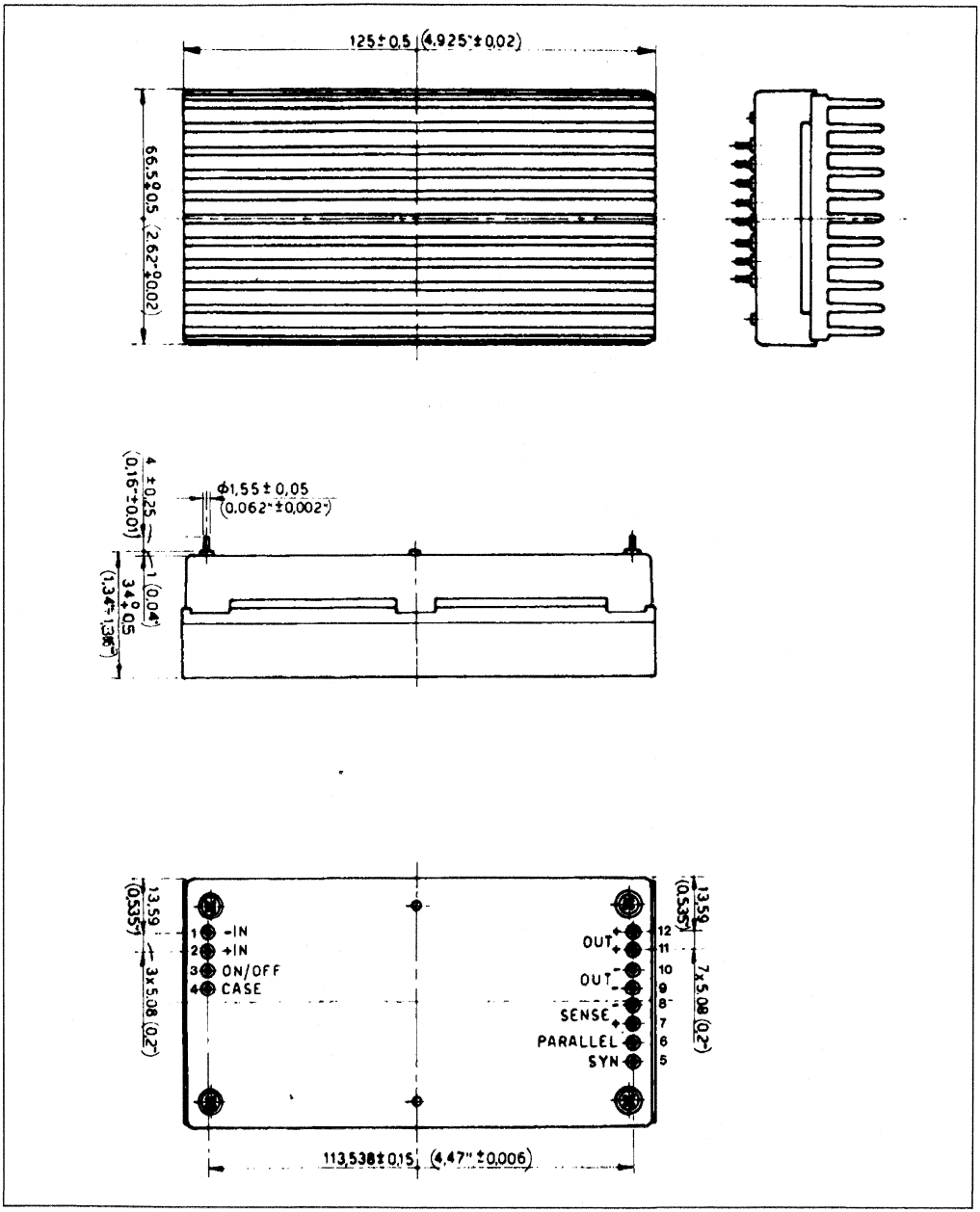


Figure 1. - GS-T150-05/1 with flat heatsink.

Figure 2. - GS-T150-05/2 with integral finned heatsink.



PIN DESCRIPTION

Pin	Function	Description
1	- **IN**	Negative input voltage.
2	+ **IN**	Positive input voltage. Unregulated input voltage (typically 48V) must be applied between pin 1-2.
3	**ON/OFF**	The converter is ON (Enable) when the voltage applied to this pin with reference to pin 1 is lower than 1.2V (see Vien). The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V. When the pin is unconnected the converter is OFF (Inhibit).
4	**CASE**	Case connection pin.
5	**SYNC**	Synchronization output. See figures 3,4,5,6. Open when not used.
6	**PARALLEL**	Parallel output. See figures 3,4,5,6. Open when not used.
7	+ **SENSE**	Senses the remote load high side. To be connected to pin 11,12 when remote sense is not used.
8	- **SENSE**	Senses the remote load return. To be connected to pin 9,10 when remote sense is not used. In parallel configuration
9,10	- **OUT**	+5V output voltage return.
11,12	+ **OUT**	+5V output voltage.

USER NOTES

Remote ON/OFF

The module is controlled by the voltage applied between the ON/OFF pin and -IN pin. The converter is ON (Enable) when the voltage applied is lower than 1.2V (see Vien on ELECTRICAL CHARACTERISTICS). The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V (see Viinh). When the pin is unconnected the converter is OFF. Maximum sinking current is 1mA.

Softstart

To avoid heavy inrush current the output voltage rise time is typically 10ms in any condition of load.

Remote Sensing

The remote voltage sense compensation range is for a total drop of 500mV equally shared between the load connecting wires.
It is a good practice to shield the sensing wires to avoid oscillations. See the connection diagram on figures 3,4,5,6.

Parallel Operation

To increase available output regulated power, the module features the parallel connection possibility with equal current sharing and maximum deviation of 10% (two modules in parallel). See the connection diagram on figures 3,4,5,6.

Figure 3.

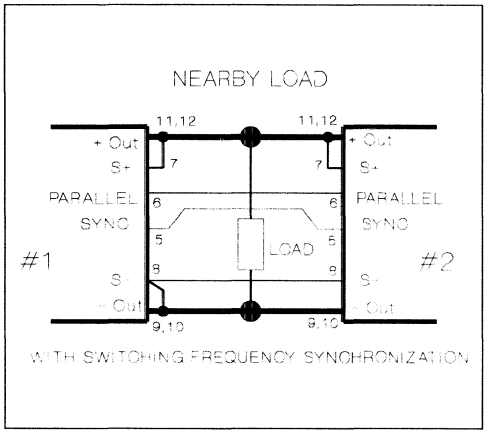


Figure 4.

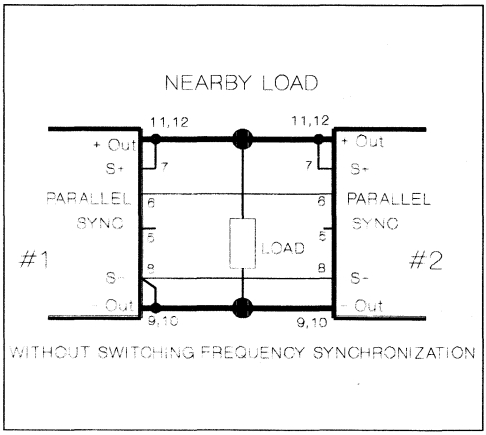


Figure 5

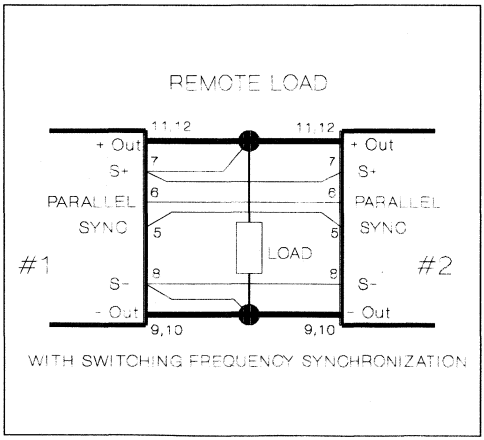
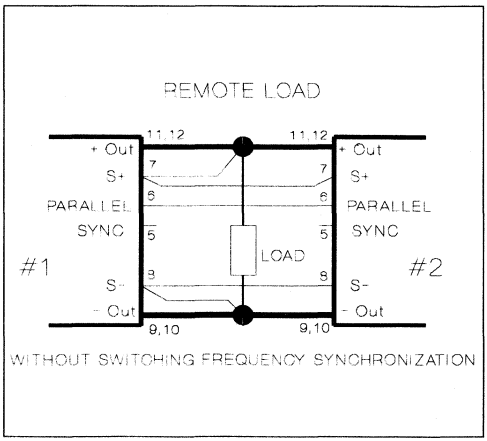


Figure 6



Thermal Characteristics

Two packaging options are available to allow the User the proper thermal management. Following figures nr.7 and nr.8 show the behaviour at still air and forced ventilation operation.

In GS-T150-05/1, the convection cooling can be improved by mounting an external heatsink to the top of the unit. Six threaded holes (# 4-40UNC),5mm (0.2") maximum deep, are provided for this purpose (see fig.1).

Module Protection

The module is protected against occasional and permanent shortcircuits of the output pins to ground, as well as against output current overload. It uses a current limiting protection circuitry, avoiding latch-up problems with certain type of loads.

A crowbar output overvoltage protection is activated when the output voltage exceeds 6.2V typical.

Figure 7. - GS-T150-05/1 with flat heatsink.

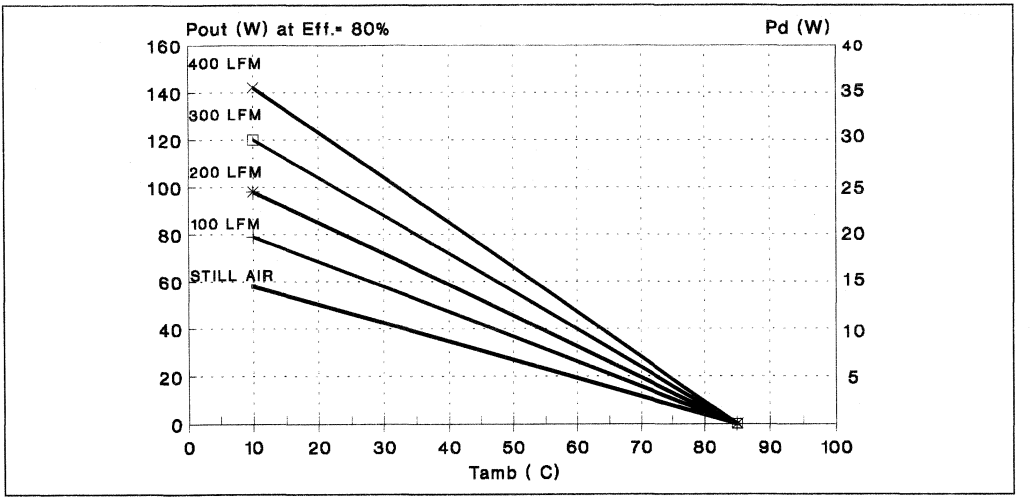
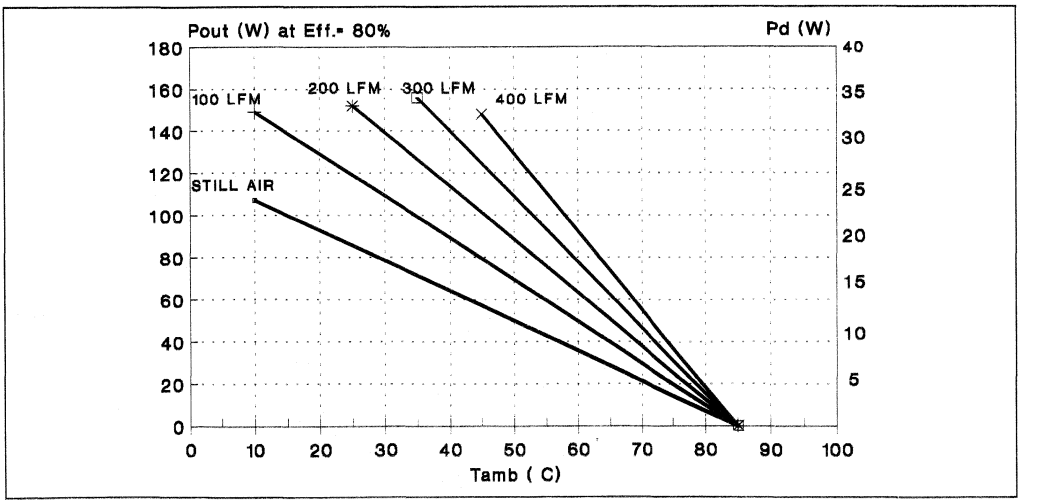
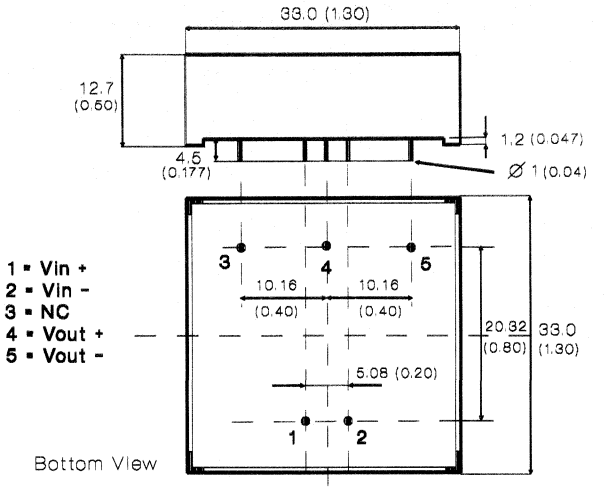


Figure 8 - GS-T150-05/2 with finned heatsink.

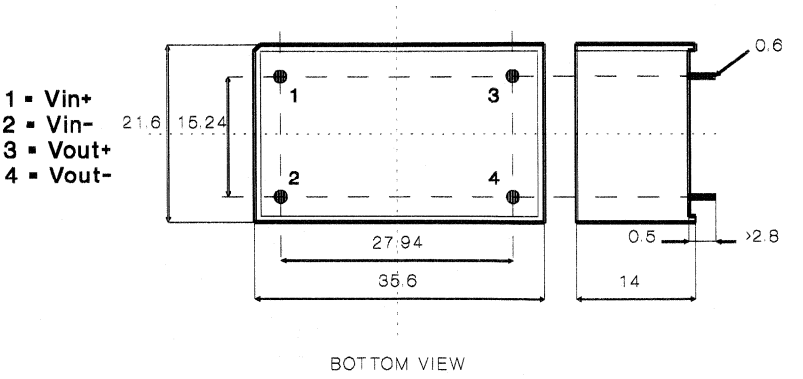


PACKAGES
SUBSYSTEMS MODULES and BOARDS

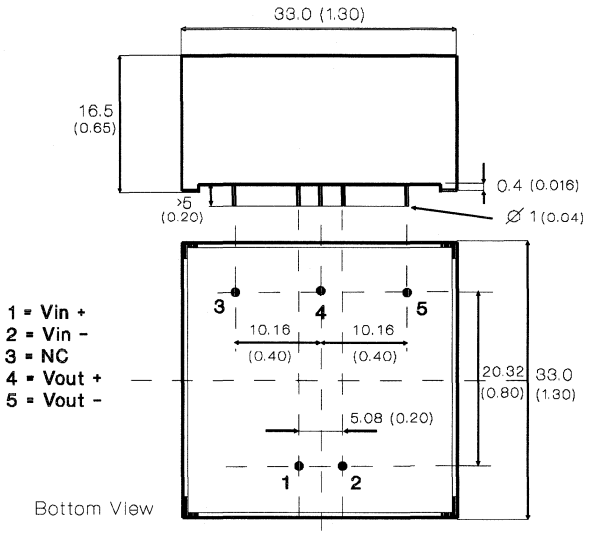
A


33.0 (1.30)
12.7
(0.50)
1.2 (0.047)
4.5
(0.177)
Ø 1 (0.04)
1 = Vin +
2 = Vin -
3 = NC
4 = Vout +
5 = Vout -
3
4
5
10.16
(0.40)
10.16
(0.40)
20.32
(0.80)
33.0
(1.30)
5.08 (0.20)
1
2
Bottom View

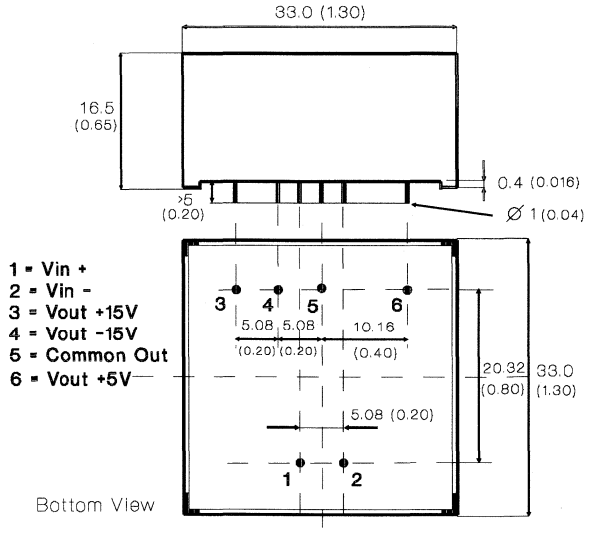
B


1 = Vin+
2 = Vin-
3 = Vout+
4 = Vout-
21.6
15.24
1
3
2
4
0.6
27.94
35.6
0.5
>2.8
14
BOTTOM VIEW

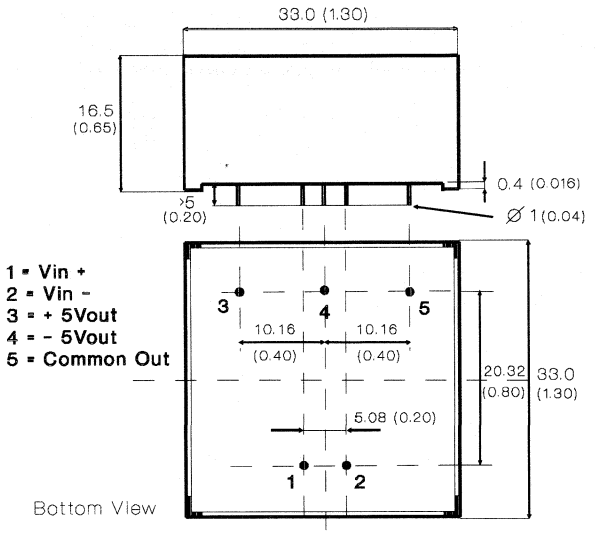
C


33.0 (1.30)
16.5
(0.65)
0.4 (0.016)
>5
(0.20)
Ø 1 (0.04)
1 = Vin +
2 = Vin -
3 = NC
4 = Vout +
5 = Vout -
3
4
5
10.16
(0.40)
10.16
(0.40)
20.32
(0.80)
33.0
(1.30)
5.08 (0.20)
1
2
Bottom View

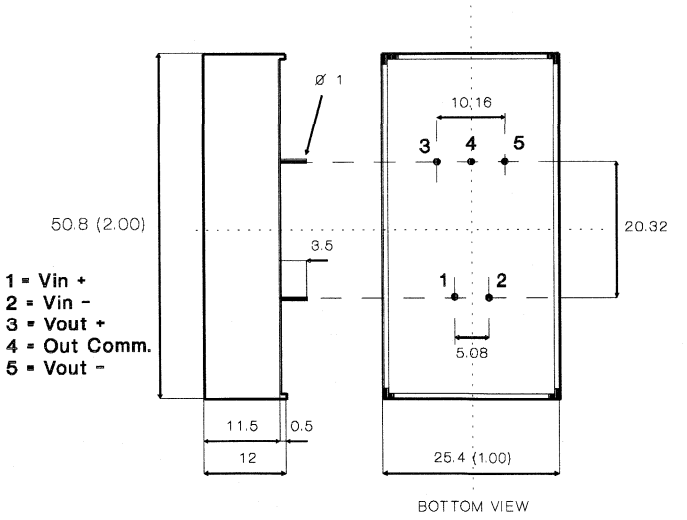
C1


33.0 (1.30)
16.5
(0.65)
0.4 (0.016)
>5
(0.20)
Ø 1 (0.04)
1 = Vin +
2 = Vin -
3 = Vout +15V
4 = Vout -15V
5 = Common Out
6 = Vout +5V
3
4
5
6
5.08
(0.20)
5.08
(0.20)
10.16
(0.40)
20.32
(0.80)
33.0
(1.30)
5.08 (0.20)
1
2
Bottom View

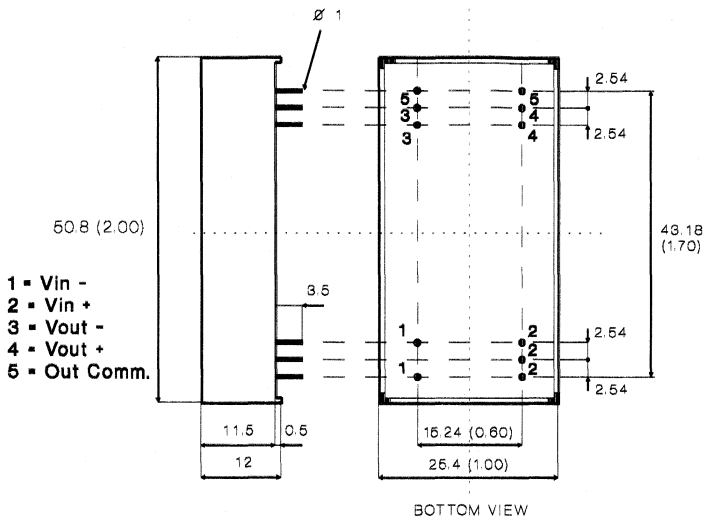
C2


33.0 (1.30)
16.5
(0.65)
0.4 (0.016)
>5
(0.20)
Ø 1 (0.04)
1 = Vin +
2 = Vin -
3 = + 5Vout
4 = - 5Vout
5 = Common Out
3
4
5
10.16
(0.40)
10.16
(0.40)
20.32
(0.80)
33.0
(1.30)
5.08 (0.20)
1
2
Bottom View

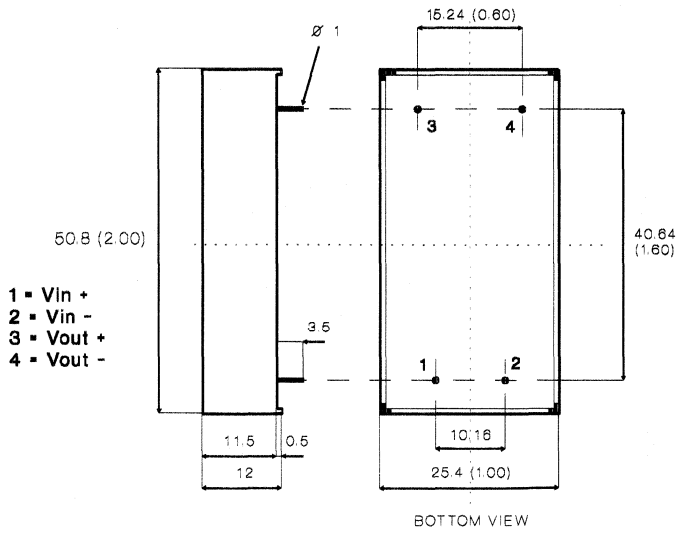
D


Ø 1
10.16
3
4
5
50.8 (2.00)
20.32
3.5
1
2
5.08
1 = Vin +
2 = Vin -
3 = Vout +
4 = Out Comm.
5 = Vout -
11.5
0.5
12
25.4 (1.00)
BOTTOM VIEW

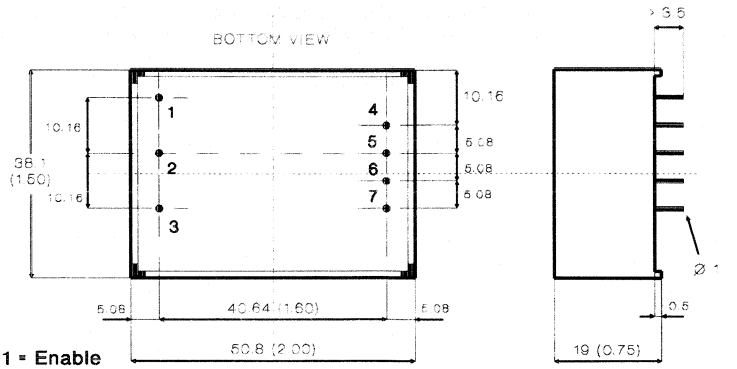
D1


Ø 1
2.54
2.54
50.8 (2.00)
43.18
(1.70)
1 = Vin -
2 = Vin +
3 = Vout -
4 = Vout +
5 = Out Comm.
3.5
2.54
2.54
11.5
0.5
12
15.24 (0.60)
25.4 (1.00)
BOTTOM VIEW

D2

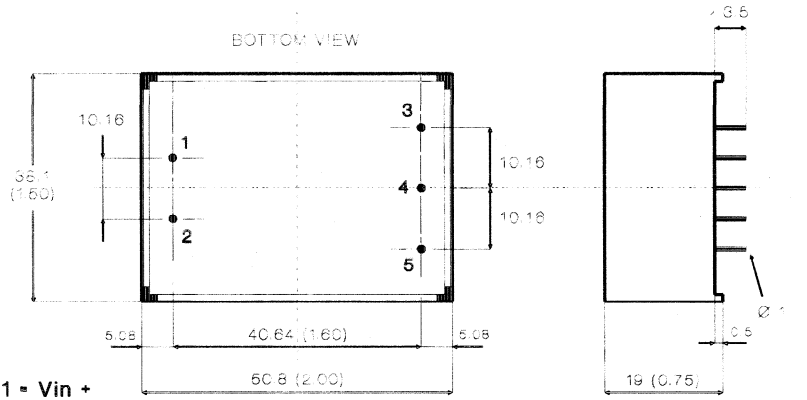

15.24 (0.60)
Ø 1
50.8 (2.00)
40.64
(1.60)
1 = Vin +
2 = Vin -
3 = Vout +
4 = Vout -
3.5
11.5
0.5
12
10.16
25.4 (1.00)
BOTTOM VIEW

E



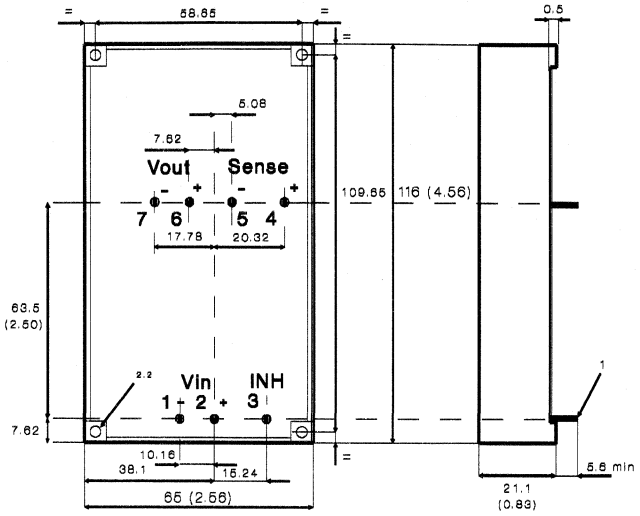
1 = Enable
2 = Vin -
3 = Vin +
4 = Vout -15V
5 = Vout +15V
6 = Out Comm.
7 = Vout +5V

E1

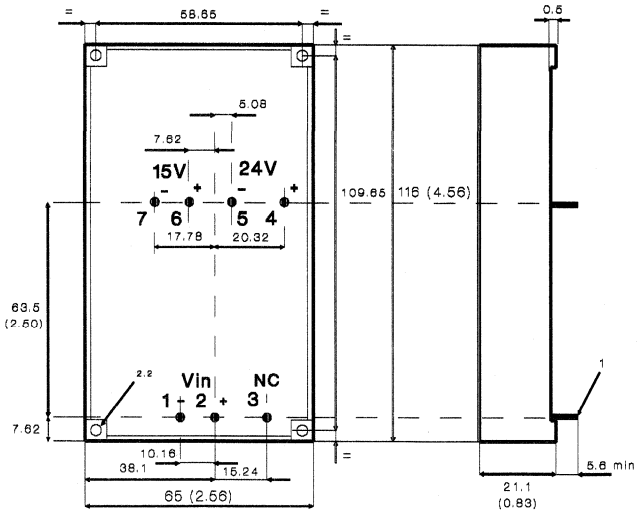


1 = Vin +
2 = Vin -
3 = Vout -
4 = Out Comm.
5 = Vout +

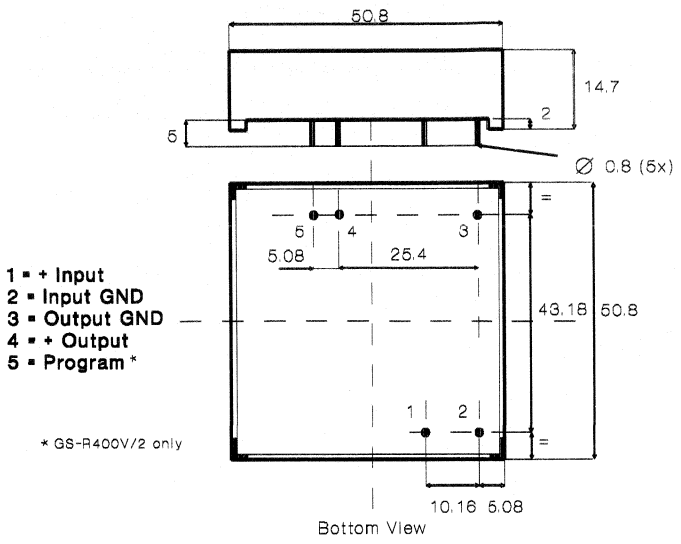
F1


58.65
0.5
5.08
7.62
Vout
Sense
7 6 5 4
17.78
20.32
109.65
116 (4.56)
63.5
(2.50)
2.2
Vin
INH
1 2 3
7.62
10.16
38.1
15.24
65 (2.56)
5.6 min
21.1
(0.83)
Bottom view

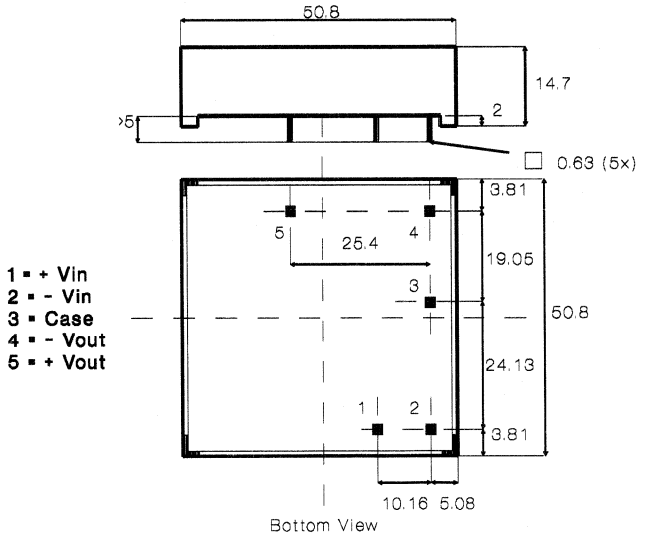
F2


58.65
0.5
5.08
7.62
15V
24V
7 6 5 4
17.78
20.32
109.65
116 (4.56)
63.5
(2.50)
2.2
Vin
NC
1 2 3
7.62
10.16
38.1
15.24
65 (2.56)
5.6 min
21.1
(0.83)
Bottom view

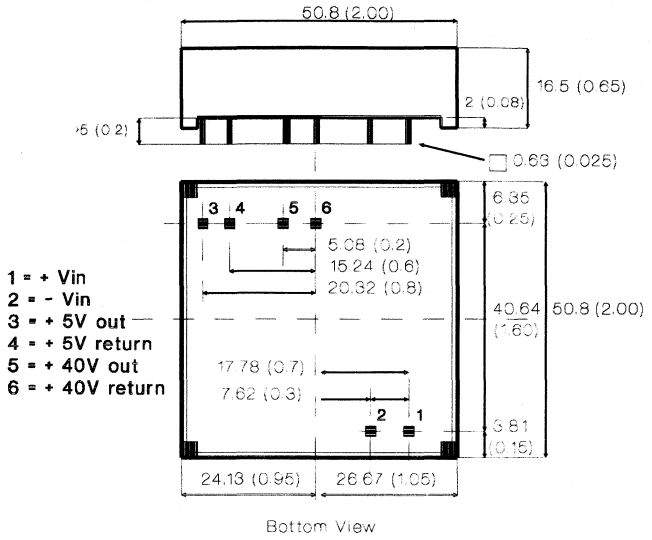
G


50.8
14.7
2
5
Ø 0.8 (5x)
5
4
3
5.08
25.4
43.18
50.8
1 = + Input
2 = Input GND
3 = Output GND
4 = + Output
5 = Program *
* GS-R400V/2 only
1
2
10.16
5.08
Bottom View

G1

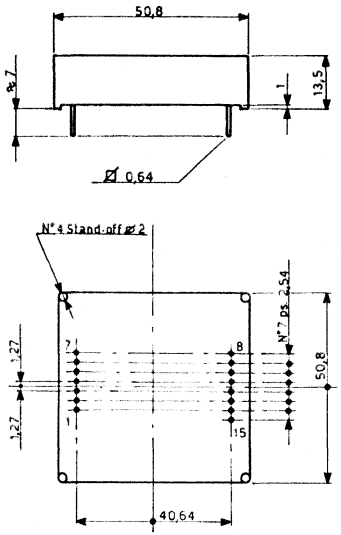

50.8
14.7
2
5
0.63 (5x)
3.81
5
25.4
4
19.05
3
50.8
24.13
1
2
3.81
1 = + Vin
2 = - Vin
3 = Case
4 = - Vout
5 = + Vout
10.16
5.08
Bottom View

G2

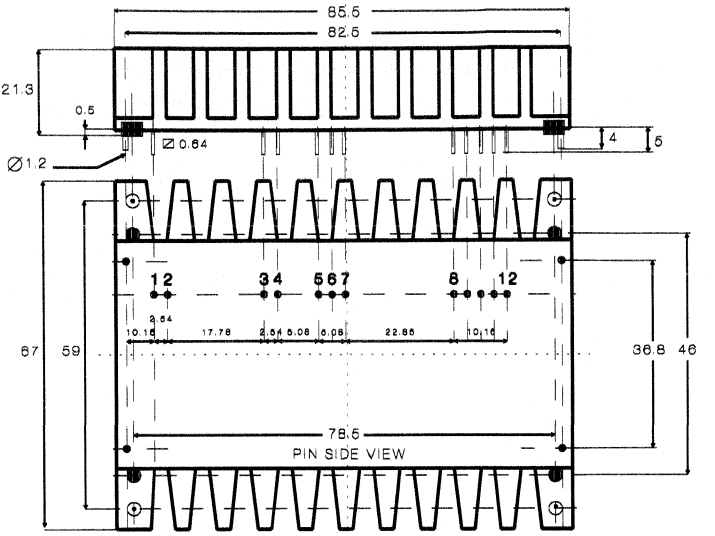


Bottom View

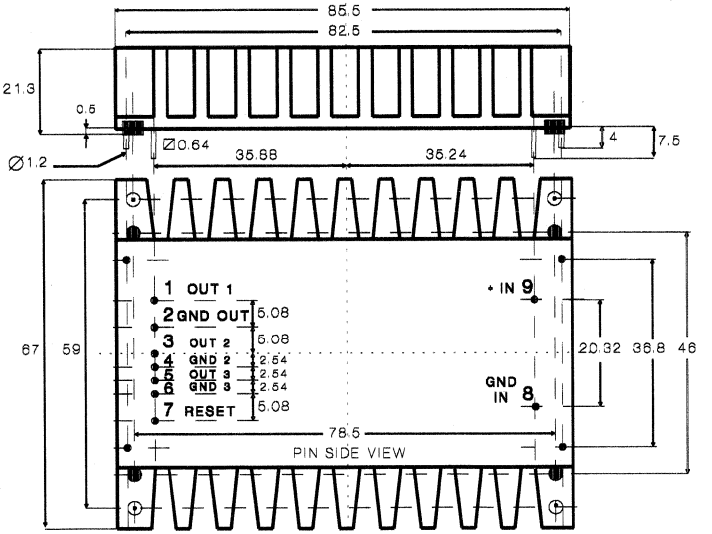
GD



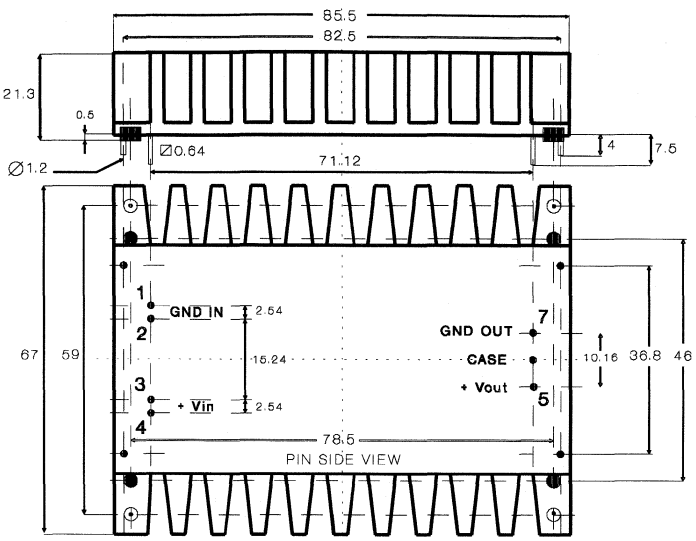
H


85.5
82.5
21.3
0.5
⊠0.64
Ø1.2
4
5
1 2
3 4
5 6 7
8
12
3.54
10.16
17.78
2.54
5.08
5.08
22.86
10.16
67
59
36.8
46
78.5
PIN SIDE VIEW

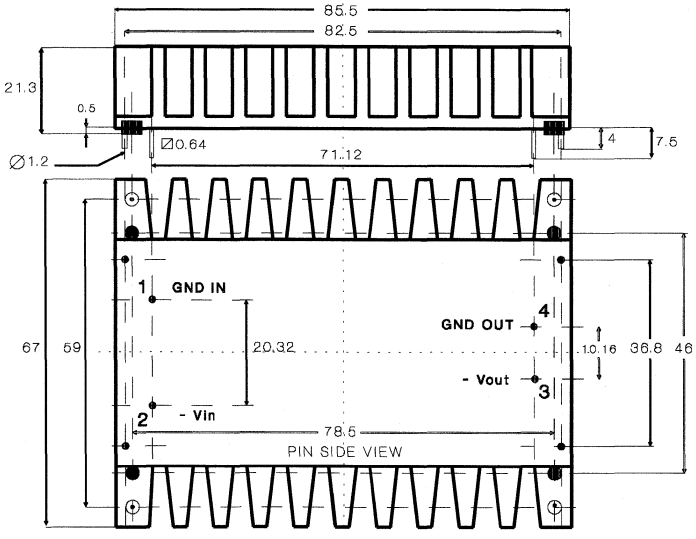
H1


85.5
82.5
21.3
0.5
⊠0.64
Ø1.2
35.88
35.24
4
7.5
1 OUT 1
2 GND OUT
3 OUT 2
4 GND 2
5 OUT 3
6 GND 3
7 RESET
5.08
5.08
2.54
2.54
2.54
5.08
+ IN 9
GND IN 8
67
59
20.32
36.8
46
78.5
PIN SIDE VIEW

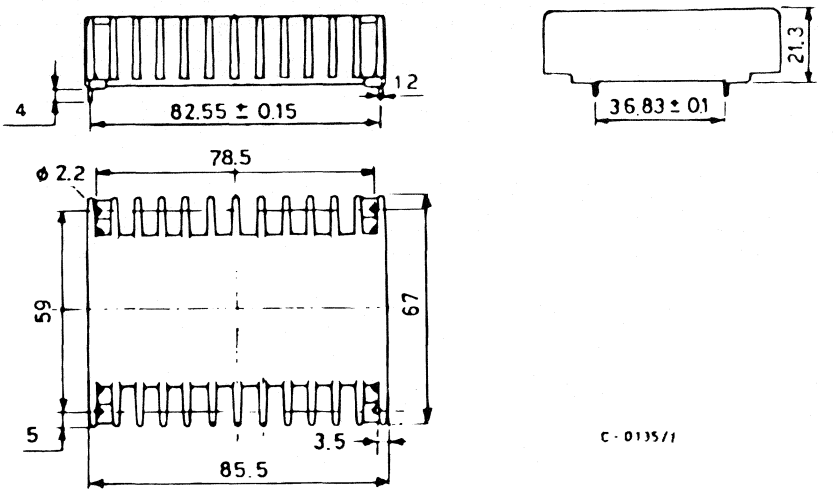
H2


85.5
82.5
21.3
0.5
Ø0.64
Ø1.2
71.12
4
7.5
1
GND IN
2
2.54
15.24
2.54
3
+ Vin
4
78.5
PIN SIDE VIEW
67
59
GND OUT
7
CASE
+ Vout
5
10.16
36.8
46

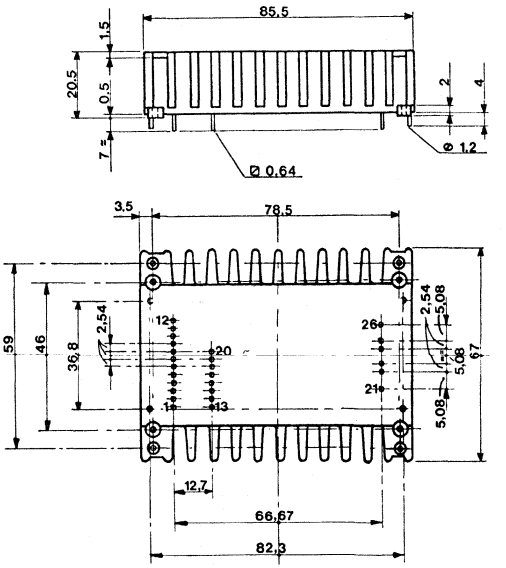
H3


85.5
82.5
21.3
0.5
Ø0.64
Ø1.2
71.12
4
7.5
1
GND IN
20.32
2
- Vin
78.5
PIN SIDE VIEW
67
59
GND OUT
4
- Vout
3
10.16
36.8
46

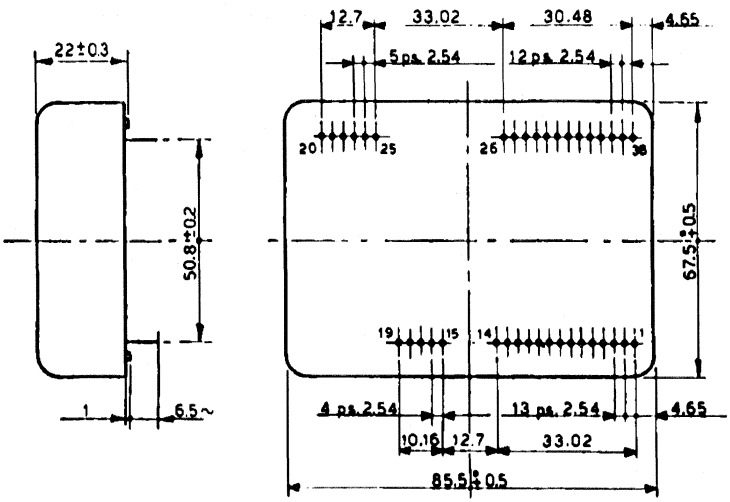
HD


4
82.55 ± 0.15
12
21.3
36.83 ± 01
ø 2.2
78.5
59
67
5
3.5
85.5
C - 0135/1

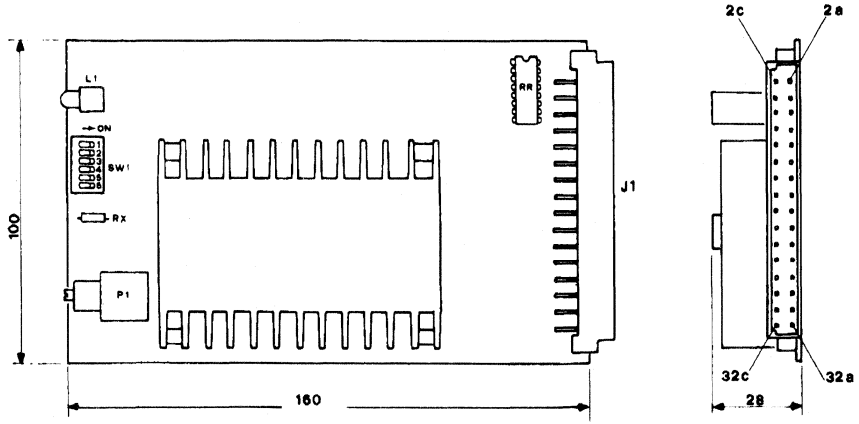
HM


85.5
1.5
20.5
0.5
7
2
4
ø 1.2
Ø 0.64
3.5
78.5
59
46
36.8
2.54
12
20
1
13
26
21
2.54
5.08
5.08
5.08
67
12.7
66.67
82.3

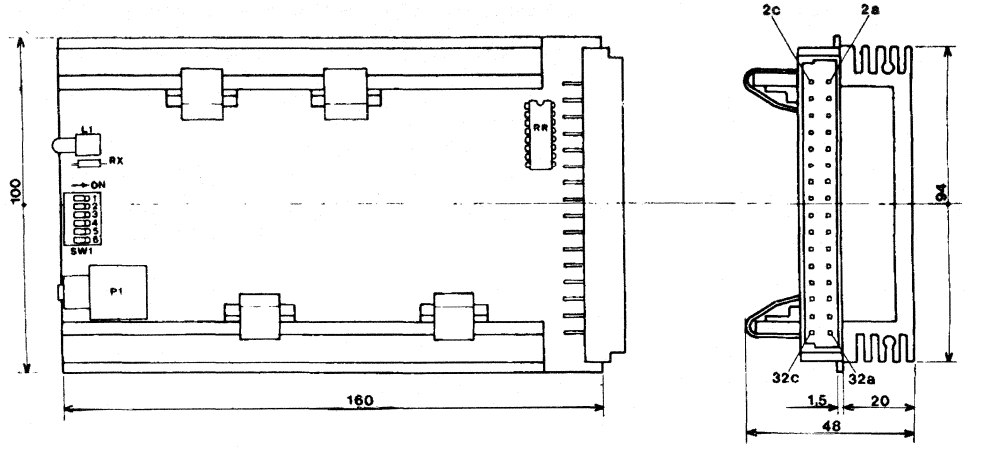
L


12.7
33.02
30.48
4.65
22±0.3
5 ps. 2.54
12 ps. 2.54
20
25
26
38
50.8±0.2
67.5±0.5
19
15
14
1
1
6.5~
4 ps. 2.54
13 ps. 2.54
4.65
10.16
12.7
33.02
85.5±0.5

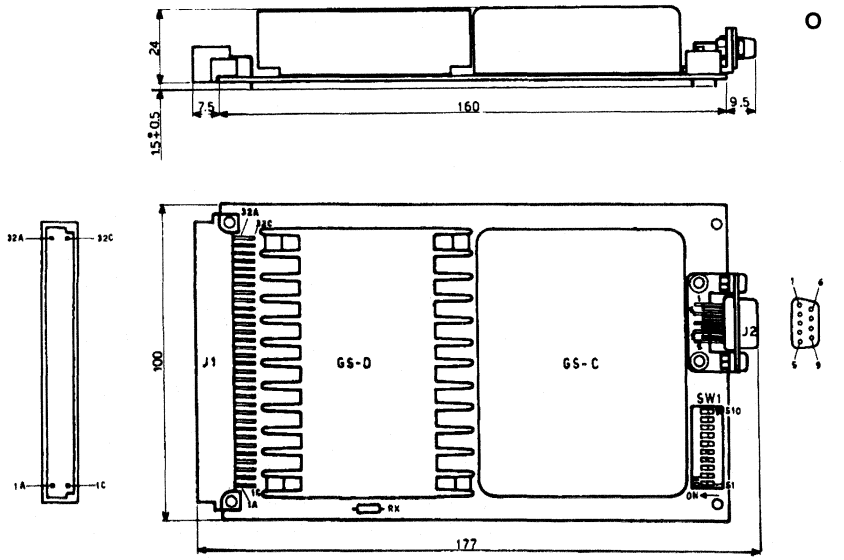
M

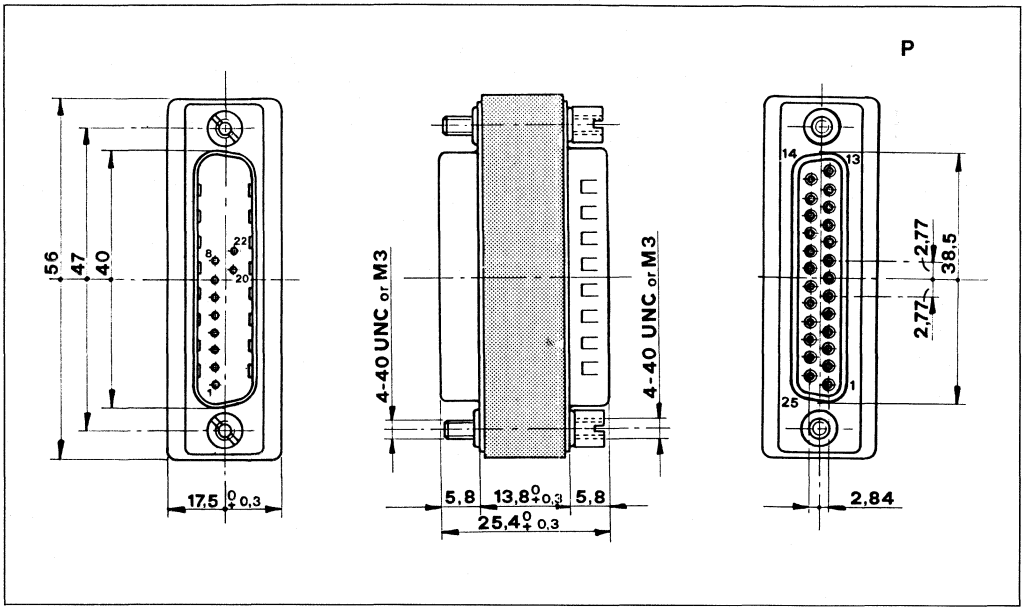

L1
ON
SW1
RX
P1
RR
J1
100
160
2c
2a
32c
32a
28

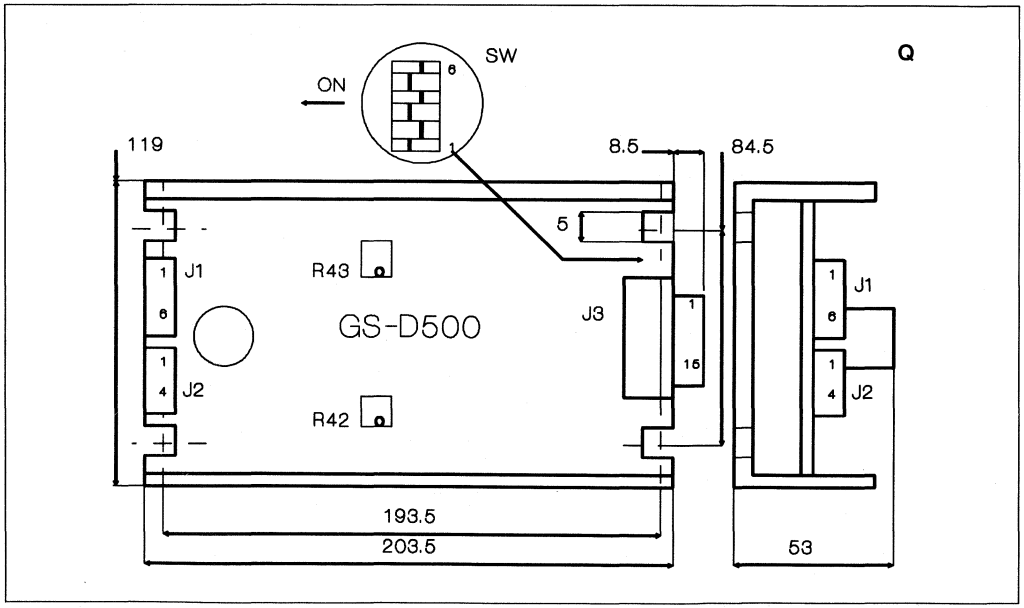
N


100
L1
RX
ON
SW1
P1
RR
160
2c
2a
32c
32a
94
1,5
20
48

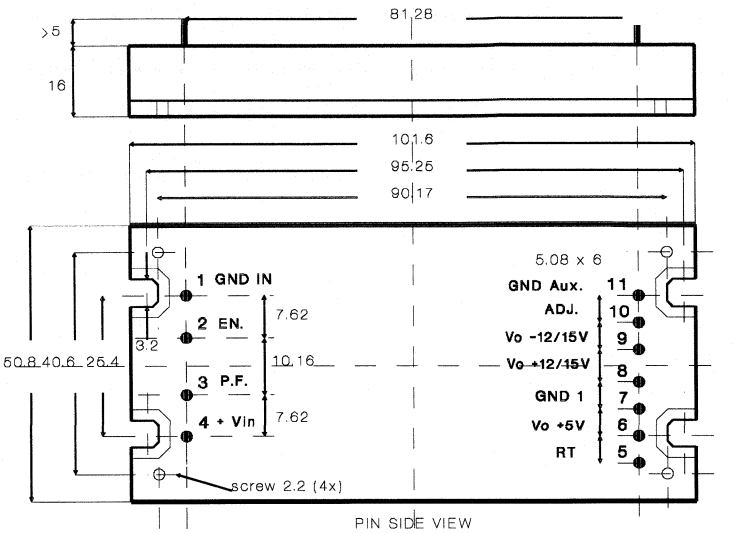
O


24
15±0.5
7.5
160
9.5
32A
32C
1A
1C
100
J1
GS-D
GS-C
J2
SW1
ON
177
RX

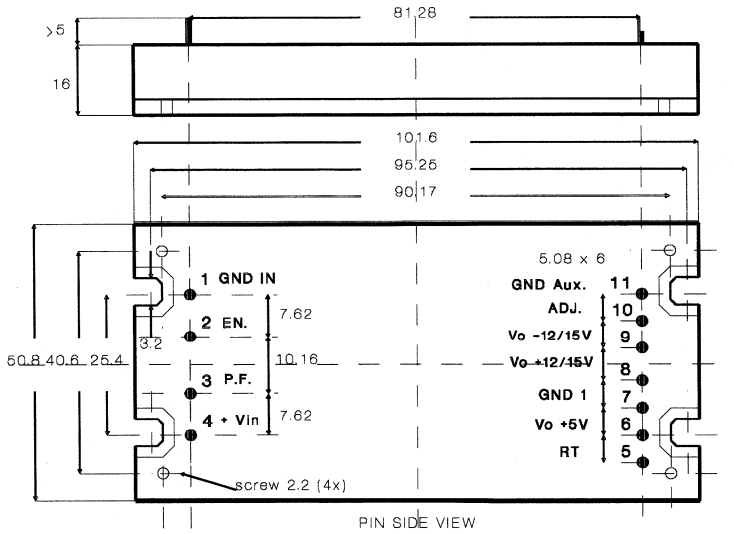

P
56
47
40
8
22
20
1
17,5 0 0,3
4-40 UNC or M3
4-40 UNC or M3
5,8
13,8 0 0,3
5,8
25,4 0 0,3
14
13
25
1
2,77
2,77
38,5
2,84


Q
SW
ON
6
1
119
8.5
84.5
5
J1
R43
GS-D500
J3
1
16
J1
J2
R42
193.5
203.5
53

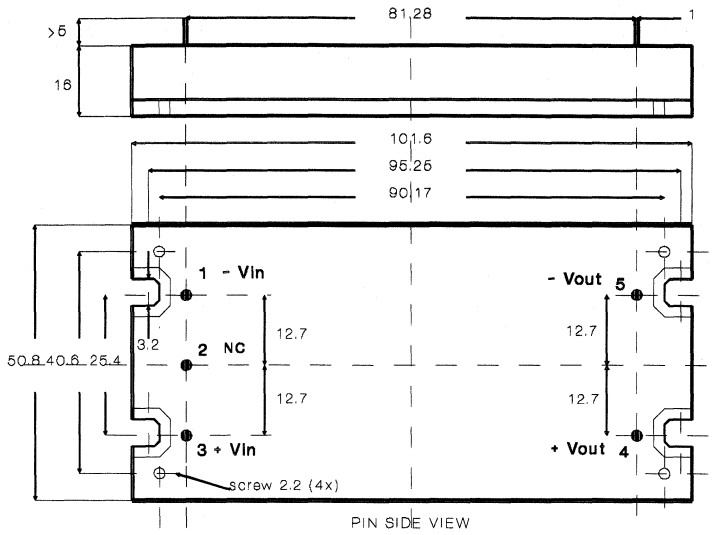
R


81.28
>5
16
101.6
95.25
90.17
1 GND IN
2 EN.
3 P.F.
4 + Vin
7.62
10.16
7.62
3.2
50.8 40.6 25.4
screw 2.2 (4x)
5.08 x 6
GND Aux. 11
ADJ. 10
Vo -12/15V 9
Vo +12/15V 8
GND 1 7
Vo +5V 6
RT 5
PIN SIDE VIEW

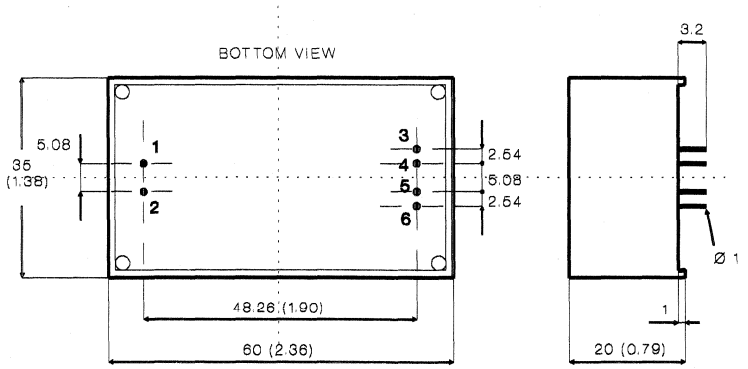
R1


81.28
>5
16
101.6
95.25
90.17
1 GND IN
2 EN.
3 P.F.
4 + Vin
7.62
10.16
7.62
3.2
50.8 40.6 25.4
screw 2.2 (4x)
5.08 x 6
GND Aux. 11
ADJ. 10
Vo -12/15V 9
Vo +12/15V 8
GND 1 7
Vo +5V 6
RT 5
PIN SIDE VIEW

R2

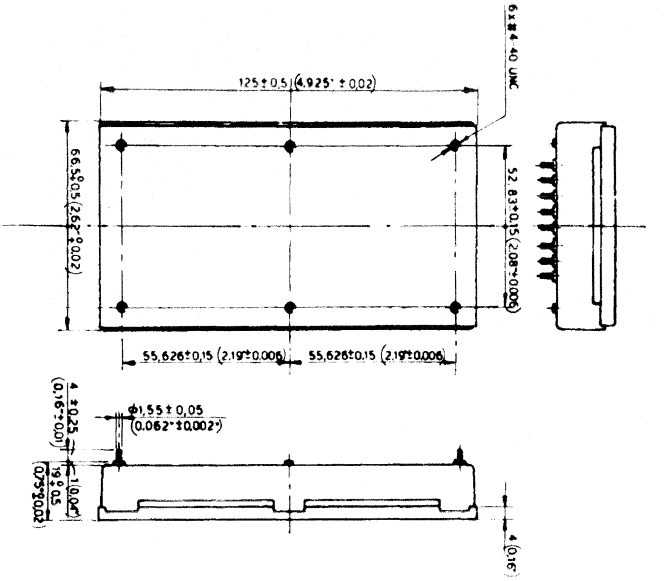


S

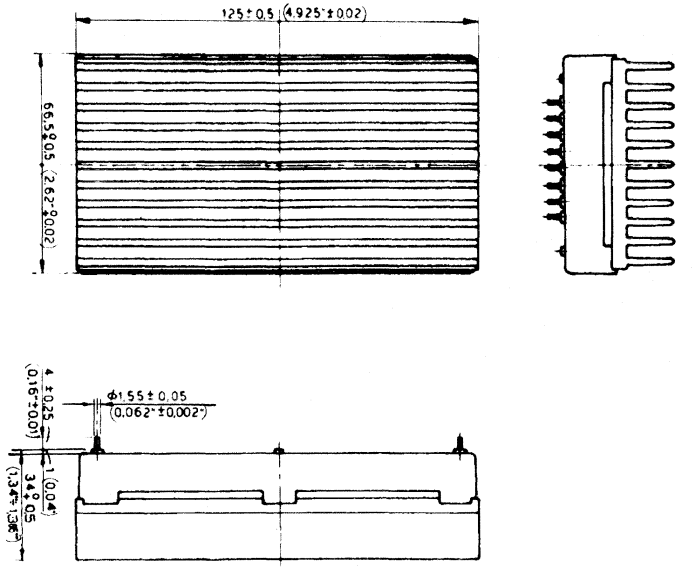


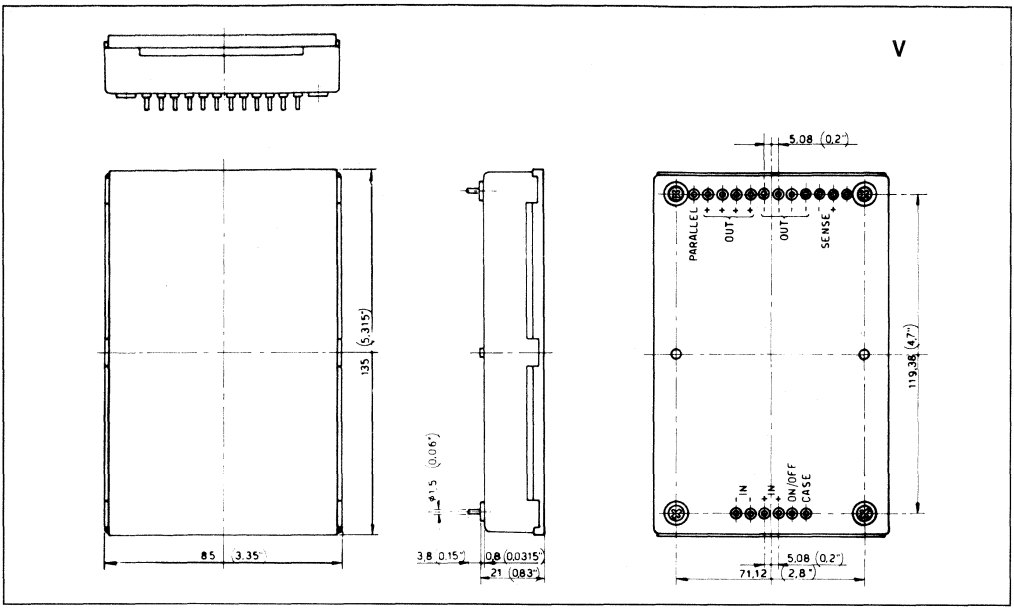
1 = Vin +
2 = Vin -
3 = +5V Out
4 = +5V Return
5 = +40V Out
6 = +40V Return

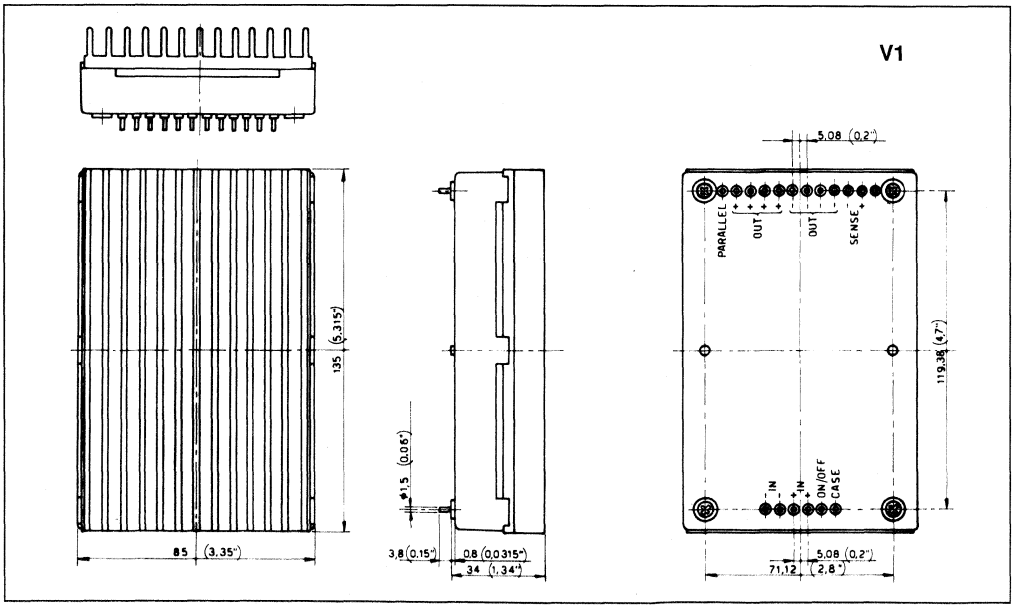
T


6 x ⌀4-40 UNC
125 ± 0.5 (4.925" ± 0.02)
66.5 ± 0.5 (2.62" ± 0.02)
52.83 ± 0.15 (2.08" ± 0.006)
55.626 ± 0.15 (2.19" ± 0.006)
55.626 ± 0.15 (2.19" ± 0.006)
4 ± 0.25 (0.16" ± 0.01)
ϕ1.55 ± 0.05 (0.062" ± 0.002")
1 (0.04")
19 ± 0.5 (0.75" ± 0.02")
4 (0.16")

T1


125 ± 0.5 (4.925" ± 0.02)
66.5 ± 0.5 (2.62" ± 0.02)
4 ± 0.25 (0.16" ± 0.01)
ϕ1.55 ± 0.05 (0.062" ± 0.002")
1 (0.04")
34 ± 0.5 (1.34" ± 0.02")


V
5.08 (0.2")
PARALLEL
OUT
OUT
SENSE
135 (5.315")
119.38 (4.7")
85 (3.35")
ϕ1.5 (0.06")
3.8 (0.15")
0.8 (0.0315")
21 (0.83")
IN
IN
ON/OFF
CASE
71.12 (2.8")


V1
5.08 (0.2")
PARALLEL
OUT
OUT
SENSE
135 (5.315")
119.38 (4.7")
85 (3.35")
ϕ1.5 (0.06")
3.8 (0.15")
0.8 (0.0315")
34 (1.34")
IN
IN
ON/OFF
CASE
71.12 (2.8")

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